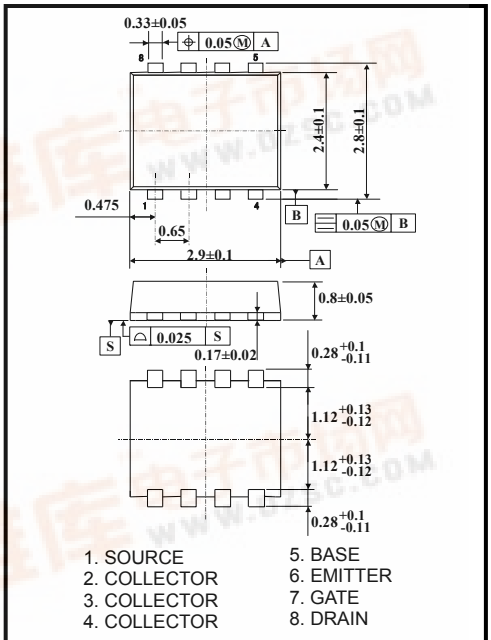
TOSHIBA Multi-Chip Transistor
Silicon NPN Epitaxial Type, Field Effect Transistor Silicon N Channel MOS Type

TPCP8H01

HIGH-SPEED SWITCHING APPLICATIONS
LORD SWITCHING APPLICATIONS
STROBE FLASH APPLICATIONS

- Multi-chip discrete device; built-in NPN transistor for main switch and N-ch MOS FET for drive
- High DC current gain: h_{FE} = 250 to 400 (I_C = 0.5 A) (NPN transistor)
- Low collector-emitter saturation voltage: $V_{CE\ (sat)}$ = 0.13 V (max) (NPN transistor)
- High-speed switching: t_f = 25 ns (typ.) (NPN transistor)



JEDEC	-
JEITA	-
TOSHIBA	2-3V1E

Weight : 0.017g (Typ.)

Absolute Maximum Ratings (Ta = 25°C)

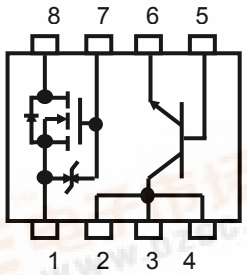
Transistor

Characteristics		Symbol	Rating	Unit
Collector-base voltage		V_{CBO}	100	V
Collector-emitter voltage		V_{CEX}	80	V
		V_{CEO}	50	
Emitter-base voltage		V_{EBO}	6	V
Collector current	DC (Note 1)	I_C	5.0	A
	Pulse (Note 1)	I_{CP}	7.0	
Base current		I_B	0.5	A
Collector power dissipation (NPN)		P_C (Note 2)	1.0	W
Junction temperature		T_j	150	°C

MOS FET

Characteristics		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	±10	V
Drain Current	DC	I_D	100	mA
	Pulse	I_{DP}	200	
Channel Temperature		T_{ch}	150	°C

Circuit Configuration



Note 1: Ensure that the junction (channel) temperature does not exceed 150°C.

Note 2: Device mounted on a glass-epoxy board (FR-4, 25.4 × 25.4 × 1.6 mm, Cu area: 645 mm^2)

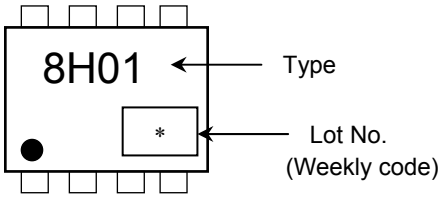
Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Please handle with caution.

Common Absolute Maximum Rating (Ta = 25°C)

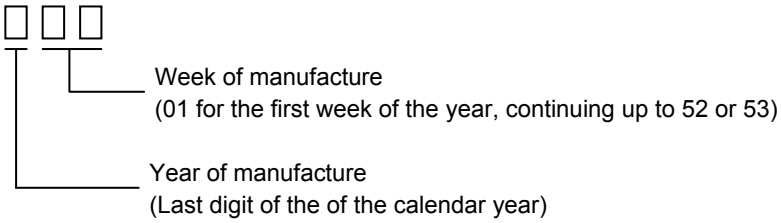
Characteristics	Symbol	Rating	Unit
Storage temperature range	T_{stg}	−55 to 150	°C

Marking (Note 4)



Note 4: The mark "●" on the lower left of the marking indicates Pin 1.

* Weekly code (three digits)

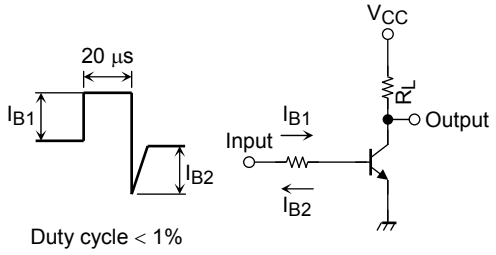


Electrical Characteristics (Ta = 25°C)

Transistor

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current		I_{CBO}	V_{CB} = 100 V, I_E = 0	—	—	100	nA
Emitter cut-off current		I_{EBO}	V_{EB} = 6 V, I_C = 0	—	—	100	nA
Collector-emitter breakdown voltage		$V_{(BR)\ CEO}$	I_C = 10 mA, I_B = 0	50	—	—	V
DC current gain		h_{FE} (1)	V_{CE} = 2 V, I_C = 0.5 A	250	—	400	
		h_{FE} (2)	V_{CE} = 2 V, I_C = 1.6 A	100	—	—	
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C = 1.6 A, I_B = 53 mA	—	80	130	mV
Base-emitter saturation voltage		$V_{BE\ (sat)}$	I_C = 1.6 A, I_B = 53 mA	—	0.8	1.1	V
Collector output capacitance		C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1 MHz	—	22	—	pF
Switching time	Rise time	t_r	See Figure 1 circuit diagram.	—	65	—	ns
	Storage time	t_{stg}	V_{CC} ≒ 24 V, R_L = 15 Ω	—	500	—	
	Fall time	t_f	I_{B1} = −I_{B2} = 53 mA	—	25	—	

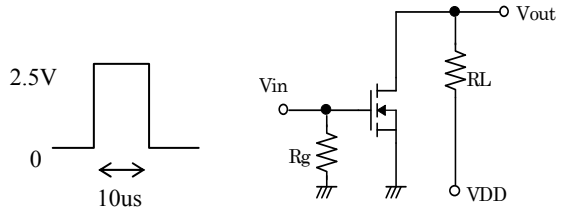
Figure 1 Switching Time Test Circuit & Timing Chart



MOS FET

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	—	±1	μA
Drain-Source breakdown voltage		$V_{(BR)DSS}$	I_D = 0.1 mA, V_{GS} = 0	20	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.6	—	1.1	V
Forward transfer admittance		|Yfs|	V_{DS} = 3 V, I_D = 10 mA	40	—	—	mS
Drain-Source ON resistance		$R_{DS(ON)}$	I_D = 10 mA , V_{GS} = 4.0 V	—	1.5	3	Ω
			I_D = 10 mA , V_{GS} = 2.5 V	—	2.2	4	
			I_D = 1 mA , V_{GS} = 1.5 V	—	5.2	15	
Input capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0, f= 1 MHz	—	9.3	—	pF
Reverse transfer capacitance		C_{rss}		—	4.5	—	
Output capacitance		C_{oss}		—	9.8	—	
Switching time	Turn-on time	t_{on}	See Figure 2 circuit diagram.	—	70	—	ns
	Turn-off time	t_{off}	V_{DD} ≒ 3 V, R_L = 300 Ω V_{GS} = 0 to 2.5 V	—	125	—	

Figure 2 Switching Time Test Circuit & Timing Chart



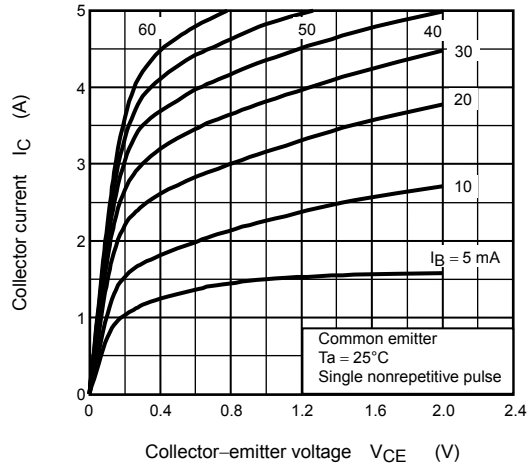
Gate Pulse Width 10 μ s, tr,tf<5ns
(Zout=50 Ω),Common Source,Ta=25°C
Duty Cycle<1%

Precautions

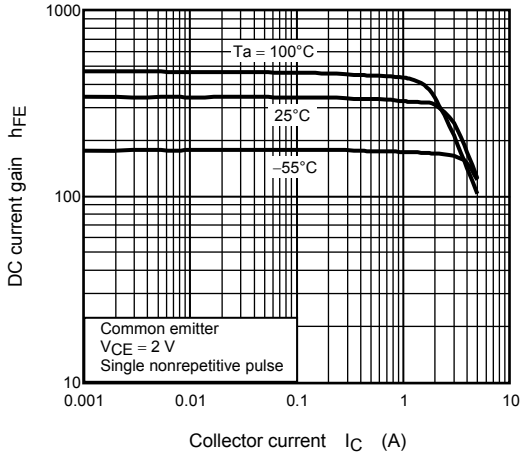
V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D=100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}.
(The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)
Please take this into consideration when using the device. The V_{GS} recommended voltage for turning on this product is 2.5 V or higher.

NPN

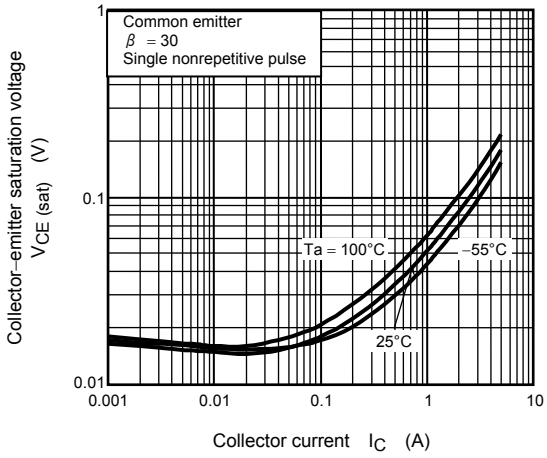
$I_C - V_{CE}$



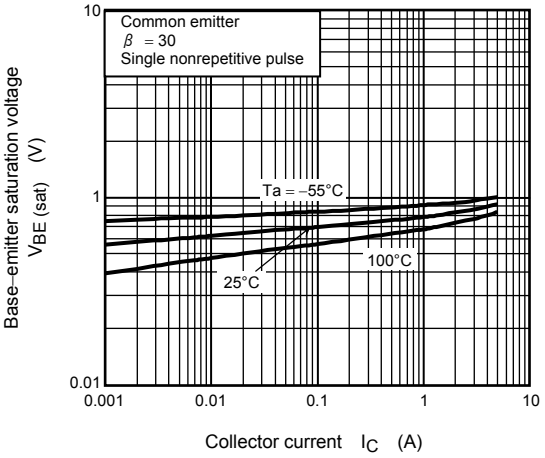
$h_{FE} - I_C$



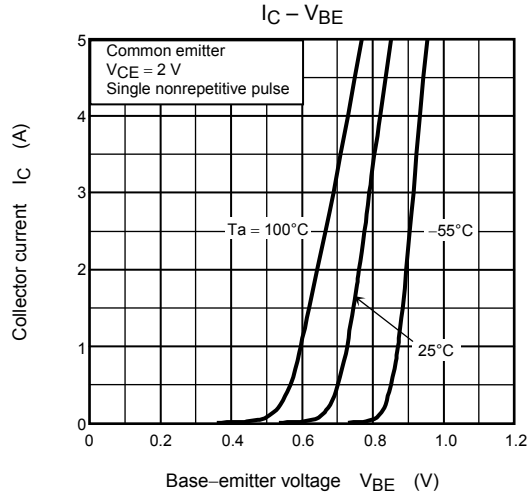
$V_{CE\ (sat)} - I_C$



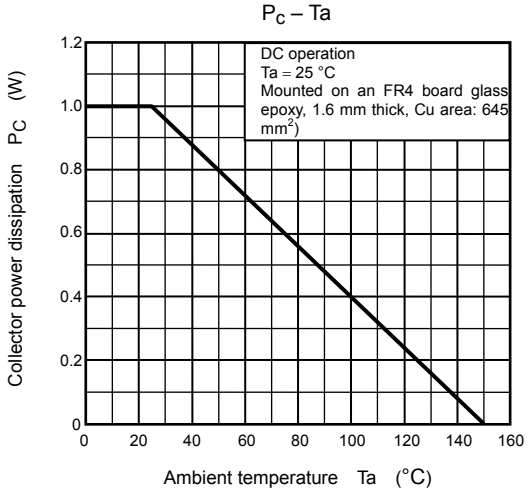
$V_{BE\ (sat)} - I_C$

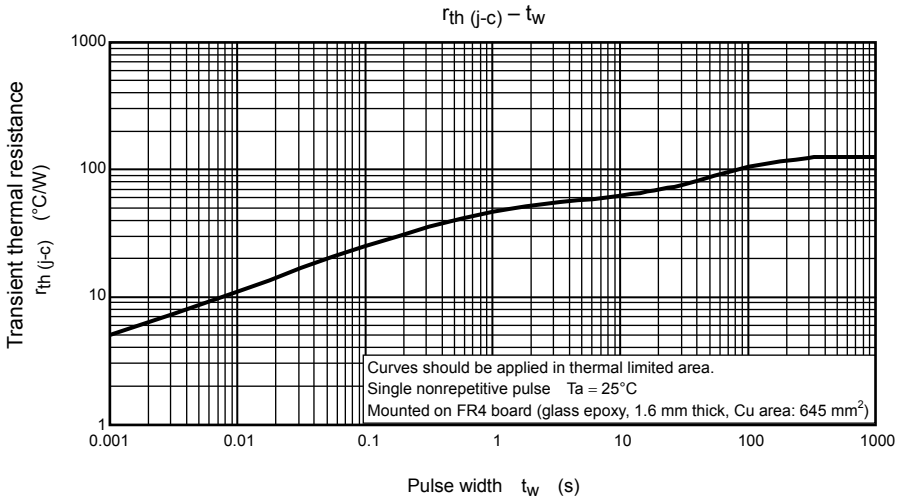


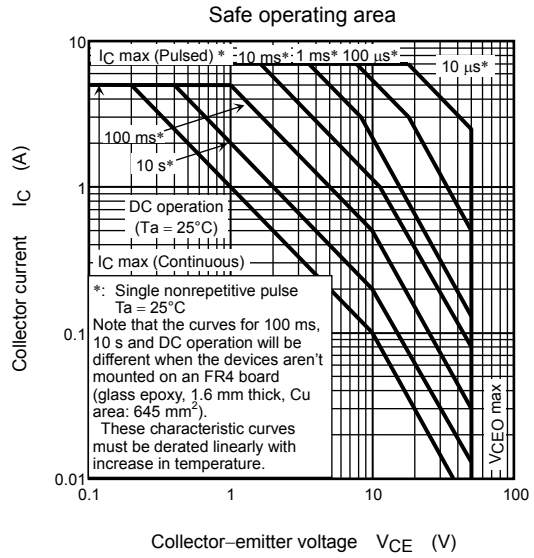
$I_C - V_{BE}$



$P_c - Ta$

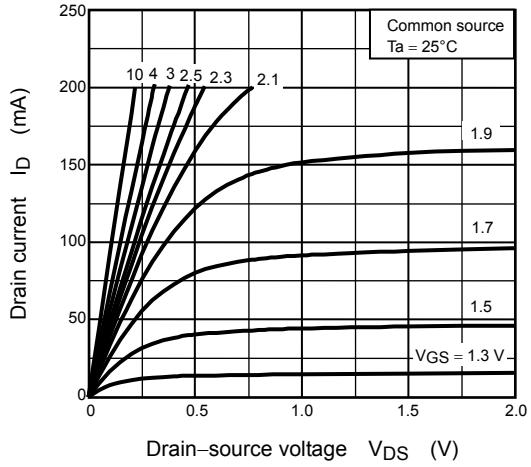



$r_{th\ (j\text{-}c)} - t_w$
Transient thermal resistance $r_{th\ (j\text{-}c)}$ (°C/W)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Curves should be applied in thermal limited area.
Single nonrepetitive pulse Ta = 25°C
Mounted on FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 mm²)
Pulse width t_w (s)

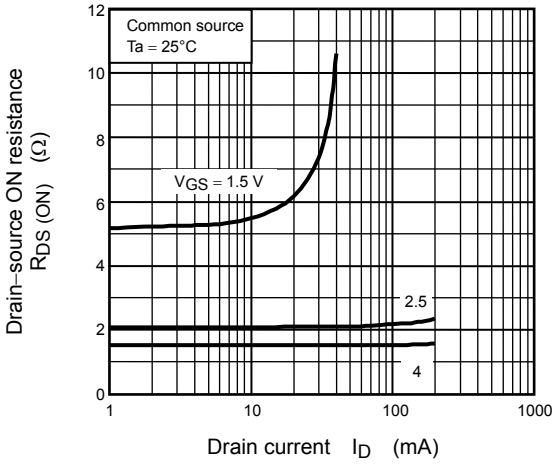

Safe operating area
Collector current I_C (A)
10
1
0.1
0.01
0.1
1
10
100
I_C max (Pulsed) *
1 ms*
100 μs*
10 μs*
100 ms*
10 s*
DC operation
(Ta = 25°C)
I_C max (Continuous)
*: Single nonrepetitive pulse
Ta = 25°C
Note that the curves for 100 ms, 10 s and DC operation will be different when the devices aren't mounted on an FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 mm²).
These characteristic curves must be derated linearly with increase in temperature.
V_{CEO} max
Collector–emitter voltage V_{CE} (V)

Nch-MOS

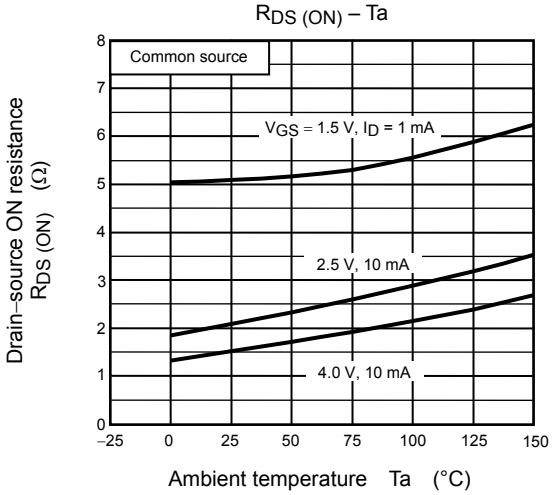
$I_D - V_{DS}$



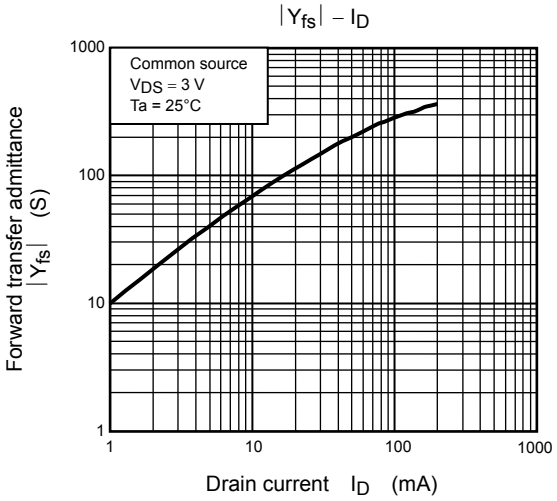
$R_{DS\ (ON)} - I_D$



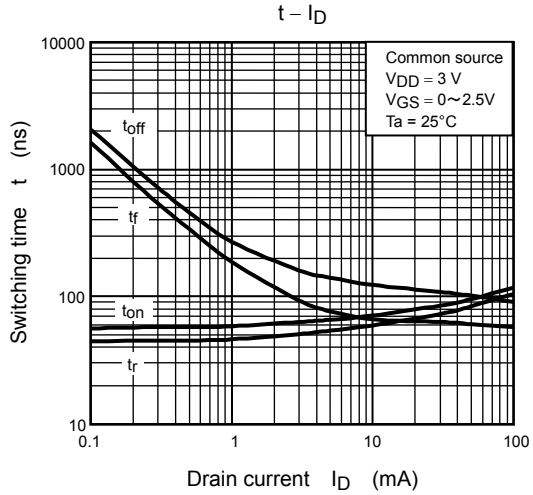
$R_{DS\ (ON)} - Ta$



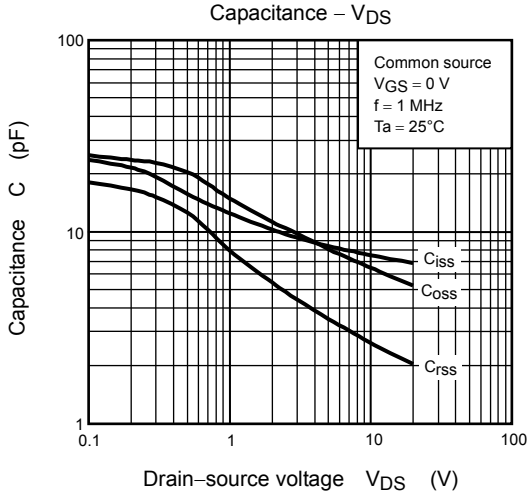
$|Y_{fs}| - I_D$



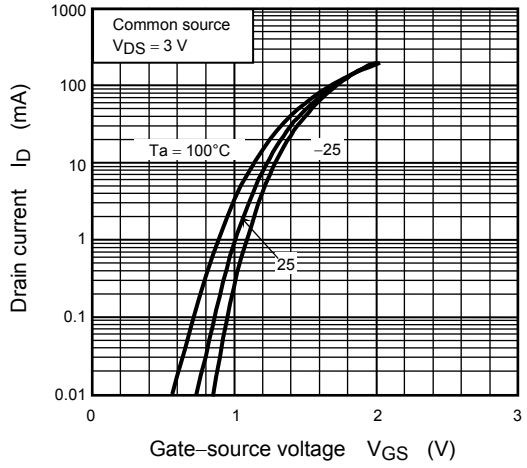
$t - I_D$



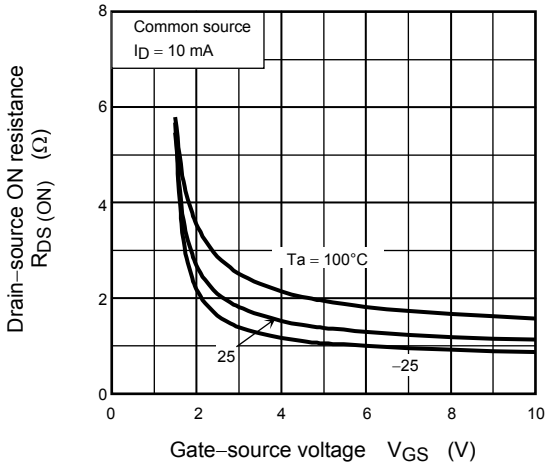
Capacitance $- V_{DS}$



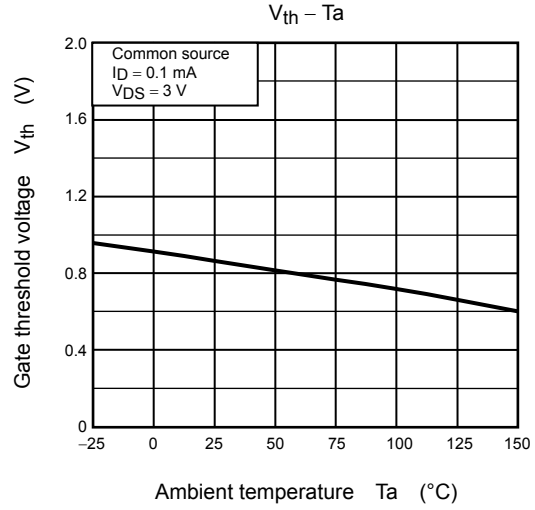
$I_D - V_{GS}$



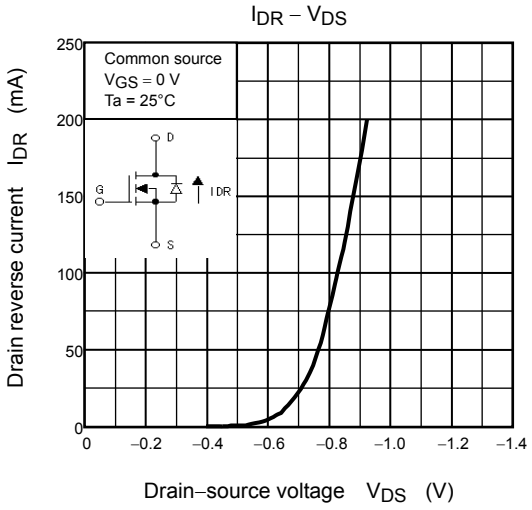
$R_{DS\ (ON)} - V_{GS}$



$V_{th} - Ta$



$I_{DR} - V_{DS}$



RESTRICTIONS ON PRODUCT USE

20070701-EN

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc.
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.).These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in his document shall be made at the customer’s own risk.
- The products described in this document shall not be used or embedded to any downstream products of which manufacture, use and/or sale are prohibited under any applicable laws and regulations.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patents or other rights of TOSHIBA or the third parties.
- Please contact your sales representative for product-by-product details in this document regarding RoHS compatibility. Please use these products in this document in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances. Toshiba assumes no liability for damage or losses occurring as a result of noncompliance with applicable laws and regulations.