MCP73827

Single Cell Lithium-Ion Charge Management Controller with Mode Indicator and Charge Current Monitor

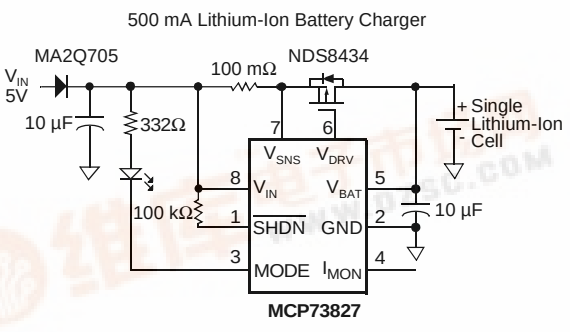
Features

- Linear Charge Management Controller for Single Lithium-Ion Cells
- High Accuracy Preset Voltage Regulation: ± 1% (max)
- Two Preset Voltage Regulation Options:
  - 4.1V - MCP73827-4.1
  - 4.2V - MCP73827-4.2
- Programmable Charge Current
- Automatic Cell Preconditioning of Deeply Depleted Cells, Minimizing Heat Dissipation During Initial Charge Cycle
- Charge Status Output for LED Drive or Microcontroller Interface
- Charge Current Monitor Output
- Automatic Power-Down when Input Power Removed
- Temperature Range: -20°C to +85°C
- Packaging: 8-Pin MSOP

Applications

- Single Cell Lithium-Ion Battery Chargers
- Personal Data Assistants
- Cellular Telephones
- Hand Held Instruments
- Cradle Chargers
- Digital Cameras

Typical Application Circuit



Description

The MCP73827 is a linear charge management controller for use in space-limited, cost sensitive applications. The MCP73827 combines high accuracy constant voltage, controlled current regulation, cell preconditioning, and charge status indication in a space saving 8-pin MSOP package. The MCP73827 provides a stand-alone charge management solution.

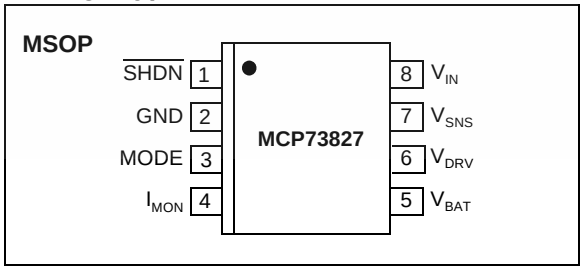
The MCP73827 charges the battery in three phases: preconditioning, controlled current, and constant voltage. If the battery voltage is below the internal low-voltage threshold, the battery is preconditioned with a foldback current. The preconditioning phase protects the lithium-ion cell and minimizes heat dissipation.

Following the preconditioning phase, the MCP73827 enters the controlled current phase. The MCP73827 allows for design flexibility with a programmable charge current set by an external sense resistor. The charge current is ramped up, based on the cell voltage, from the foldback current to the peak charge current established by the sense resistor. This phase is maintained until the battery reaches the charge-regulation voltage.

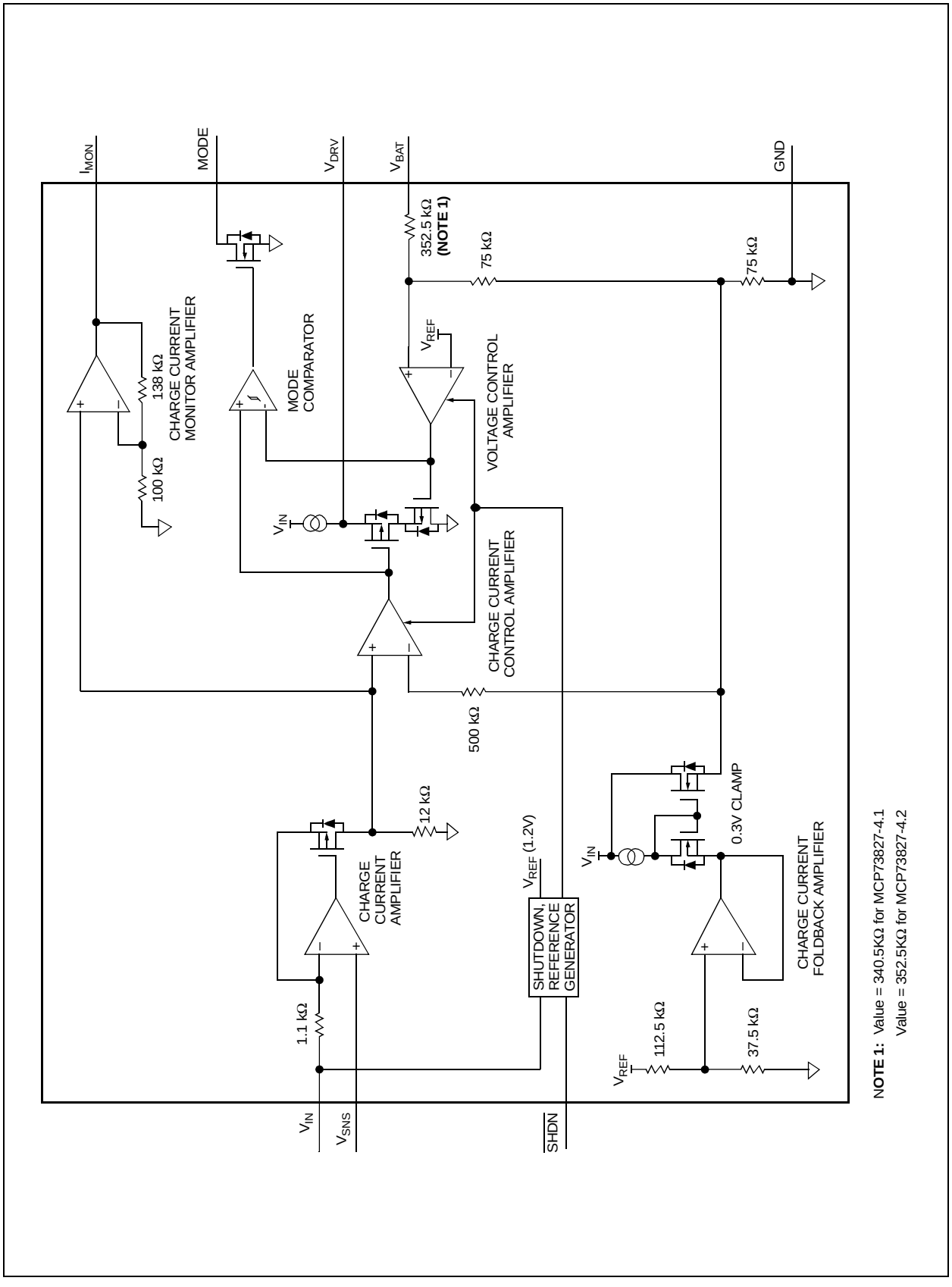
Then, the MCP73827 enters the final phase, constant voltage. The accuracy of the voltage regulation is better than ±1% over the entire operating temperature range and supply voltage range. The MCP73827-4.1 is preset to a regulation voltage of 4.1V, while the MCP73827-4.2 is preset to 4.2V. The charge status output, MODE, indicates when the charge cycle has transitioned to constant voltage mode. The charge cycle can be terminated by a timer that is started when the MODE pin goes to a logic High or by monitoring the charge current monitor output, I_{MON}, for a minimum current.

The MCP73827 operates with an input voltage range from 4.5V to 5.5V. The MCP73827 is fully specified over the ambient temperature range of -20°C to +85°C.

Package Type



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{IN} ..... -0.3V to 6.0V
All inputs and outputs w.r.t. GND ..... -0.3 to (V_{IN}+0.3)V
Current at MODE Pin ..... +/-30 mA
Current at V_{DRV} ..... +/-1 mA
Maximum Junction Temperature, T_J ..... 150°C
Storage temperature ..... -65°C to +150°C
ESD protection on all pins ..... ≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Pin	Name	Description
1	$\overline{SHDN}$	Logic Shutdown
2	GND	Battery Management 0V Reference
3	MODE	Charge Status Output
4	I_{MON}	Charge Current Monitor
5	V_{BAT}	Cell Voltage Monitor Input
6	V_{DRV}	Drive Output
7	V_{SNS}	Charge Current Sense Input
8	V_{IN}	Battery Management Input Supply

DC CHARACTERISTICS: MCP73827-4.1, MCP73827-4.2

Unless otherwise specified, all limits apply for V_{IN} = [V_{REG}(typ)+1V], R_{SENSE} = 500 mΩ, T_A = -20°C to +85°C.
Typical values are at +25°C. Refer to Figure 1-1 for test circuit.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{IN}	4.5	—	5.5	V	
Supply Current	I_{IN}	— —	0.5 250	15 560	µA	Shutdown, V_{SHDN} = 0V Constant Voltage Mode
Voltage Regulation (Constant Voltage Mode)						
Regulated Output Voltage	V_{REG}	4.059 4.158	4.1 4.2	4.141 4.242	V V	MCP73827-4.1 only MCP73827-4.2 only
Line Regulation	ΔV_{BAT}	-10	—	10	mV	V_{IN} = 4.5V to 5.5V, I_{OUT} = 75 mA
Load Regulation	ΔV_{BAT}	-1	±0.1	1	mV	I_{OUT}=10 mA to 75 mA
Output Reverse Leakage Current	I_{LK}	—	8	—	µA	V_{IN}=Floating, V_{BAT}=V_{REG}
External MOSFET Gate Drive						
Gate Drive Current	I_{DRV}	— 0.08	— —	1 —	mA mA	Sink, CV Mode Source, CV Mode
Gate Drive Minimum Voltage	V_{DRV}	—	1.6	—	V	
Current Regulation (Controlled Current Mode)						
Current Sense Gain	A_{CS}	—	100	—	dB	$\Delta(V_{SNS}-V_{DRV}) / \Delta V_{BAT}$
Current Limit Threshold	V_{CS}	40	53	75	mV	(V_{IN}-V_{SNS}) at I_{OUT}
Foldback Current Scale Factor	K	—	0.43	—	A/A	
Charge Status Indicator - MODE						
Threshold Voltage	V_{TH}	—	V_{REG}	—	V	
Low Output Voltage	V_{OL}	—	—	400	mV	I_{SINK} = 10 mA
Leakage Current	I_{LK}	—	—	1	µA	I_{SINK}=0 mA, V_{MODE}=5.5V
Shutdown Input - $\overline{SHDN}$						
Input High Voltage Level	V_{IH}	40	—	—	%V_{IN}	
Input Low Voltage Level	V_{IL}	—	—	25	%V_{IN}	
Input Leakage Current	I_{LK}	—	—	1	µA	V_{SHDN}=0V to 5.5V
Charge Current Monitor - I_{MON}						
Charge Current Monitor Gain	A_{IMON}	—	26	—	V/V	$\Delta V_{IMON} / \Delta(V_{IN}-V_{SNS})$

TEMPERATURE SPECIFICATIONS

Unless otherwise specified, all limits apply for V_{IN} = 4.5V-5.5V						
Parameters	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-20	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistance						
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	Single Layer SEMI G42-88 Standard Board, Natural Convection

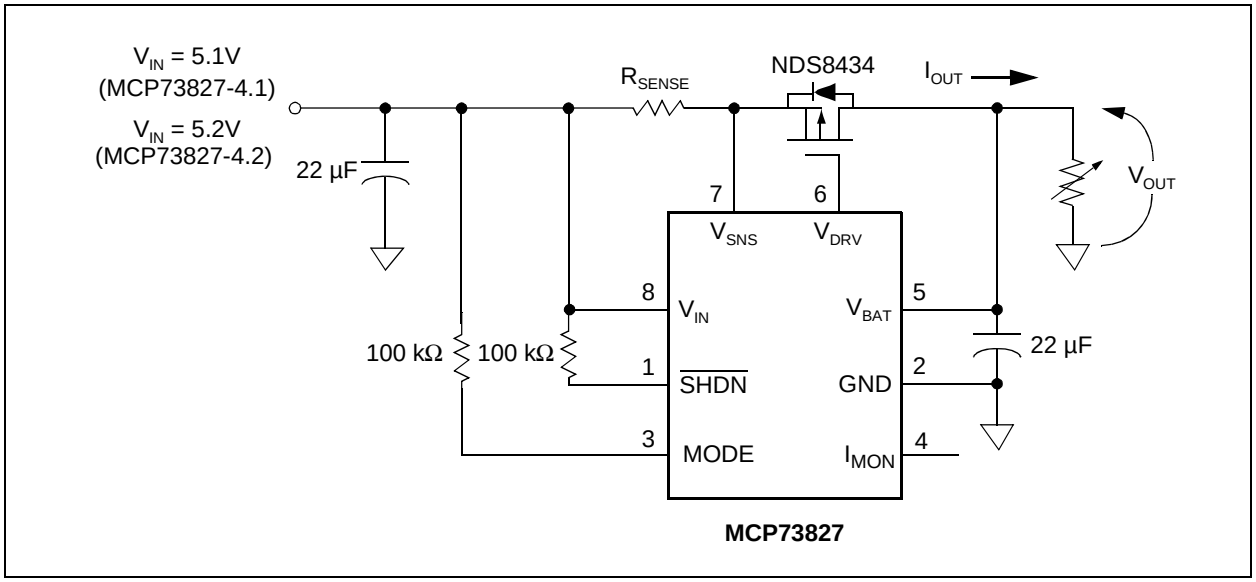


FIGURE 1-1: *MCP73827 Test Circuit.*

2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, I_{OUT} = 10 mA, Constant Voltage Mode, T_A = 25°C. Refer to Figure 1-1 for test circuit.

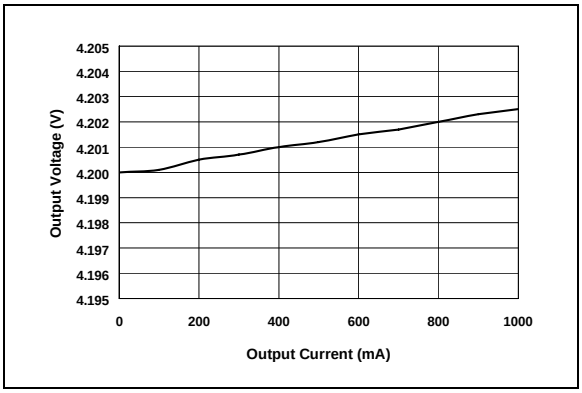


FIGURE 2-1: *Output Voltage vs. Output Current (MCP73827-4.2).*

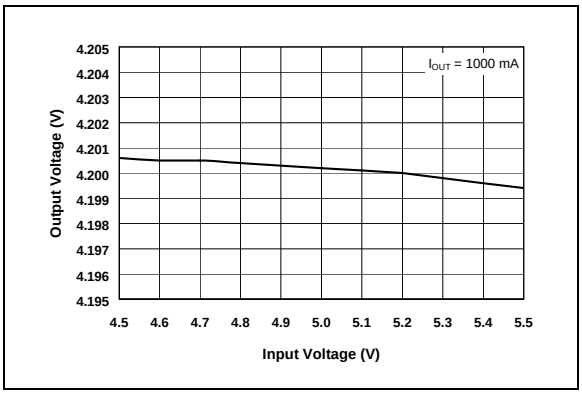


FIGURE 2-2: *Output Voltage vs. Input Voltage (MCP73827-4.2)*

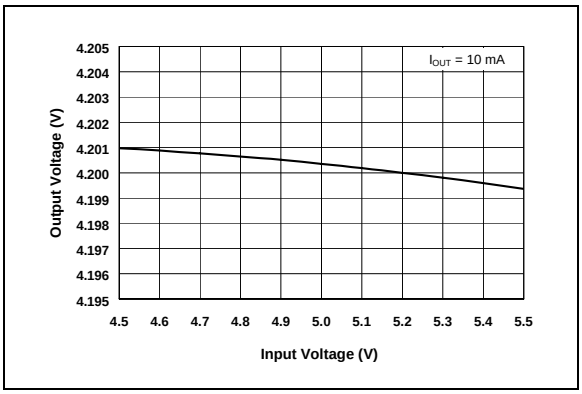


FIGURE 2-3: *Output Voltage vs. Input Voltage (MCP73827-4.2)*

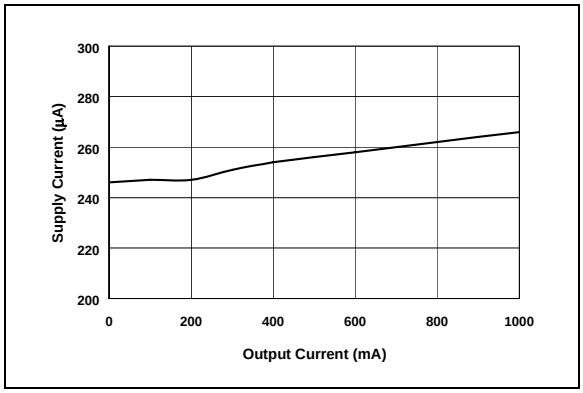


FIGURE 2-4: *Supply Current vs. Output Current.*

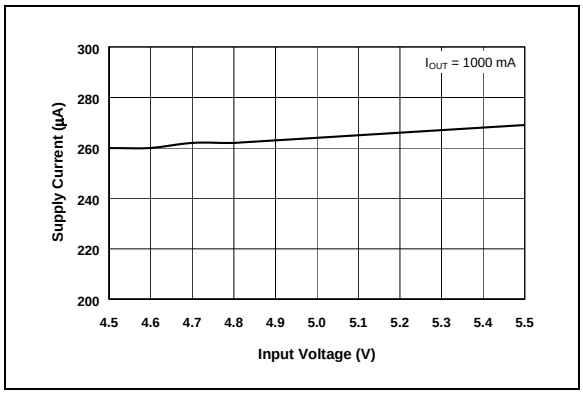


FIGURE 2-5: *Supply Current vs. Input Voltage.*

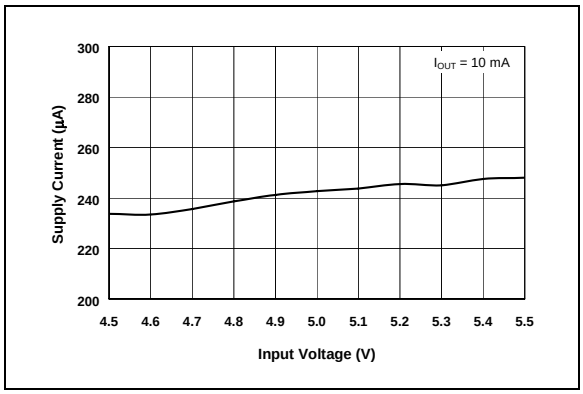


FIGURE 2-6: *Supply Current vs. Input Voltage.*

Note: Unless otherwise indicated, I_{OUT} = 10 mA, Constant Voltage Mode, T_A = 25°C. Refer to Figure 1-1 for test circuit.

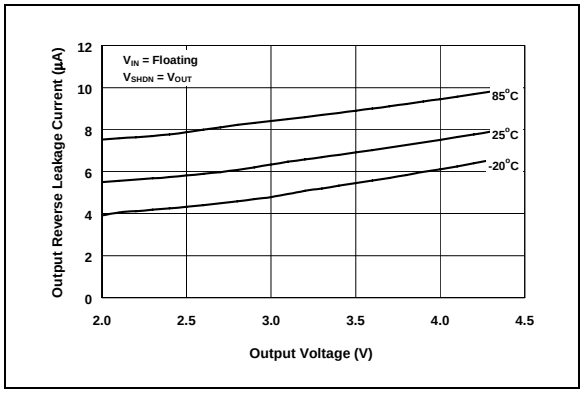


FIGURE 2-7: *Output Reverse Leakage Current vs. Output Voltage.*

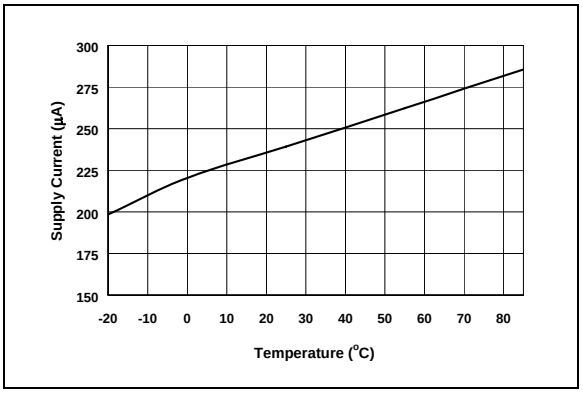


FIGURE 2-10: *Supply Current vs. Temperature.*

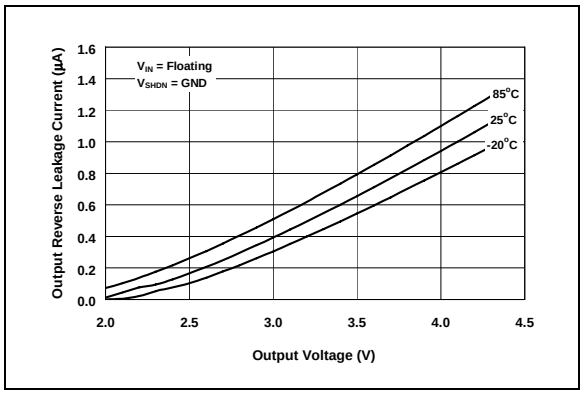


FIGURE 2-8: *Output Reverse Leakage Current vs. Output Voltage.*

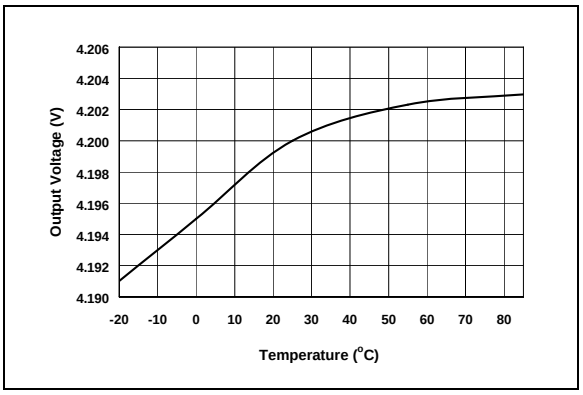


FIGURE 2-11: *Output Voltage vs. Temperature (MCP73827-4.2).*

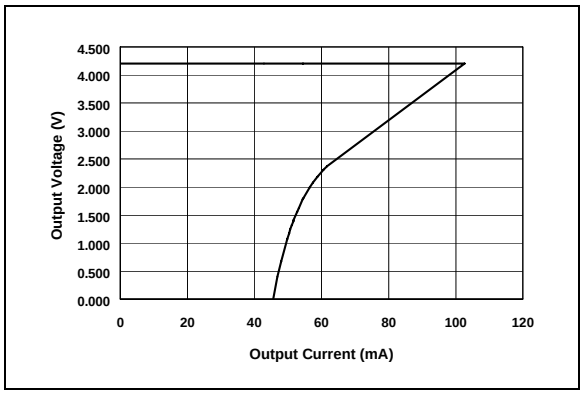


FIGURE 2-9: *Current Limit Foldback.*

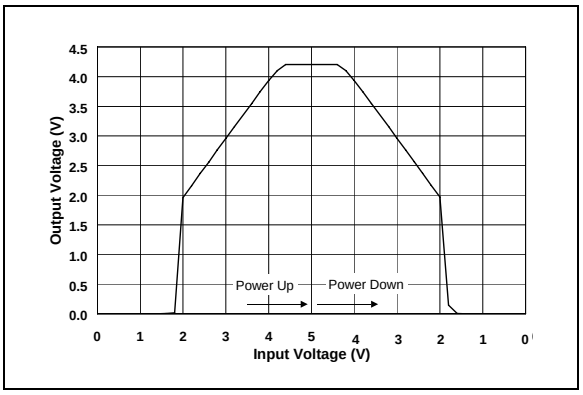


FIGURE 2-12: *Power-Up / Power-Down.*

Note: Unless otherwise indicated, I_{OUT} = 10 mA, Constant Voltage Mode, T_A = 25°C. Refer to Figure 1-1 for test circuit.

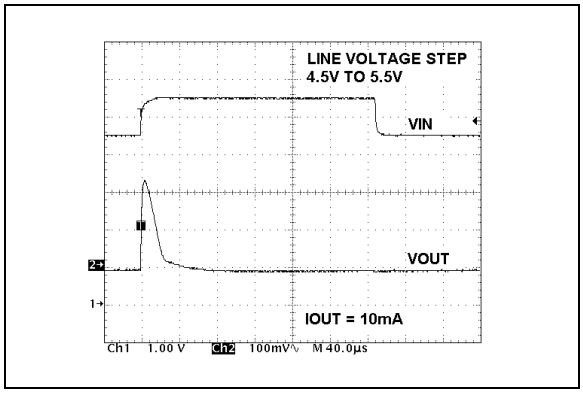


FIGURE 2-13: *Line Transient Response.*

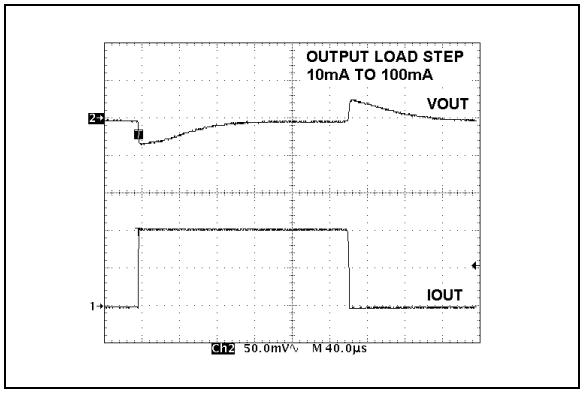


FIGURE 2-15: *Load Transient Response.*

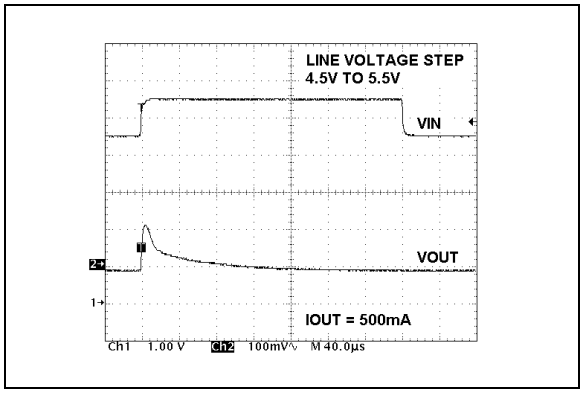


FIGURE 2-14: *Line Transient Response.*

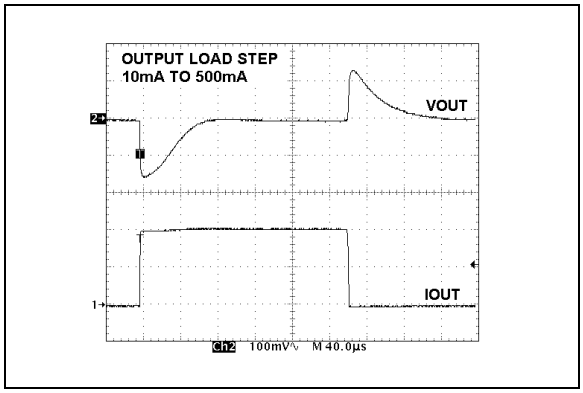


FIGURE 2-16: *Load Transient Response.*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

Pin	Name	Description
1	$\overline{SHDN}$	Logic Shutdown
2	GND	Battery Management 0V Reference
3	MODE	Charge Status Output
4	I_{MON}	Charge Current Monitor
5	V_{BAT}	Cell Voltage Monitor Input
6	V_{DRV}	Drive Output
7	V_{SNS}	Charge Current Sense Input
8	V_{IN}	Battery Management Input Supply

TABLE 3-1: *Pin Function Table.*

3.1 Logic Shutdown ($\overline{SHDN}$)

Input to force charge termination, initiate charge, or initiate recharge.

3.2 Battery Management 0V Reference (GND)

Connect to negative terminal of battery.

3.3 Charge Status Output (MODE)

Open-drain drive for connection to an LED for charge status indication. Alternatively, a pull-up resistor can be applied for interfacing to a microcontroller. A low impedance state indicates foldback current limit or controlled current phase. A high impedance indicates constant voltage phase or battery cell disconnected.

3.4 Charge Current Monitor (I_{MON})

Amplified output of the voltage difference between V_{IN} and V_{SNS}. A host microcontroller can monitor this output with an A/D converter.

3.5 Cell Voltage Monitor Input (V_{BAT})

Voltage sense input. Connect to positive terminal of battery. Bypass to GND with a minimum of 10 µF to ensure loop stability when the battery is disconnected. A precision internal resistor divider regulates the final voltage on this pin to VREG.

3.6 Drive Output (V_{DRV})

Direct output drive of an external P-channel MOSFET pass transistor for current and voltage regulation.

3.7 Charge Current Sense Input (V_{SNS})

Charge current is sensed via the voltage developed across an external precision sense resistor. The sense resistor must be placed between the supply voltage (V_{IN}) and the source of the external pass transistor. A 50 mΩ sense resistor produces a fast charge current of 1 A, typically.

3.8 Battery Management Input Supply (V_{IN})

A supply voltage of 4.5V to 5.5V is recommended. Bypass to GND with a minimum of 10 µF.

4.0 DEVICE OVERVIEW

The MCP73827 is a linear charge management controller. Refer to the functional block diagram on page 2 and the typical application circuit, Figure 6-1.

4.1 Charge Qualification and Preconditioning

Upon insertion of a battery or application of an external supply, the MCP73827 verifies the state of the $\overline{SHDN}$ pin. The $\overline{SHDN}$ pin must be above the logic High level.

If the $\overline{SHDN}$ pin is above the logic High level, the MCP73827 initiates a charge cycle. The charge status output, MODE, is pulled low throughout throughout the preconditioning and controlled current phases (see Table 5-1 for charge status outputs). If the cell is below the preconditioning threshold, 2.4V typically, the MCP73827 preconditions the cell with a scaled back current. The preconditioning current is set to approximately 43% of the fast charge peak current. The preconditioning safely replenishes deeply depleted cells and minimizes heat dissipation in the external pass transistor during the initial charge cycle.

4.2 Controlled Current Regulation - Fast Charge

Preconditioning ends and fast charging begins when the cell voltage exceeds the preconditioning threshold. Fast charge utilizes a foldback current scheme based on the voltage at the V_{SNS} input developed by the drop across an external sense resistor, R_{SENSE}, and the output voltage, V_{BAT}. Fast charge continues until the cell voltage reaches the regulation voltage, V_{REG}.

4.3 Constant Voltage Regulation

When the cell voltage reaches the regulation voltage, V_{REG}, constant voltage regulation begins. The MCP73827 monitors the cell voltage at the V_{BAT} pin. This input is tied directly to the positive terminal of the battery. The MCP73827 is offered in two fixed-voltage versions for battery packs with either coke or graphite anodes: 4.1V (MCP73827-4.1) and 4.2V (MCP73827-4.2).

4.4 Charge Cycle Completion

The charge cycle can be terminated by a host microcontroller when the output of the charge current monitor, I_{MON}, has diminished below approximately 10% of the peak output voltage level. Alternatively, the transition of the charge status output, MODE, can be used to initialize a timer to terminate the charge. The charge is terminated by pulling the shutdown pin, $\overline{SHDN}$, to a logic Low Level.

5.0 DETAILED DESCRIPTION

Refer to the typical application circuit, Figure 6-1.

5.1 Analog Circuitry

5.1.1 CHARGE CURRENT MONITOR (I_{MON})

The I_{MON} pin provides an output voltage that is proportional to the battery charging current. It is an amplified version of the sense resistor voltage drop that the current loop uses to control the external P-channel pass transistor. This voltage signal can be applied to the input of an A/D Converter and used by a host microcontroller to display information about the state of the battery or charge current profile.

5.1.2 CELL VOLTAGE MONITORED INPUT (V_{BAT})

The MCP73827 monitors the cell voltage at the V_{BAT} pin. This input is tied directly to the positive terminal of the battery. The MCP73827 is offered in two fixed-voltage versions for single cells with either coke or graphite anodes: 4.1V (MCP73827-4.1) and 4.2V (MCP73827-4.2).

5.1.3 GATE DRIVE OUTPUT (V_{DRV})

The MCP73827 controls the gate drive to an external P-channel MOSFET, Q1. The P-channel MOSFET is controlled in the linear region, regulating current and voltage supplied to the cell. The drive output is automatically turned off when the input supply falls below the voltage sensed on the V_{BAT} input.

5.1.4 CURRENT SENSE INPUT (V_{SNS})

Fast charge current regulation is maintained by the voltage drop developed across an external sense resistor, R_{SENSE}, applied to the V_{SNS} input pin. The following formula calculates the value for R_{SENSE}:

$$R_{SENSE} = \frac{V_{CS}}{I_{OUT}}$$

Where:

V_{CS} is the current limit threshold

I_{OUT} is the desired peak fast charge current in amps. The preconditioning current is scaled to approximately 43% of I_{PEAK}.

5.1.5 SUPPLY VOLTAGE (V_{IN})

The V_{IN} input is the input supply to the MCP73827. The MCP73827 automatically enters a power-down mode if the voltage on the V_{IN} input falls below the voltage on the V_{BAT} pin. This feature prevents draining the battery pack when the V_{IN} supply is not present.

5.2 Digital Circuitry

5.2.1 SHUTDOWN INPUT ($\overline{SHDN}$)

The shutdown input pin, $\overline{SHDN}$, can be used to terminate a charge anytime during the charge cycle, initiate a charge cycle, or initiate a recharge cycle.

Applying a logic High input signal to the $\overline{SHDN}$ pin, or tying it to the input source, enables the device. Applying a logic Low input signal disables the device and terminates a charge cycle. In shutdown mode, the device's supply current is reduced to 0.5 µA, typically.

5.2.2 CHARGE STATUS OUTPUT (MODE)

A charge status output, MODE, provides information on the state of charge. The open drain output can be used to illuminate an external LED. Optionally, a pull-up resistor can be used on the output for communication with a microcontroller. Table 5-1 summarizes the state of the charge status output during a charge cycle.

Charge Cycle State	Mode
Qualification	OFF
Preconditioning	ON
Controlled Current Fast Charge	ON
Constant Voltage	OFF
Disabled - Sleep mode	OFF
Battery Disconnected	OFF

TABLE 5-1: *Charge Status Output.*

6.0 APPLICATIONS

The MCP73827 is designed to operate in conjunction with a host microcontroller or in stand-alone applications. The MCP73827 provides the preferred charge algorithm for Lithium-Ion cells, controlled current followed by constant voltage. Figure 6-1 depicts a typical stand-alone application circuit and Figure 6-2 depicts the accompanying charge profile.

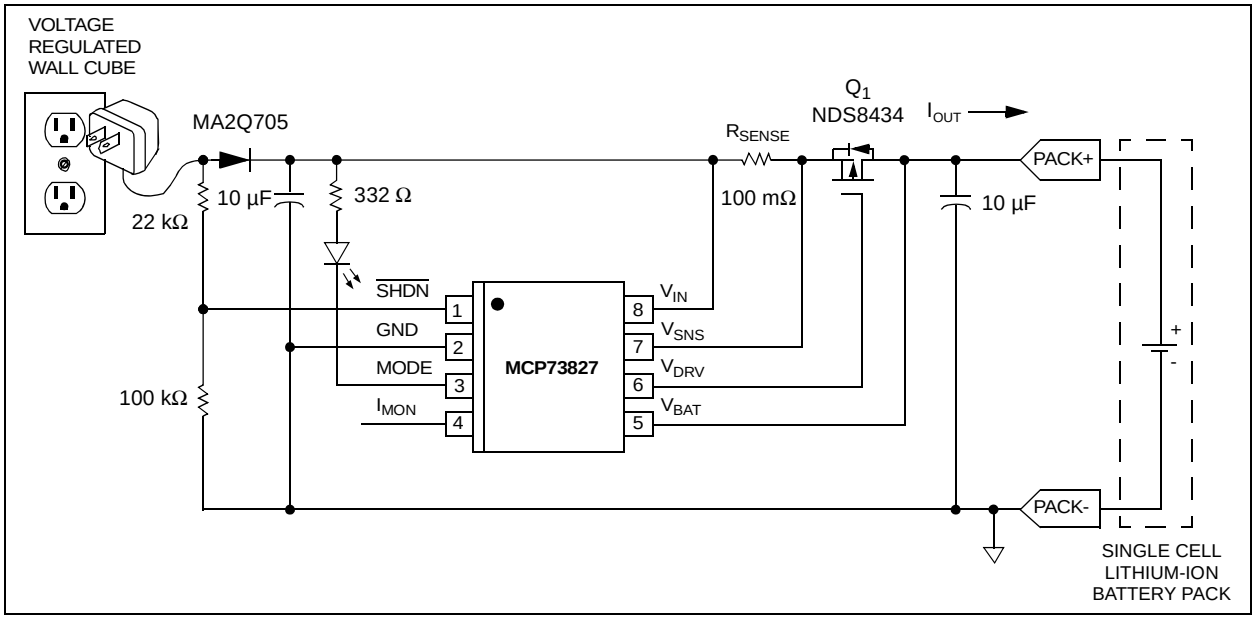


FIGURE 6-1: *Typical Application Circuit.*

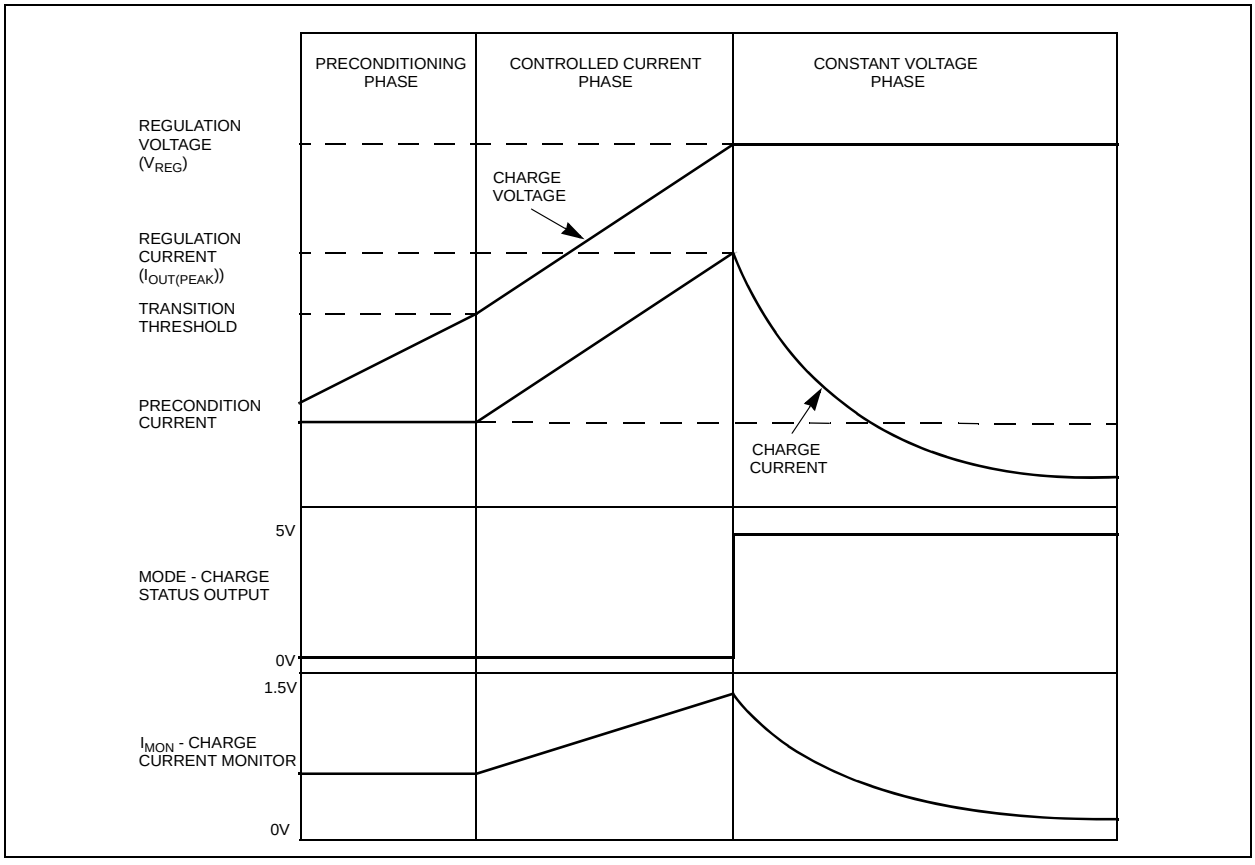


FIGURE 6-2: *Typical Charge Profile.*

6.1 Application Circuit Design

Due to the low efficiency of linear charging, the most important factors are thermal design and cost, which are a direct function of the input voltage, output current and thermal impedance between the external P-channel pass transistor, Q1, and the ambient cooling air. The worst-case situation is when the output is shorted. In this situation, the P-channel pass transistor has to dissipate the maximum power. A trade-off must be made between the charge current, cost and thermal requirements of the charger.

6.1.1 COMPONENT SELECTION

Selection of the external components in Figure 6-1 is crucial to the integrity and reliability of the charging system. The following discussion is intended as a guide for the component selection process.

6.1.1.1 SENSE RESISTOR

The preferred fast charge current for Lithium-Ion cells is at the 1C rate with an absolute maximum current at the 2C rate. For example, a 500 mAH battery pack has a preferred fast charge current of 500 mA. Charging at this rate provides the shortest charge cycle times without degradation to the battery pack performance or life.

The current sense resistor, R_{SENSE}, is calculated by:

$$R_{SENSE} = \frac{V_{CS}}{I_{OUT}}$$

Where:

V_{CS} is the current limit threshold voltage

I_{OUT} is the desired fast charge current

For the 500 mAH battery pack example, a standard value 100 mΩ, 1% resistor provides a typical peak fast charge current of 530 mA and a maximum peak fast charge current of 758 mA. Worst case power dissipation in the sense resistor is:

$$PowerDissipation = 100m\Omega \times 758mA^2 = 57.5mW$$

A Panasonic ERJ-L1WKF100U 100 mΩ, 1%, 1 W resistor is more than sufficient for this application.

A larger value sense resistor will decrease the peak fast charge current and power dissipation in both the sense resistor and external pass transistor, but will increase charge cycle times. Design trade-offs must be considered to minimize space while maintaining the desired performance.

6.1.1.2 EXTERNAL PASS TRANSISTOR

The external P-channel MOSFET is determined by the gate to source threshold voltage, input voltage, output voltage, and peak fast charge current. The selected P-channel MOSFET must satisfy the thermal and electrical design requirements.

Thermal Considerations

The worst case power dissipation in the external pass transistor occurs when the input voltage is at the maximum and the output is shorted. In this case, the power dissipation is:

$$PowerDissipation = V_{INMAX} \times I_{OUT} \times K$$

Where:

V_{INMAX} is the maximum input voltage

I_{OUT} is the maximum peak fast charge current

K is the foldback current scale factor.

Power dissipation with a 5V, +/-10% input voltage source, 100 mΩ, 1% sense resistor, and a scale factor of 0.43 is:

$$PowerDissipation = 5.5V \times 758mA \times 0.43 = 1.8W$$

Utilizing a Fairchild NDS8434 or an International Rectifier IRF7404 mounted on a $1in^2$ pad of 2 oz. copper, the junction temperature rise is 90°C, approximately. This would allow for a maximum operating ambient temperature of 60°C.

By increasing the size of the copper pad, a higher ambient temperature can be realized or a lower value sense resistor could be utilized.

Alternatively, different package options can be utilized for more or less power dissipation. Again, design trade-offs should be considered to minimize size while maintaining the desired performance.

Electrical Considerations

The gate to source threshold voltage and R_{DSON} of the external P-channel MOSFET must be considered in the design phase.

The worst case, V_{GS} provided by the controller occurs when the input voltage is at the minimum and the charge current is at the maximum. The worst case, V_{GS} is:

$$V_{GS} = V_{DRVMAX} - (V_{INMIN} - I_{OUT} \times R_{SENSE})$$

Where:

V_{DRVMAX} is the maximum sink voltage at the V_{DRV} output

V_{INMIN} is the minimum input voltage source

I_{OUT} is the maximum peak fast charge current

R_{SENSE} is the sense resistor

Worst case, V_{GS} with a 5V, +/-10% input voltage source, 100 mΩ, 1% sense resistor, and a maximum sink voltage of 1.6V is:

$$V_{GS} = 1.6V - (4.5V - 758mA \times 99m\Omega) = -2.8V$$

At this worst case V_{GS}, the R_{DSON} of the MOSFET must be low enough as to not impede the performance of the charging system. The maximum allowable R_{DSON} at the worst case V_{GS} is:

$$R_{DSON} = \frac{V_{INMIN} - I_{PEAK} \times R_{SENSE} - V_{BATMAX}}{I_{OUT}}$$

$$R_{DSON} = \frac{4.5V - 758mA \times 99m\Omega - 4.242V}{758mA} = 242m\Omega$$

The Fairchild NDS8434 and International Rectifier IRF7404 both satisfy these requirements.

6.1.1.3 EXTERNAL CAPACITORS

The MCP73827 is stable with or without a battery load. In order to maintain good AC stability in the constant voltage mode, a minimum capacitance of 10 µF is recommended to bypass the V_{BAT} pin to GND. This capacitance provides compensation when there is no battery load. In addition, the battery and interconnections appear inductive at high frequencies. These elements are in the control feedback loop during constant voltage mode. Therefore, the bypass capacitance may be necessary to compensate for the inductive nature of the battery pack.

Virtually any good quality output filter capacitor can be used, independent of the capacitor's minimum ESR (Effective Series Resistance) value. The actual value of the capacitor and its associated ESR depends on the forward trans conductance, g_m, and capacitance of the external pass transistor. A 10 µF tantalum or aluminum electrolytic capacitor at the output is usually sufficient to ensure stability for up to a 1 A output current.

6.1.1.4 REVERSE BLOCKING PROTECTION

The optional reverse blocking protection diode depicted in Figure 6-1 provides protection from a faulted or shorted input or from a reversed polarity input source. Without the protection diode, a faulted or shorted input would discharge the battery pack through the body diode of the external pass transistor.

If a reverse protection diode is incorporated in the design, it should be chosen to handle the peak fast charge current continuously at the maximum ambient temperature. In addition, the reverse leakage current of the diode should be kept as small as possible.

6.1.1.5 SHUTDOWN INTERFACE

In the stand-alone configuration, the shutdown pin is generally tied to the input voltage. The MCP73827 will automatically enter a low power mode when the input voltage is less than the output voltage reducing the battery drain current to 8 µA, typically.

By connecting the shutdown pin as depicted in Figure 6-1, the battery drain current may be further reduced. In this application, the battery drain current becomes a function of the reverse leakage current of the reverse protection diode.

6.1.1.6 CHARGE STATUS INTERFACE

The charge status indicator, MODE, can be utilized to illuminate an LED when the MCP73827 is in the controlled current phase. When the MCP73827 transitions to constant voltage mode, the MODE pin will transition to a high impedance state. A current limit resistor should be used in series with the LED to establish a nominal LED bias current of 10 mA. The maximum allowable sink current of the MODE pin is 30 mA.

6.2 PCB Layout Issues

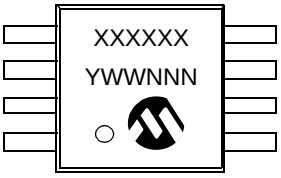
For optimum voltage regulation, place the battery pack as close as possible to the device's V_{BAT} and GND pins. It is recommended to minimize voltage drops along the high current carrying PCB traces.

If the PCB layout is used as a heatsink, adding many vias around the external pass transistor can help conduct more heat to the back-plane of the PCB, thus reducing the maximum junction temperature.

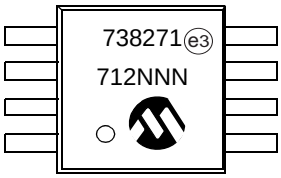
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

8-Lead MSOP



Example:



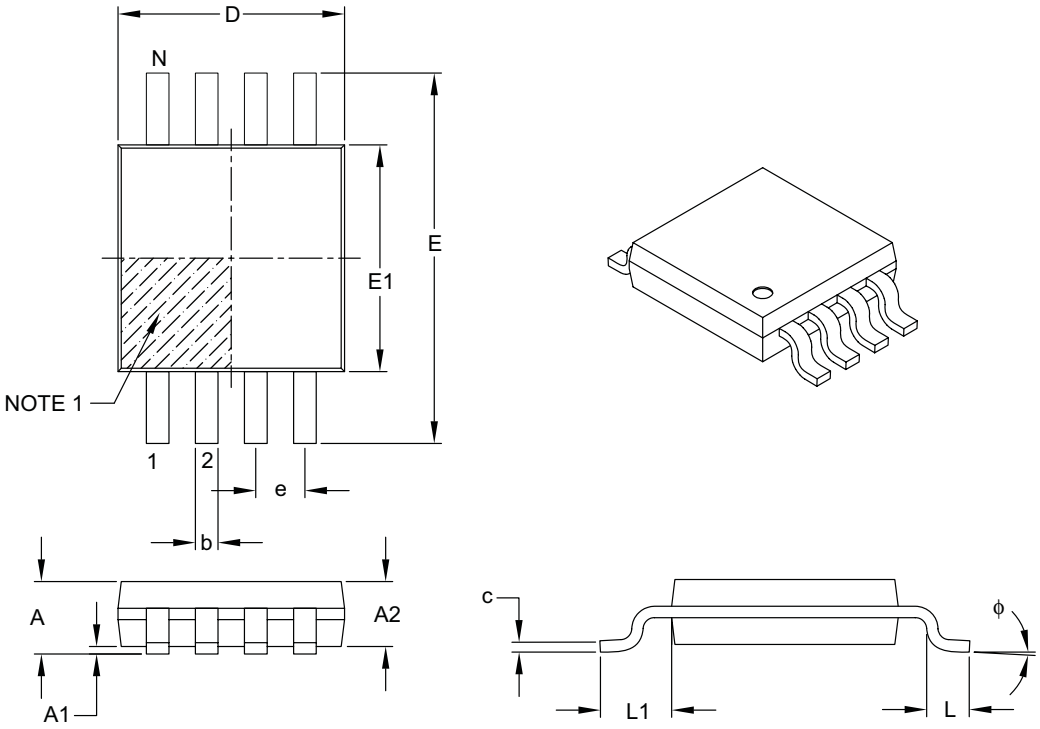
Part Number	Code
MCP73827-4.1VUA	738271
MCP73827-4.2VUA	738272

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (MS or UA) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (February 2007)

This revision includes updates to the packaging diagrams.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X.X	X	XX
Device	Output Voltage	Temperature Range	Package

Device:	MCP73827: Linear Charge Management Controller
Output Voltage:	4.1 = 4.1V 4.2 = 4.2V
Temperature Range:	V = -20°C to +85°C
Package:	UA = Plastic Micro Small Outline (MSOP), 8-lead

Examples:

a) MCP73827-4.1VUA: Linear Charge Management Controller, 4.1V

b) MCP73827-4.2VUA: Linear Charge Management Controller, 4.2V

c) MCP73827-4.2VUATR: Linear Charge Management Controller, 4.2V, in tape and reel

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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