Single Port PHY (Physical Layer) for 25.6, 51.2, and 204.8 Mbps ATM Networks and Backplane Applications

IDT77V126L200

Features

- Performs the PHY-Transmission Convergence (TC) and Physical Media Dependent (PMD) Sublayer functions of the Physical Layer
- Compliant to ATM Forum (af-phy-040.000) and ITU-T I.432.5 specifications for 25.6 Mbps physical interface
- Operates at 25.6, 51.2, 102.4, 204.8 Mbps data rates
- Backwards Compatible with 77V106L25
- 8-bit UTOPIA Level 1 Interface
- 3-Cell Transmit & Receive FIFOs
- Receiver Auto-Synchronization and Good Signal Indication
- LED Interface for status signalling
- Supports UTP Category 3 and 5 physical media
- Interfaces to standard magnetics
- Low-Power CMOS
- 3.3V supply with 5V tolerant inputs
- 64-lead TQFP Package (10 x 10 mm)
- Industrial Temperature Ranges

Description

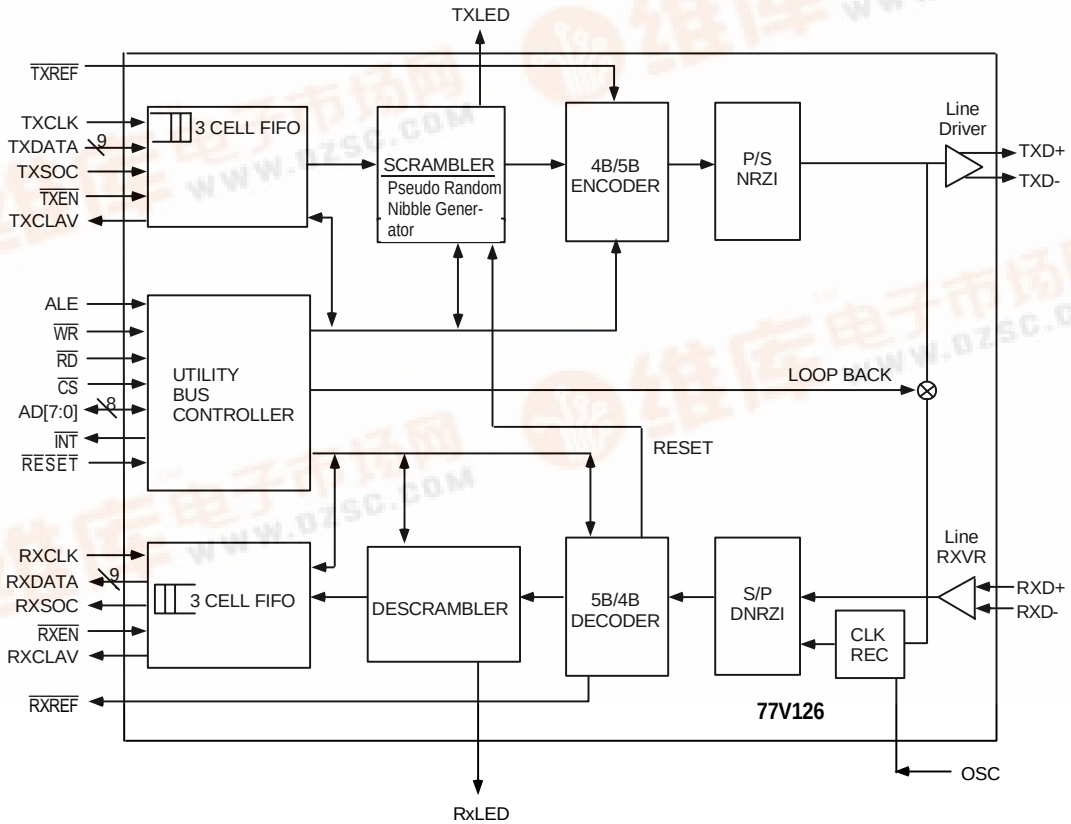
The IDT77V126L200 is a member of IDT's family of products supporting Asynchronous Transfer Mode (ATM) data communications and networking. The IDT77V126L200 implements the physical layer for 25.6 Mbps ATM, connecting a serial copper link (UTP Category 3 and 5) to an ATM layer device such as a SAR or a switch ASIC. The IDT77V126L200 also operates at 51.2 and 204.8 Mbps and is well suited to backplane driving applications. The 77V126L200 utilizes an 8-bit UTOPIA1 interface on the cell side.

The IDT77V126L200 is fabricated using IDT's state-of-the-artCMOS technology, providing the highest levels of integration, performance and reliability, with the low-power consumption characteristics of CMOS.

Applications

- Up to 204.8Mbps backplane transmission
- Rack-to-rack short links
- ATM Switches

Block Diagram



77V126L200 Overview

The 77V126L200 is a physical layer interface chip for up to 200Mbps data rate ATM network communications as defined by ATM Forum document af-phy-040.000 and ITU-T I.432.5. The physical layer is divided into a Physical Media Dependent sub layer (PMD) and Transmission Convergence (TC) sub layer. The PMD sub layer includes the functions for the transmitter, receiver and clock recovery for operation across 100 meters of category 3 and 5 unshielded twisted pair (UTP) cable. This is referred to as the Line Side Interface. The TC sub layer defines the line coding, scrambling, data framing and synchronization.

On the cell side, the 77V126L200 connects to an ATM layer device (such as a switch core or SAR) through an 8-bit Utopia Level 1 interface.

The 77V126L200 is based on the 77105 and maintains significant register compatibility with it, but it also has additional register features.

Access to these status and control registers is through the utility bus. This is an 8-bit muxed address and data bus, controlled by a conventional asynchronous read/write handshake.

Additional pins permit insertion and extraction of an 8kHz timing marker, and provide LED indication of receive and transmit status.

Auto-Synchronization and Good Signal Indication

The 77V126L200 features a new receiver synchronization algorithm that allow it to achieve 4b/5b symbol framing on any valid data stream. This is an improvement on earlier products which could frame only on the escape symbol, which occurs only in start-of-cell or 8kHz (X8) timing marker symbol pairs.

ATM25 transceivers always transmit valid 4b/5b symbols, allowing the 77V126L200 receive section to achieve symbol framing and properly indicate receive signal status, even in the absence of ATM cells or 8kHz (X8) timing markers in the receive data stream. A state machine monitors the received symbols and asserts the “Good Signal” status bit when a valid signal is being received. “Good Signal” is deasserted and the receive FIFO is disabled when the signal is lost. This is sometimes referred to as Loss of Signal (LOS).

Operation at Speeds Greater Than 25 Mbps

In addition to operation at the standard rate of 25.6 Mbps, the 77V126L200 is also specified to operate at 51.2 and 204.8 Mbps. Except for the higher bit rates, all other aspects of operation are identical to the 25.6 Mbps mode.

The rate is determined by the frequency of the clock applied to the OSC input pin. OSC is 32 MHz for the 25.6 Mbps line rate, and 64 MHz for the 51.2 and 204.8 Mbps line rate.

See Figure 16 for recommended line magnetics. Magnetics for 51.2 Mbps operation have a higher bandwidth than magnetics optimized for 25.6 Mbps. For 204.8Mbps data rate applications, ST6200T magnetics from Pulse Engineering can be used. These magnetics have been tested to work over 10 meters of UTP 5 cable at 204.8Mbps. Table 1 shows some of the different data rates the PHY can operate at using a 32MHz or 64MHz oscillator. Note that any oscillator frequency between 32MHz and 64MHz can be used. For example, if a 48MHz oscillator is used and the multiplier is set to 4x, the data rate would be 153.6Mbps.

Reference Clock (OSC)	Clock Multiplier Control Bits **(Enhanced Control 2 Registers)**	Line Bit Rate (MHz)	Data Rate (Mbps)
32 MHz	00 (1x)	32	25.6
	01 (2x)	64	51.2
	10 (4x)	128	102.4
64 MHz	00 (1x)	64	51.2
	01 (2x)	128	102.4
	10 (4x)	256	204.8

Table 1 200 Speed Grade Option

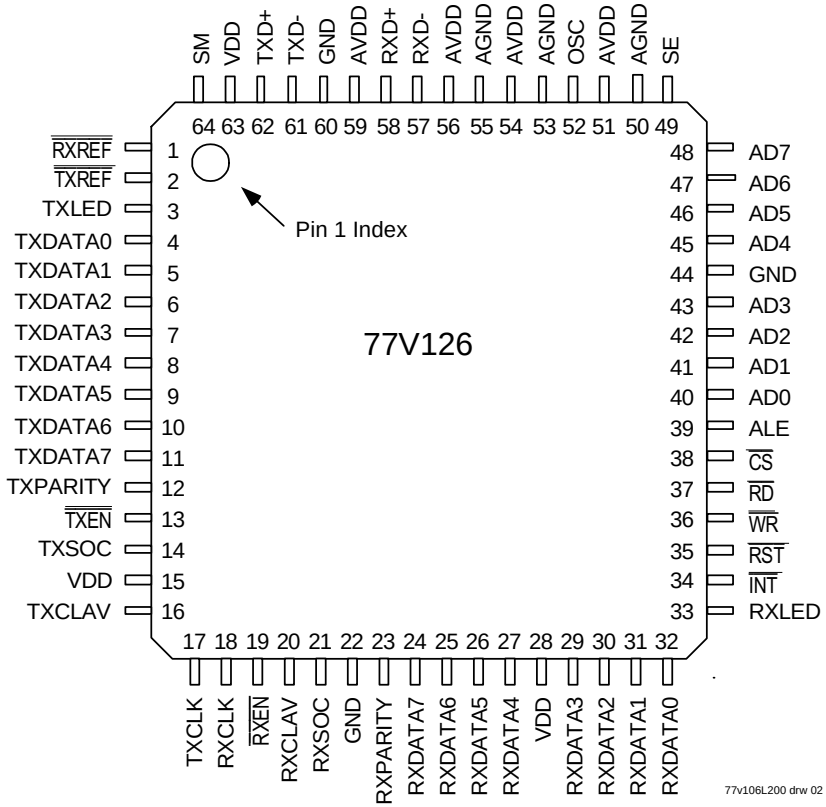


Figure 1 Pin Assignments

Signal Descriptions

Line Side Signals			
Signal Name	**Pin Number**	**I/O**	**Signal Description**
RXD+, RXD-	58, 57	In	Positive and negative receive differential input pair.
TXD+, TXD-	62, 61	Out	Positive and negative transmit differential output pair.
Utility Bus Signals			
Signal Name	**Pin Number**	**I/O**	**Signal Description**
AD[7:0]	48, 47, 46, 45, 43, 42, 41, 40	In/ Out	Utility bus address/data bus. The address input is sampled on the falling edge of ALE. Data is output on this bus when a read is performed. Input data is sampled at the completion of a write operation.
ALE	39	In	Utility bus address latch enable. Asynchronous input. An address on the AD bus is sampled on the falling edge of ALE. ALE must be low when the AD bus is being used for data.
$\overline{CS}$	38	In	Utility bus asynchronous chip select. $\overline{CS}$ must be asserted to read or write an internal register. It may remain asserted at all times if desired.
$\overline{RD}$	37	In	Utility bus read enable. Active low asynchronous input. After latching an address, a read is performed by deasserting $\overline{WR}$ and asserting $\overline{RD}$ and $\overline{CS}$.
$\overline{WR}$	36	In	Utility bus write enable. Active low asynchronous input. After latching an address, a write is performed by deasserting $\overline{RD}$, placing data on the AD bus, and asserting $\overline{WR}$ and $\overline{CS}$. Data is sampled when $\overline{WR}$ or $\overline{CS}$ is deasserted.
Utopia Bus Signals			
Signal Name	**Pin Number**	**I/O**	**Signal Description**
RXCLAV	20	Out	"Utopia Receive Cell Available. "1" indicates that the receive FIFO contains a complete cell. "0" indicates that it does not.
RXCLK	18	In	Utopia Receive Clock. This is a free running clock input.
RXDATA[7:0]	24, 25, 26, 27, 29, 30, 31, 32	Out	Utopia Receive Data. When one of the four ports is selected, the 77V126L200 transfers received cells to an ATM device across this bus. Also see RXPARITY.
$\overline{RXEN}$	19	In	Utopia Receive Enable. Driven by an ATM device to indicate its ability to receive data across the RXDATA bus.
RXPARITY	23	Out	Utopia Receive Data Parity. Odd parity over RXDATA[7:0].
RXSOC	21	Out	Utopia Receive Start of Cell. Asserted coincident with the first word of data for each cell on RXDATA.
TXCLAV	16	Out	"Utopia Transmit Cell Available. "1" indicates that the transmit FIFO has room available for at least one complete cell. "0" indicates that it does not.
TXCLK	17	In	Utopia Transmit Clock. This is a free running clock input.
TXDATA[7:0]	11, 10, 9, 8, 7, 6, 5, 4	In	Utopia Transmit Data. An ATM device transfers cells across this bus to the 77V126L200 for transmission. Also see TXPARITY.
$\overline{TXEN}$	13	In	Utopia Transmit Enable. Driven by an ATM device to indicate it is transmitting data across the TXDATA bus.
TXPARITY	12	In	Utopia Transmit Data Parity. Odd parity across TXDATA[7:0]. Parity is checked and errors are indicated in the Interrupt Status Registers, as enabled in the Master Control Register. No other action is taken in the event of an error. Tie high or low if unused.
TXSOC	14	In	Utopia Transmit Start of Cell. Asserted coincident with the first word of data for each cell on TXDATA.

Table 2 Signal Descriptions (Part 1 of 2)

Miscellaneous Signals			
Signal Name	**Pin Number**	**I/O**	**Signal Description**
$\overline{INT}$	34	Out	Interrupt. $\overline{INT}$ is an open-drain output, driven low to indicate an interrupt. Once low, $\overline{INT}$ remains low until the interrupt status in the appropriate interrupt Status Register is read. Interrupt sources are programmable via the interrupt Mask Registers.
OSC	52	In	TTL line rate clock source, driven by a 100 ppm oscillator. 32 MHz for 25.6 Mbps; 64 MHz for 51.2 Mbps.
$\overline{RST}$	35	In	Reset. Active low asynchronous input resets all control logic, counters and FIFOs. A reset must be performed after power up prior to normal operation of the part.
RXLED	33	Out	Receive LED driver. Driven low for 223 cycles of OSC, beginning with RXSOC when a good (non-null and non-errored) cell is received. Drives 8 mA both high and low.
$\overline{RXREF}$	1	Out	Receive Reference. Active low. $\overline{RXREF}$ pulses low for a programmable number of clock cycles when an X_8 command byte is received.
SE	49	In	Reserved signal. This input must be connected to logic low.
SM	64	In	Reserved signal. This input must be connected to logic low.
TXLED	3	Out	Transmit LED driver. Goes low for 223 cycles of OSC, beginning with TXSOC when a cell is received for transmission. 8 mA drive current both high and low
$\overline{TXREF}$	2	In	Transmit Reference. At the falling edge of $\overline{TXREF}$, an X_8 command byte is inserted into the transmit data stream. Typical application is WAN timing.
Power Supply Signals			
Signal Name	**Pin Number**	**I/O**	**Signal Description**
AGND	50, 53, 55	—	Analog ground. AGND is ground the analog portion of the ship, which sources a more constant current than the digital portion.
AVDO	51, 54, 56, 59	—	Analog power supply. AVDD supplies power to the analog portion of the chip, which draws a more constant current than the digital portion. 3.3 $\pm$ 0.3V
GND	22, 44, 60	—	Digital Ground.
VDD	15, 28, 63	—	Digital power supply. 3.3 $\pm$ 0.3V.

Table 2 Signal Descriptions (Part 2 of 2)

Functional Description

Transmission Convergence (TC) Sub Layer

Introduction

The TC sub layer defines the line coding, scrambling, data framing and synchronization. Under control of a switch interface or Segmentation and Reassembly (SAR) unit, the 25.6Mbps ATM PHY accepts a 53-byte ATM cell, scrambles the data, appends a command byte to the beginning of the cell, and encodes the entire 53 bytes before transmission. These data transformations ensure that the signal is evenly distributed across the frequency spectrum. In addition, the serialized bit stream is NRZI coded. An 8kHz timing sync pulse may be used for isochronous communications.

Data Structure and Framing

Each 53-byte ATM cell is preceded with a command byte. This byte is distinguished by an escape symbol followed by one of 17 encoded symbols. Together, this byte forms one of seventeen possible command bytes. Three command bytes are defined:

1. **X_X** (read: 'escape' symbol followed by another 'escape'): Start-of-cell with scrambler/descrambler reset.
2. **X_4** ('escape' followed by '4'): Start-of-cell without scrambler/descrambler reset.
3. **X_8** ('escape' followed by '8'): 8kHz timing marker. This command byte is generated when the 8kHz sync pulse is detected, and has priority over all line activity (data or command bytes). It is transmitted immediately when the sync pulse is detected. When this occurs during a cell transmission, the data transfer is temporarily interrupted on an octet boundary, and the X_8 command byte is inserted. This condition is the only allowed interrupt in an otherwise contiguous transfer.

Below is an illustration of the cell structure and command byte usage:

{X_X} {53-byte ATM cell} {X_4} {53-byte ATM {X_8} cell}...

In the above example, the first ATM cell is preceded by the X_X start-of-cell command byte which resets both the transmitter-scrambler and receiver-descrambler pseudo-random nibble generators (PRNG) to their initial states. The following cell illustrates the insertion of a start-of-cell command without scrambler/descrambler reset. During this cell's transmission, an 8kHz timing sync pulse triggers insertion of the X_8 8kHz timing marker command byte.

Transmission Description

Refer to Figure 2. Cell transmission begins with the PHY-ATM Interface. An ATM layer device transfers a cell into the 77V126L200 across the Utopia transmit bus. This cell enters a 3-cell deep transmit FIFO. Once a complete cell is in the FIFO, transmission begins by passing the cell, four bits (MSB first) at a time to the 'Scrambler'.

The ‘Scrambler’ takes each nibble of data and exclusive-ORs them against the 4 high order bits (X(t), X(t-1), X(t-3)) of a 10 bit pseudo-random nibble generator (PRING). Its function is to provide the appropriate frequency distribution for the signal across the line.

The PRNG is clocked every time a nibble is processed, regardless of whether the processed nibble is part of a data or command byte. Note however that only data nibbles are scrambled. The entire command byte (X _C) is NOT scrambled before it's encoded (see diagram for illustration).

The PRNG is based upon the following polynomial:

$X^{10} + X^7 + 1$

With this polynomial, the four output data bits (D3, D2, D1, D0) will be generated from the following equations:

D3 = d3 xor X(t-3)
D2 = d2 xor X(t-2)
D1 = d1 xor X(t-1)
D0 = d0 xor X(t)

The following nibble is scrambled with X(t+4), X(t+3), X(t+2), and X(t+1).

A scrambler lock between the transmitter and receiver occurs each time an X_X command is sent. An X_X command is initiated only at the beginning of a cell transfer after the PRNG has cycled through all of its states (2^{10} - 1 = 1023 states). The first valid ATM data cell transmitted after power on will also be accompanied with an X_X command byte. Each time an X_X command byte is sent, the first nibble after the last escape (X) nibble is XOR'd with 1111b (PRNG = 3FFx).

Because a timing marker command (X_8) may occur at any time, the possibility of a reset PRNG start-of-cell command and a timing marker command occurring consecutively does exist (e.g. X_X_X_8). In this case, the detection of the last two consecutive escape (X) nibbles will cause the PRNG to reset to its initial 3FFx state. Therefore, the PRNG is clocked only after the first nibble of the second consecutive escape pair.

Once the data nibbles have been scrambled using the PRNG, the nibbles are further encoded using a 4b/5b process. The 4b/5b scheme ensures that an appropriate number of signal transitions occur on the line. A total of seventeen 5-bit symbols are used to represent the sixteen 4-bit data nibbles and the one escape (X) nibble. The table below lists the 4-bit data with their corresponding 5-bit symbols:

Data	Symbol
0000	10101
0100	00111
1000	10010
1100	10111

Data	Symbol
0001	01001
0101	01101
1001	11001
1101	11101

Data	Symbol
0010	01010
0110	01110
1010	11010
1110	11110

Data	Symbol
0011	01011
0111	01111
1011	11011
1111	11111

ESC(X) = 00010

3505 drw 05a

Transmit Block Diagram

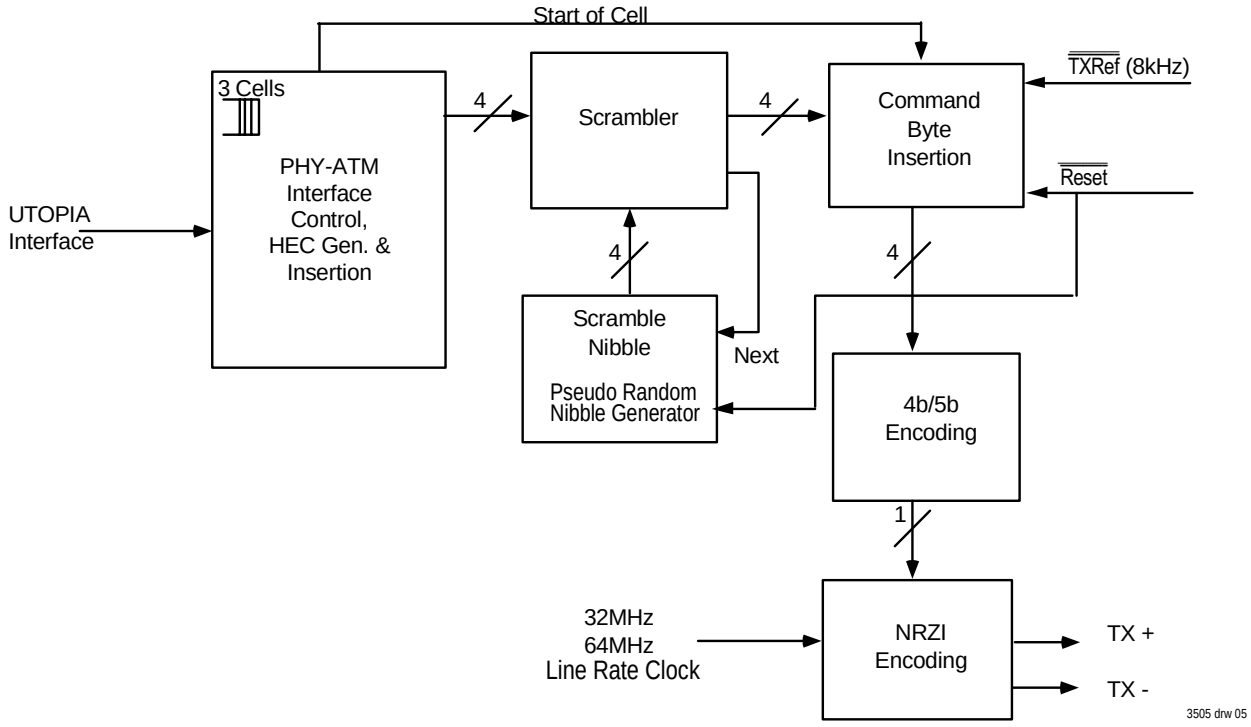


Figure 2 TC Transmit Block Diagram

This encode/decode implementation has several very desirable properties. Among them is the fact that the output data bits can be represented by a set of relatively simple symbols;

- Run length is limited to <= 5;
- Disparity never exceeds +/- 1.

On the receiver, the decoder determines from the received symbols whether a timing marker command (X_8) or a start-of-cell command was sent (X_X or X_4). If a start-of-cell command is detected, the next 53 bytes received are decoded and forwarded to the descrambler. (See the TC Receive Block Diagram).

The output of the 4b/5b encoder provides serial data to the NRZI encoder. The NRZI code transitions the wire voltage each time a '1' bit is sent. This, together with the previous encoding schemes guarantees that long run lengths of either '0' or '1's are prevented. Each symbol is shifted out with its most significant bit sent first.

When no cells are available to transmit, the 77V126L200 keeps the line active by continuing to transmit valid symbols. But it does not transmit another start-of-cell command until it has another cell for transmission. The 77V126L200 never generates idle cells.

Transmit HEC Byte Calculation/Insertion

Byte #5 of each ATM cell, the HEC (Header Error Control) is calculated automatically across the first 4 bytes of the cell header, depending upon the setting of bit 5 of the LED Driver and HEC Status/Control Register (0x03). This byte is then either inserted as a replacement of the fifth byte transferred to the PHY by the external system, or the cell is transmitted as received. A third operating mode provides for insertion of "Bad" HEC codes which may aid in communication diagnostics. These modes are controlled by the LED Driver and HEC Status/Control Registers.

Receiver Description

The receiver side of the TC sublayer operates like the transmitter, but in reverse. The data is NRZI decoded before each symbol is reassembled. The symbols are then sent to the 5b/4b decoder, followed by the Command Byte Interpreter, De-Scrambler, and finally through a FIFO to the UTOPIA interface to an ATM Layer device.

ATM Cell Format

Bit 7 Bit 0
Header Byte 1
Header Byte 2
Header Byte 3
Header Byte 4
UDF
Payload Byte 1
• • •
Payload Byte 48

Note that although the IDT77V126L200 can detect symbol and HEC errors, it does not attempt to correct them.

Good Signal Bit

Upon resetting the device or re-establishing a serial link, logic in front of the 4b/5b decoder uses feedback from the 4b/5b decoder to determine if it is not properly "framed" on the 5-bit symbols being received. If not properly framed, it will shift its framing, one bit at a time, until it achieves proper symbol framing. Receipt of an Escape (X) symbol will also force proper symbol framing.

The IDT77V126L200 monitors line conditions and can provide an interrupt if the line is deemed 'bad'. The Interrupt Status Register contains a Good Signal Bit (bit 6, set to 0 = Bad signal initially) which shows the status of the line per the following algorithm:

To declare 'Good Signal' (from "Bad" to "Good")

There is an up-down counter that counts from 7 to 0 and is initially set to 7. When the clock ticks for 1,024 cycles (32MHz clock, 1,024 cycles = 204.8 symbols) and no "bad symbol" has been received, the counter decreases by one. However, if at least one "bad symbol" is detected during these 1,024 clocks, the counter is increased by one, to a maximum of 7. The Good Signal Bit is set to 1 when this counter reaches 0. The Good Signal Bit could be set to 1 as quickly as 1,433 symbols (204.8 x 7) if no bad symbols have been received.

To declare 'Bad Signal' (from "Good" to "Bad")

The same up-down counter counts from 0 to 7 (being at 0 to provide a "Good" status). When the clock ticks for 1,024 cycles (32MHz clock, 1,024 cycles = 204.8 symbols) and there is at least one "bad symbol", the counter increases by one. If it detects all "good symbols" and no "bad symbols" in the next time period, the counter decreases by one. The "Bad Signal" is declared when the counter reaches 7. The Good Signal Bit could be set to 0 as quickly as 1,433 symbols (204.8 x 7) if at least one "bad symbol" is detected in each of seven consecutive groups of 204.8 symbols.

8kHz Timing Marker

The 8kHz timing marker, described earlier, is a completely optional feature which is essential for some applications requiring synchronization for voice or video, and unnecessary for other applications. When unused, TXREF should be tied high. Also note that it is not limited to 8kHz, should a different frequency be desired. When looped, a received X_8 command byte causes one to be generated on the transmit side.

A received X_8 command byte causes the 77V126L200 to issue a negative pulse on RXREF.

PHY-ATM Interface

UTOPIA Level 1 is a Physical (PHY) Layer to ATM Layer interface standardized by the ATM Forum. It is used for transferring ATM cells and has separate transmit and receive channels and specific handshaking protocols. It is defined in ATM Forum documents af-phy-0017 and af-phy-0039.

There is a single 8-bit data bus in the transmit (ATM-to-PHY) direction, and a single 8-bit data bus in the receive (PHY-to-ATM) direction. In addition to the data bus, each direction also includes a single optional parity bit and several handshaking signals. Please note that the transmit bus and the receive bus operate completely independently.

Receive Block Diagram

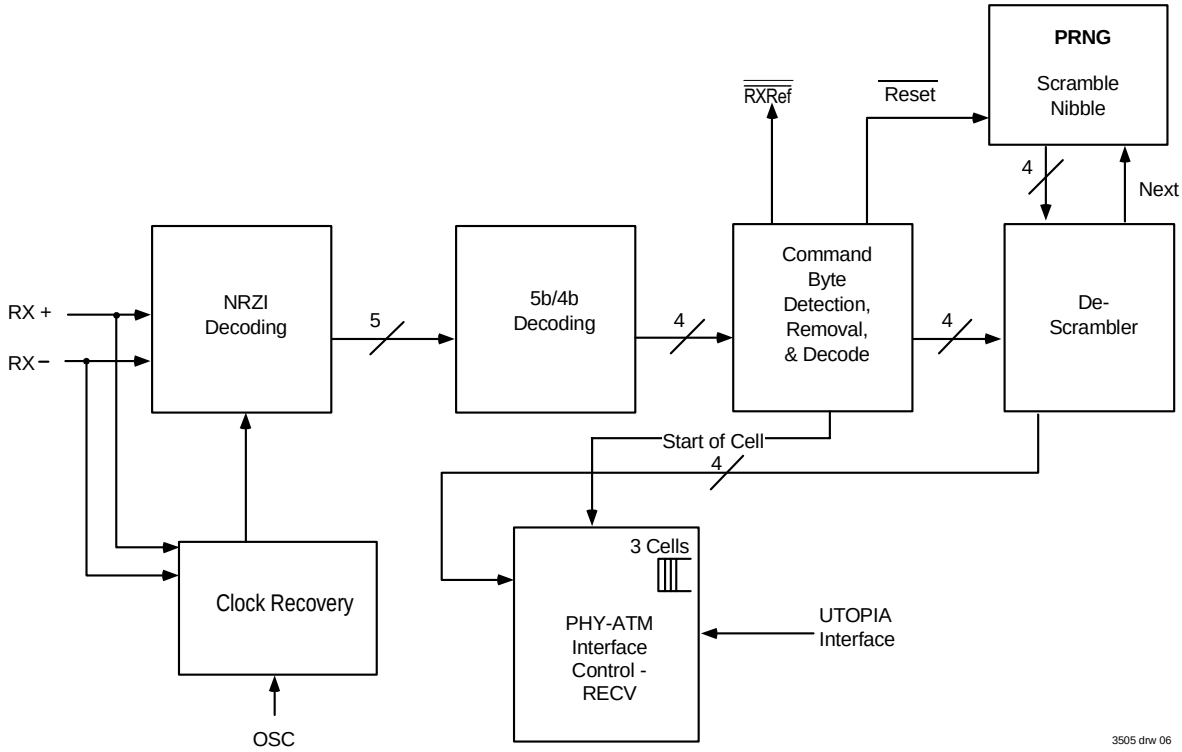


Figure 3 Receive Block Diagram

The Utopia signals are summarized below:

TXDATA[7:0]	ATM to PHY
TXPARITY	ATM to PHY
TXSOC	ATM to PHY
$\overline{\text{TXEN}}$	ATM to PHY
TXCLAV	PHY to ATM
TXCLK	ATM to PHY
RXDATA[7:0]	PHY to ATM
RXPARITY	PHY to ATM
RXSOC	PHY to ATM
$\overline{\text{RXEN}}$	ATM to PHY
RXCLAV	PHY to ATM
RXCLK	ATM to PHY

Transmit and receive both utilize free running clocks, which are inputs to the 77V126. All Utopia signals are timed to these clocks.

In the transmit direction, the PHY first asserts TXCLAV (transmit cell available) to indicate that it has room in its transmit FIFO to accept at least one 53-byte ATM cell. When the ATM layer device is ready to begin passing the cell, it asserts $\overline{\text{TXEN}}$ (transmit enable) and TXSOC (start of cell), coincident with the first byte of the cell on TXDATA. $\overline{\text{TXEN}}$ can remain asserted for the duration of the cell transfer, or the ATM device may deassert $\overline{\text{TXEN}}$ at any time once the cell transfer has begun; data is transferred only when $\overline{\text{TXEN}}$ is asserted.

In the receive direction, $\overline{\text{RXEN}}$ indicates when the ATM device is prepared to receive data. As with transmit, it may be asserted or deasserted at any time.

Note that this Utopia interface can be operated in either cell-mode or in byte-mode as determined by bit 1 in the Master Control Register. In cell-mode, which is the default, the 77V126L200 does not assert TXCLAV until it has enough room in it's transmit FIFO to accept a complete cell, and doesn't assert RXCLAV until it has a complete cell in the receive FIFO. It will not deassert TXCLAV or RXCLAV until at or near the end of the transfer of a cell.

In byte-mode, the phy can assert TXCLAV before it has room for a complete cell. It will modulate TXCLAV to prevent the FIFO from overflowing. Likewise, it may assert RXCLAV before a complete cell has been received, and will modulate RXCLAV to prevent the FIFO from underflowing. There is generally little advantage to the byte-mode, so most users will leave the 77V126L200 in the default cell-mode.

In both transmit and receive, TXSOC and RXSOC (start of cell) is asserted for one clock, coincident with the first byte of each cell. Odd parity is utilized across each 8-bit data field, which means that for an all-zero pattern. the corresponding parity bit is one.

The following figures show examples of the Utopia Level 1 handshake.

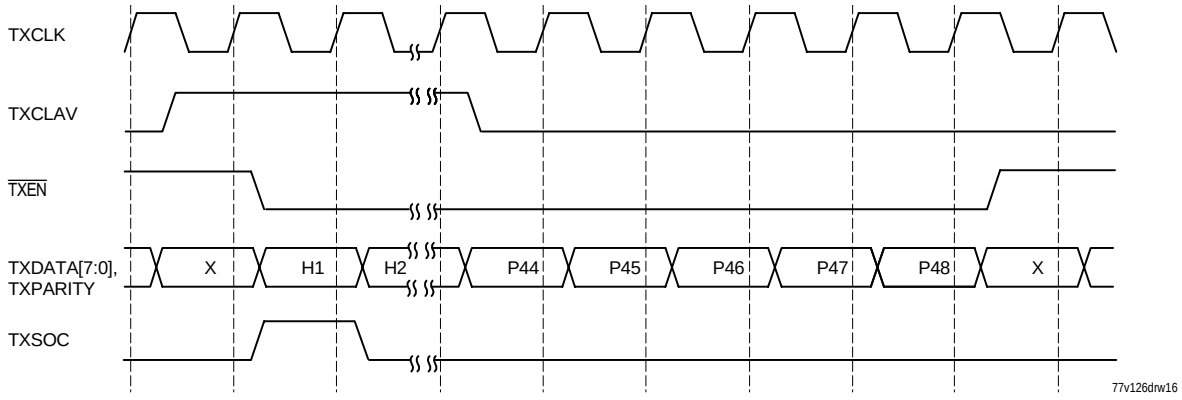


Figure 4 Utopia Transmit Handshake - Single Cell

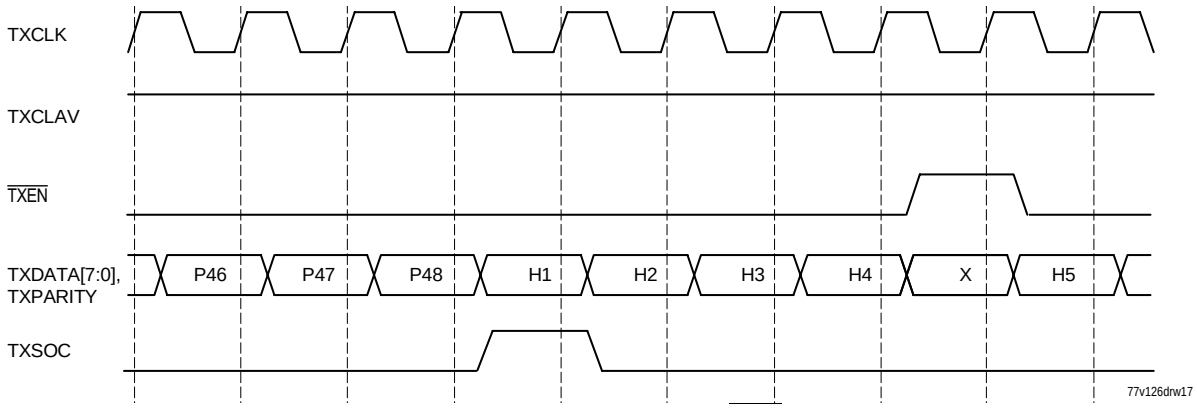


Figure 5 Utopia Transmit Handshake - Back to Back Cells and TXEN Suspended Transmission

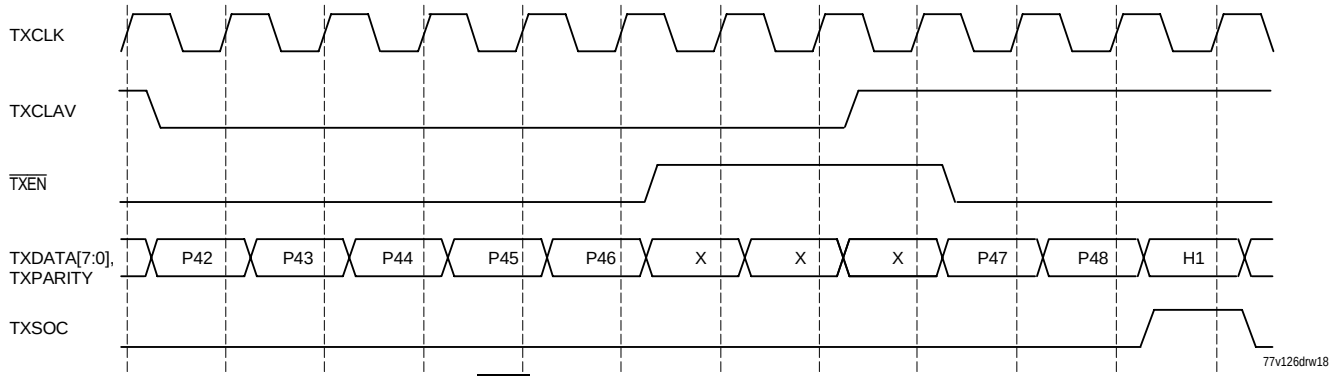


Figure 6 Utopia Transmit Handshake - TXEN Suspended Transmission and Back to Back Cells (Octet Mode Only)

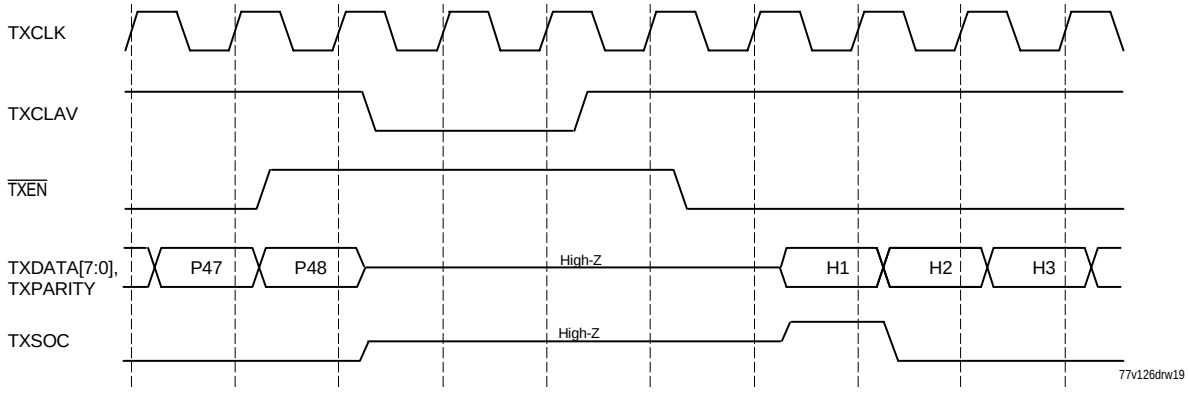


Figure 7 Utopia Transmit Handshake - Delay Between Cells

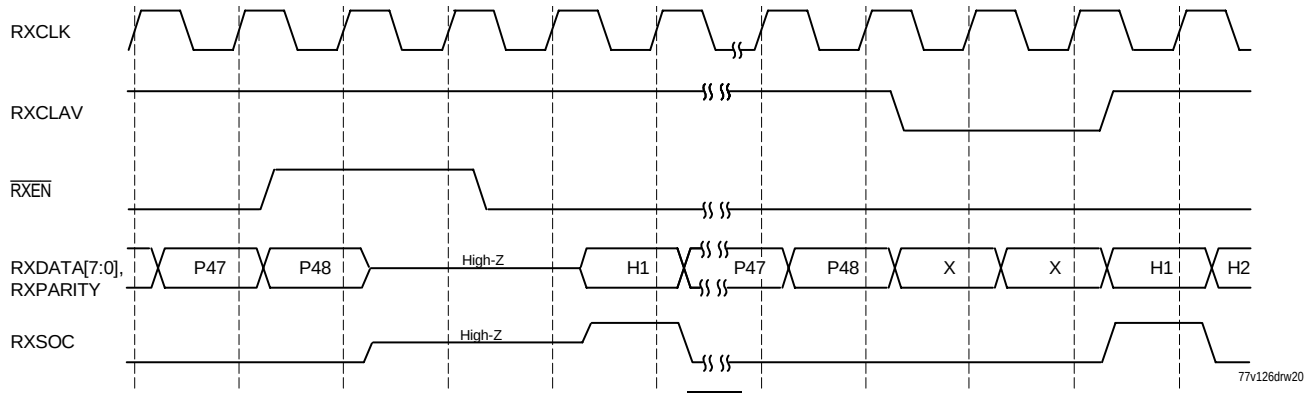


Figure 8 Utopia Receive Handshake - RXEN and RXCLAV Control

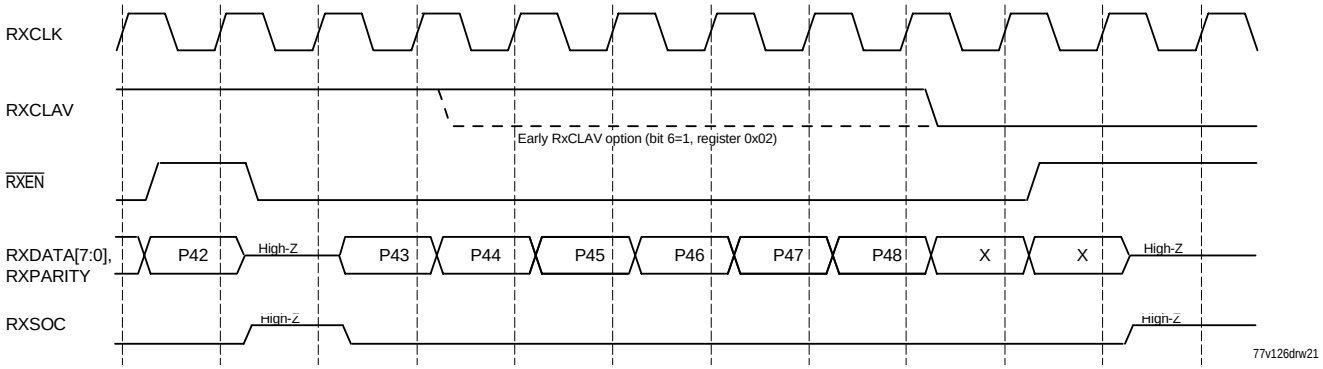


Figure 9 Utopia Receive Handshake - RXCLAV Deassertion

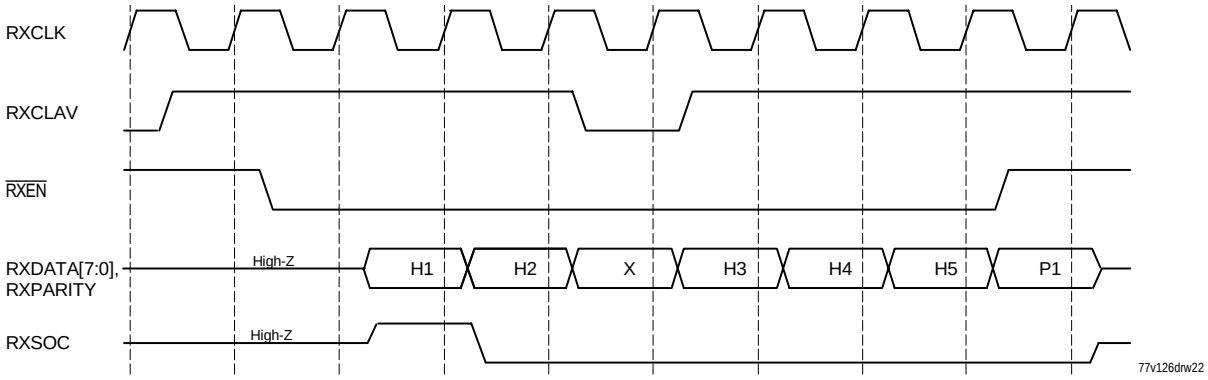


Figure 10 Utopia Receive Handshake - RXCLAV Suspended Transfer (Octet Mode Only)

Control and Status Interface

Utility Bus

The Utility Bus is a byte-wide interface that provides access to the registers within the IDT77V126L200. These registers are used to select desired operating characteristics and functions, and to communicate status to external systems.

The Utility Bus is implemented using a multiplexed address and data bus (AD[7:0]) where the register address is latched via the Address Latch Enable (ALE) signal.

The Utility Bus interface is comprised of the following pins:

AD[7:0], ALE, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$

Read Operation

Refer to the Utility Bus timing waveforms. A register read is performed as follows:

1. Initial condition:
   - *RD, WR, CS not asserted (logic 1)*
   - *ALE not asserted (logic 0)*
2. Set up register address:
   - *place desired register address on AD[7:0]*
   - *set ALE to logic 1;*
   - *latch this address by setting ALE to logic 0.*
3. Read register data:
   - *Remove register address data from AD[7:0]*
   - *assert CS by setting to logic 0;*
   - *assert RD by setting to logic 0*
   - *wait minimum pulse width time (see AC specifications)*

Write Operation

A register write is performed as described below:

1. Initial condition:
   - *RD, WR, CS not asserted (logic 1)*
   - *ALE not asserted (logic 0)*
2. Set up register address:
   - *place desired register address on AD[7:0]*
   - *set ALE to logic 1;*
   - *latch this address by setting ALE to logic 0.*
3. Write data:
   - *place data on AD[7:0]*
   - *assert CS by setting to logic 0;*
   - *assert WR (logic 0) for minimum time (according to timing specification); reset WR or CS to logic 1 to complete register write cycle.*

Interrupt Operations

A variety of selectable interrupt and signalling conditions are provided. They are useful both during 'normal' operation, and as diagnostic aids. Refer to the Status and Control Register List section.

Overall interrupt control is provided via bit 0 of the Master Control Register. When this bit is cleared (set to 0), interrupt signalling is prevented. The Interrupt Mask Register allows individual masking of different interrupt sources. Additional interrupt signal control is provided by bit 5 of the Master Control Register. When this bit is set (=1), receive cell errors will be flagged via interrupt signalling and all other interrupt conditions are masked. These errors include:

- Bad receive HEC
- Short (fewer than 53 bytes) cells
- Received cell symbol error

Normal interrupt operations are performed by setting bit 0 and clearing bit 5 in the Master Control Register. $\overline{INT}$ (pin 34) will go to a low state when an interrupt condition is detected. The external system should then interrogate the 77V126L200 to determine which one (or more) conditions caused this flag, and reset the interrupt for further occurrences. This is accomplished by reading the Interrupt Status Register. Decoding the bits in this byte will tell which error condition caused the interrupt. Reading this register also:

- clears the (sticky) interrupt status bits in the registers that are read
- resets $\overline{INT}$

This leaves the interrupt system ready to signal an alarm for further problems.

LED Control and Signaling

The LED outputs provide bi-directional LED drive capability of 8 mA. As an example, the RxLED outputs are described in the truth table:

State	Pin Voltage
Cells being received	Low
Cells not being received	High

As illustrated in Figure 11, this could be connected to provide for a two-LED condition indicator. These could also be different colors to provide simple status indication at a glance. (The minimum value for R should be 330Ω).

TxLED Truth Table

State	Pin Voltage
Cells being transmitted	Low
Cells not being transmitted	High

Diagnostic Functions

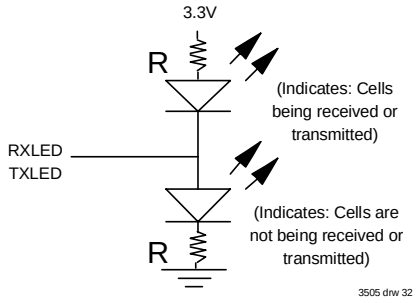


Figure 11 LED Indicator

Loopback

There are two loopback modes supported by the 77V126L200. The loopback mode is controlled via bits 1 and 0 of the Diagnostic Control Register:

Bit 1	Bit 0	Mode
0	0	Normal operating mode
1	0	PHY Loopback
1	1	Line Loopback

Normal Mode

Figure 12 shows normal operating conditions: data to be transmitted is transferred to the TC, where it is queued and formatted for transmission by the PMD. Receive data from the PMD is decoded along with its clock for transfer to the receiving "upstream system".

PHY Loopback

As Figure 13 shows, this loopback mode provides a connection within the PHY from the transmit PHY-ATM interface to the PHY-ATM receive interface. Note that while this mode is operating, no data is forwarded to or received from the line interface.

Line Loopback

Figure 14 might also be called “remote loopback” since it provides for a means to test the overall system, including the line. Since this mode will probably be entered under direction from another system (at a remote location), receive data is also decoded and transferred to the upstream system to allow it to listen for commands. A common example would be a command asking the upstream system to direct the TC to leave this loopback state, and resume normal operations.

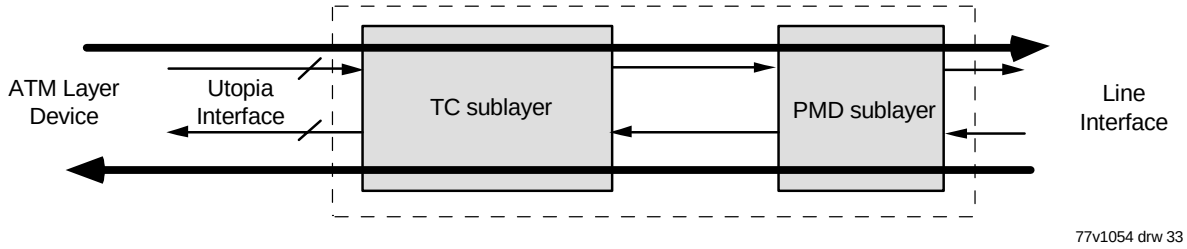


Figure 12 Normal Mode

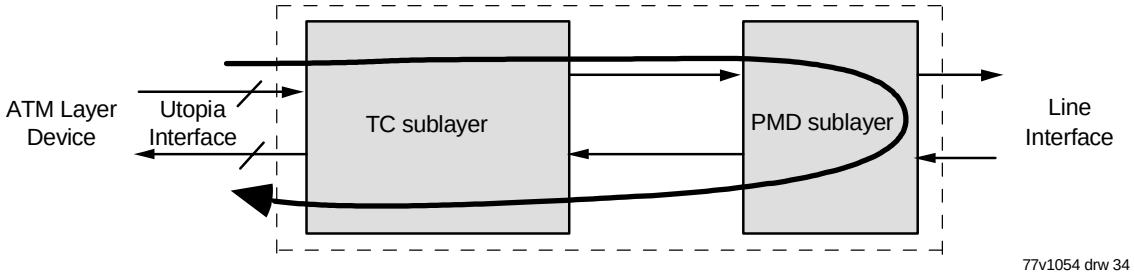


Figure 13 PHY Loopback

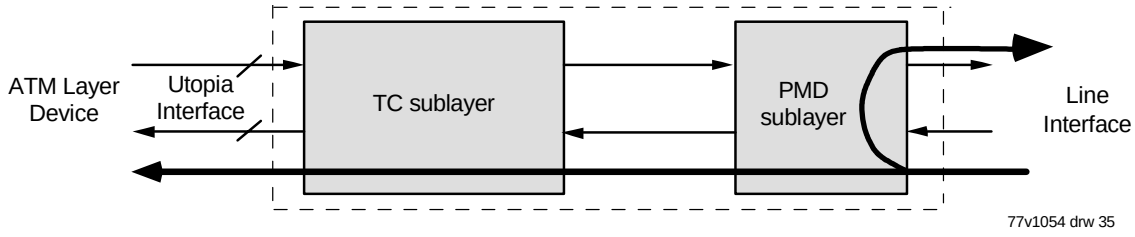


Figure 14 Line Loopback

Counters

Several condition counters are provided to assist external systems (e.g. software drivers) in evaluating communications conditions. It is anticipated that these counters will be polled from time to time (user selectable) to evaluate performance.

- Symbol Error Counters
  - *8 bits*
  - *counts all invalid 5-bit symbols received*
- Transmit Cell Counters
  - *16 bits*
  - *counts all transmitted cells*
- Receive Cell Counters
  - *16 bits*
  - *counts all received cells, excluding idle cells and HEC errored cells*
- Receive HEC Error Counters
  - *5 bits*
  - *counts all HEC errors received*

The TxCell and RxCell counters are sized (16 bits) to provide a full cell count (without roll over) if the counter is read once/second. The Symbol Error counter and HEC Error counter were given sufficient size to indicate exact counts for low error-rate conditions. If these counters overflow, a gross condition is occurring, where additional counter resolution does not provide additional diagnostic benefit.

Reading Counters

1. Decide which counter value is desired. Write to the Counter Select Register to the bit location corresponding to the desired counter. This loads the High and Low Byte Counter Registers with the selected counter's value, and resets this counter to zero.

   Note: Only one counter may be enabled at any time in each of the Counter Select Registers.
2. Read the Counter Registers (low byte and high byte) to get the value.

Further reads may be accomplished in the same manner by writing to the Counter Select Registers.

Note: The PHY takes some time to set up the low and high byte counters after a specific counter has been selected in the Counter Selector register. This time delay (in µS) varies with the line rate and can be calculated as follows:

$$\text{Time delay (µS)} = \frac{12.5}{\text{line rate (Mbps)}}$$

Loop Timing Feature

The 77v126 also offers a loop timing feature for specific applications where data needs to be repeated / transmitted using the recovered clock. If the loop timing mode is enabled in the Enhanced Control Register 1 bit 6, the recovered receive clock is used as to clock out data on transmit side. In normal mode, the transmitter transmits data using the multiplied oscillator clock.

Jitter in Loop Timing Mode

One of the primary concerns when using loop timing mode is the amount of jitter that gets added each time data is transmitted. Table 3 shows the jitter measured at various data rates. The set-up shown in Figure 15 was used to perform these tests. The maximum jitter seen was at TX point 5 and the minimum jitter was at point 2. The loop timing jitter is defined as the amount of jitter generated by each TX node. In other words, the loop timing jitter or the jitter added by a loop-timed port in the set-up below is the difference between the Total Output Jitter and the Total Input Jitter.

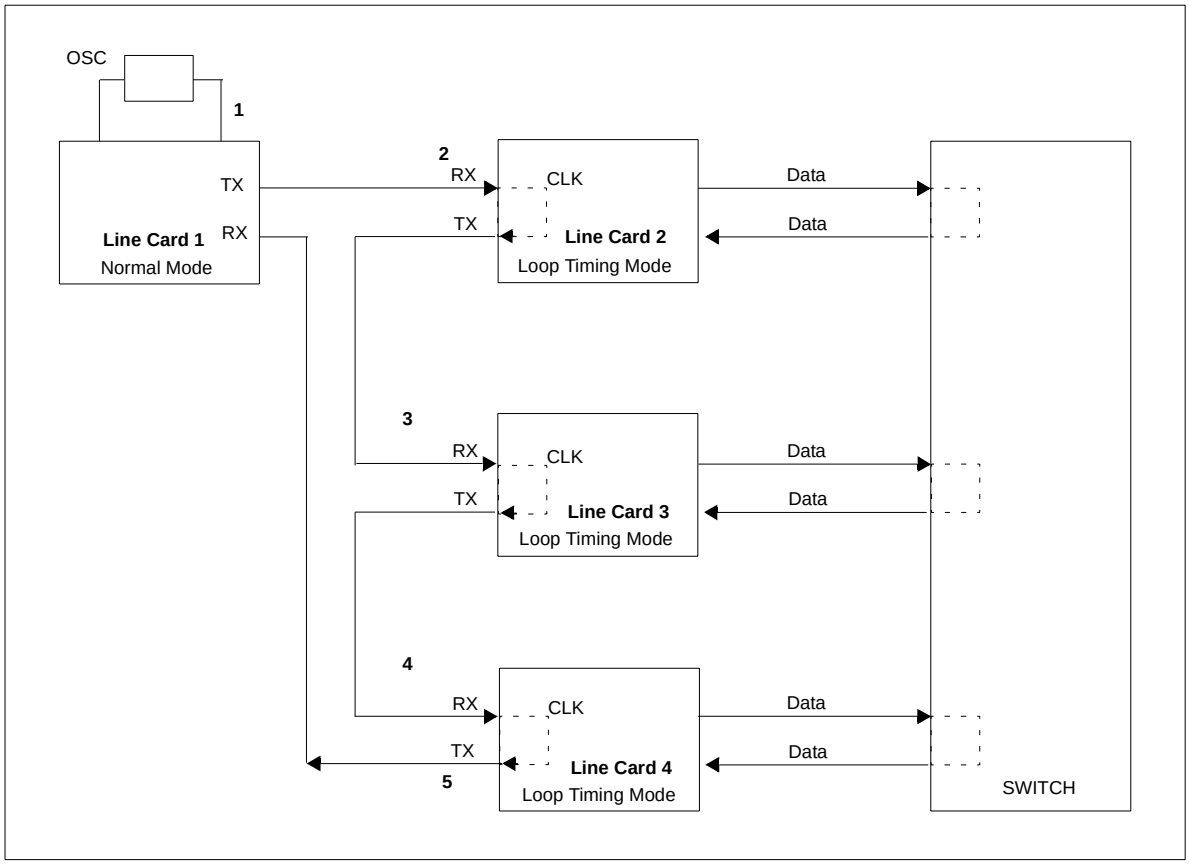


Figure 15 Test Setup for Loop Timing Jitter Measurements

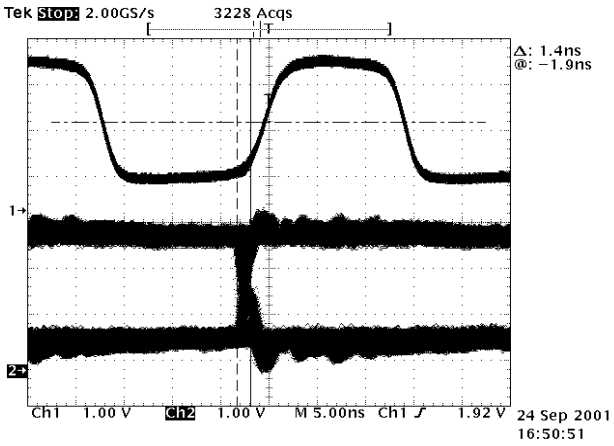
Loop Timing Jitter Specification

Line Rate Mbps	Data Rate Mbps	Min.	Typ.	Max.	Note
32	25.6	--	100 ps	--	Using 32Mhz OSC, multiplier at 1x
64	51.2	--	100 ps	--	Using 64Mhz OSC, multiplier at 1x
128	102.4	--	80 ps	--	Using 32Mhz OSC, multiplier at 4x
256	204.8	--	20 ps	--	Using 64Mhz OSC, multiplier at 4x

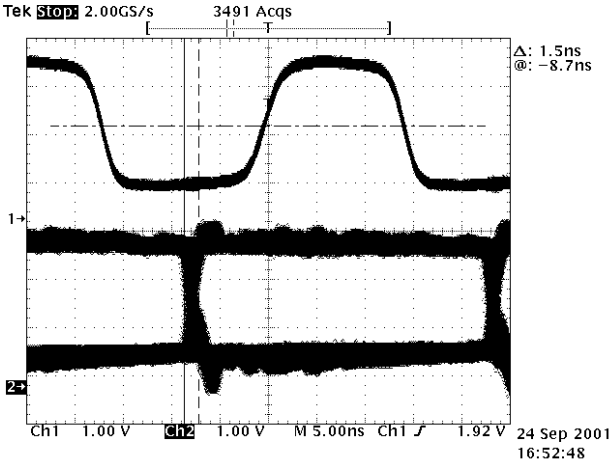
Table 3 Loop Timing Jitter

The waveforms below show some of the measurements taken with the set-up in Figure 15. Using the formula above, the jitter specification was derived. For example, at data rate of 25.6Mbps, jitter added going through Line Card 3 is 1.5ns -1.4ns (as shown in the waveforms below).

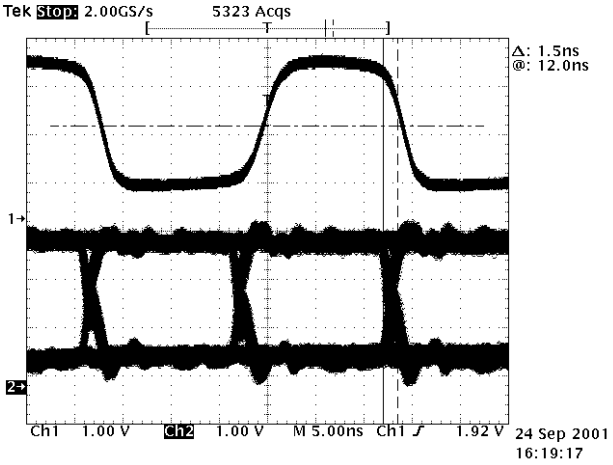
Jitter at 25.6Mbps at point 4 with respect to point 1



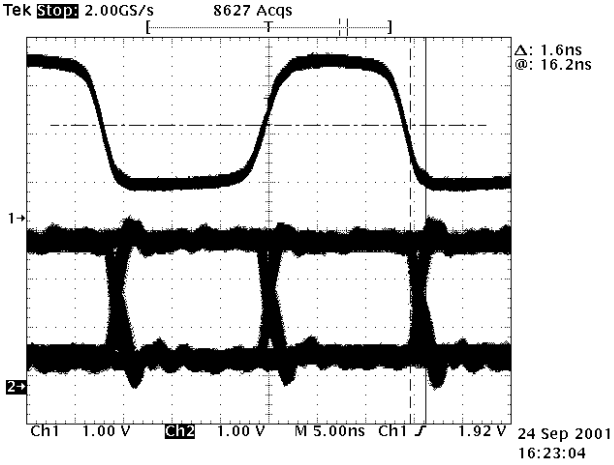
Jitter at 25.6Mbps at point 5 with respect to point 1



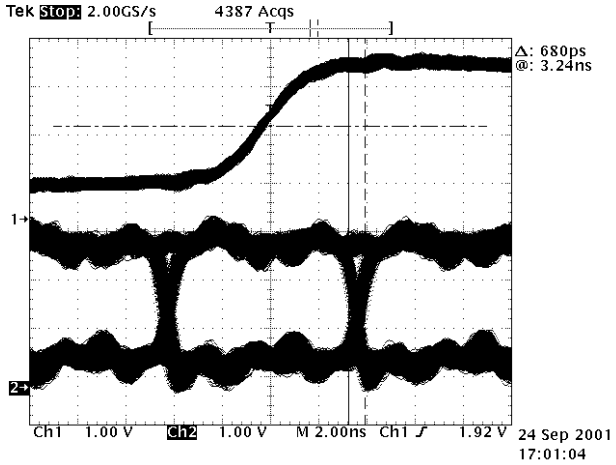
Jitter at 51.2Mbps at point 4 with respect to point 1



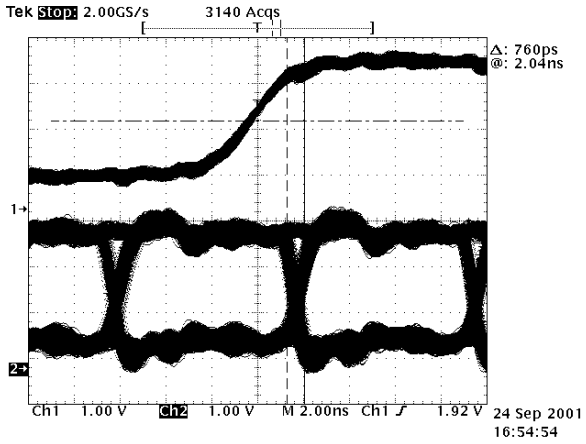
Jitter at 51.2Mbps at point 5 with respect to point 1



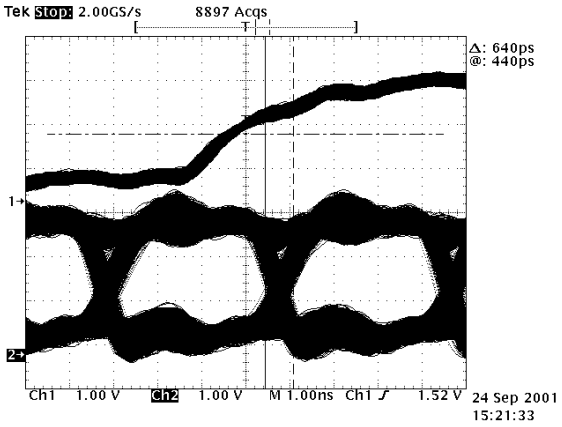
Jitter at 102.4Mbps at point 4 with respect to point 1



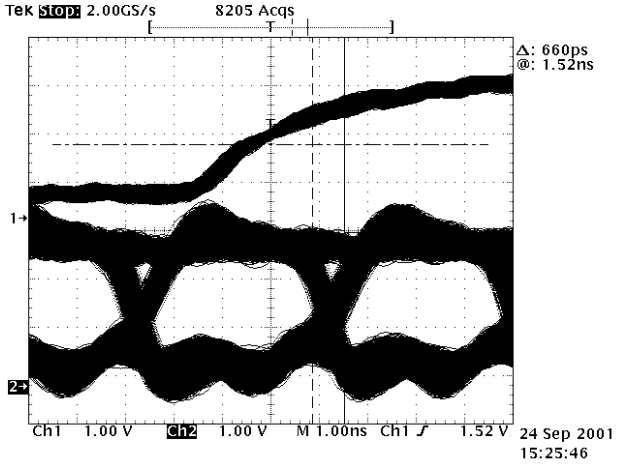
Jitter at 102.4Mbps at point 5 with respect to point 1



Jitter at 256Mbps at point 4 with respect to point 1



Jitter at 256Mbps at point 5 with respect to point 1



From the above measurements taken, the amount of jitter being added at each TX point is not significant. These tests were also run at line rates of 256Mbps for extended periods of time (64 hours) and no bit errors were seen.

Line Side (Serial) Interface

PHY to Magnetics Interface

A standard connection to 100Ω and 120Ω unshielded twisted pair cabling is shown in Figure 16. Note that the transmit signal is somewhat attenuated in order to meet the launch amplitude specified by the standards. The external receive circuitry is designed to attenuate low frequencies in order to compensate for the high frequency attenuation of the cable.

Also, the receive circuitry biases the positive and negative RX inputs to slightly different voltages. This is done so that the receiver does not receive false signals in the absence of a real signal. This can be important because the 77V126L200 does not disable error detection or interrupts when an input signal is not present.

When connecting to UTP at 51.2Mbps and 204.8Mbps, it is necessary to use magnetics with sufficient bandwidth. Refer to Table 5 on page 20 for the recommended magnetics.

PHY to Magnetics Interface

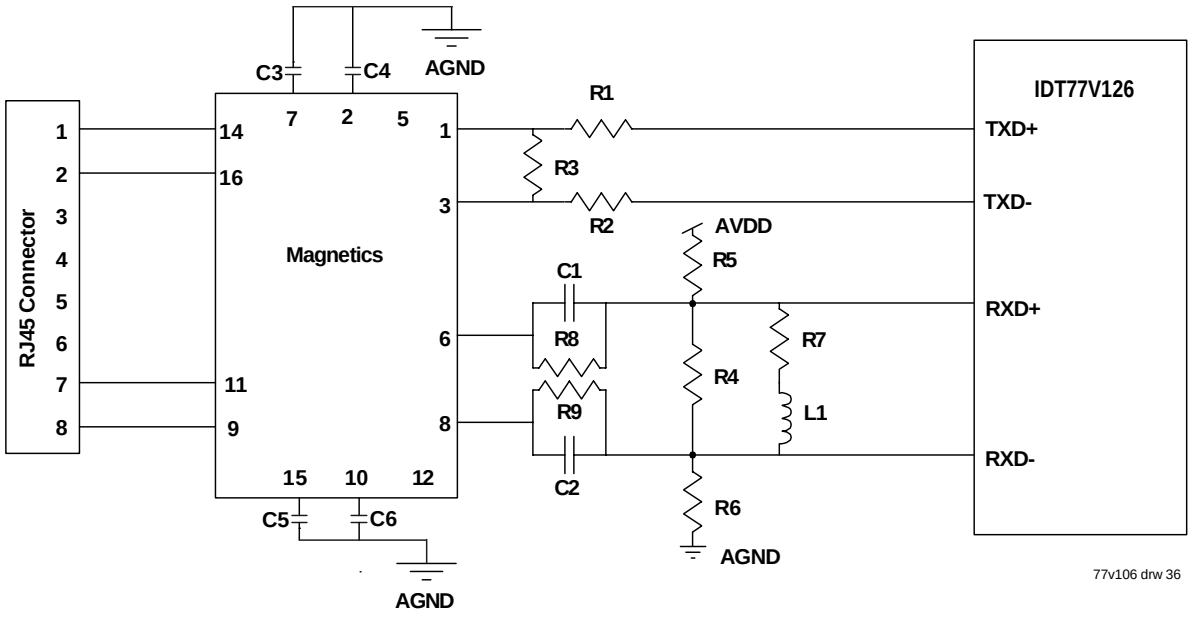


Figure 16 Recommended Connection to Magnetics

Component	Value	Tolerance
R1	47Ω	±5%
R2	47Ω	±5%
R3	620Ω	±5%
R4	110Ω	±5%
R5	2.7kΩ	±5%
R6	2.7kΩ	±5%
R7	82Ω	±5%
R8	33Ω	±5%
R9	33Ω	±5%
C1	0.1µFΩ	±20%
C2	0.1µFΩ	±20%
C3	0.1µFΩ	±20%
C4	0.1µFΩ	±20%
C5	0.1µFΩ	±20%
C6	0.1µFΩ	±20%
L1	3.3µH	±20%

Table 4 Analog Component Values

Magnetics Modules for 25.6 Mbps	
Pulse PE-67583 or R4005	www.pulseeng.com
TDK TLA-6M103	www.component.tdk.com
Magnetics Module for 51.2 Mbps	
Pulse R4005	www.pulseeng.com
Magnetics Module for 204.8 Mbps	
Pulse ST6200T	www.pulseeng.com

Table 5 Magnetics Modules

Status and Control Register List

Master Control Register

Address: 0x00

Bit	Type	Initial State	Function
7	R/W		**Reserved**
6	R/W	1 = discard errored cells	**Discard Receive Error Cells** On receipt of any cell with an error (e.g. short cell, invalid command mnemonic, receive HEC error (if enabled)), this cell will be discarded and will not enter the receive FIFO.
5	R/W	0 = all interrupts	**Enable Cell Error Interrupts Only** If Bit 0 in this register is set (Interrupts Enabled), setting of this bit enables only "Received Cell Error" (as defined in bit 6) to trigger interrupt line."
4	R/W	0 = disabled	**Transmit Data Parity Check** Directs TC to check parity of TxDATA against parity bit located in TXPARITY.
3	R/W	1 = discard idle cells	**Discard Received Idle Cells** Directs TC to discard received idle (VPI/VCI = 0 and GFC = 0) cells from PMD without signalling external systems.
2	R/W	0 = not halted	**Halt Tx** Halts transmission of data from TC to PMD and forces the TxD outputs to the "0" state."
1	R/W	0 = cell mode	**UTOPIA Mode Select:** 0 = cell mode, 1 = byte mode.
0	R/W	1 = enable interrupts	**Enable Interrupt Pin (Interrupt Mask Bit)** Enables the $\overline{INT}$ output pin. If cleared, pin is always high and interrupt is masked. If set, an interrupt will be signaled by setting the interrupt pin to "0". It doesn't affect the Interrupt Status Registers."

Nomenclature
"Reserved" register bits, if written, should always be written "0"
R/W = register may be read and written via the utility bus
R-only or W-only = register is read-only or write-only
sticky = register bit is cleared after the register containing it is read; all sticky bits are read-only
"0" = 'cleared' or 'not set'
"1" = 'set'

Interrupt Status Register

Address: 0x01

Bit	Type	Initial State	Function
7		0	**Reserved**
6	R	0 = Bad Signal	**Good Signal Bit** See definitions earlier in this data sheet. 1 - Good Signal 0 - Bad Signal

5	sticky	0	**HEC error cell received** Set when a HEC error is detected on received cell.
4	sticky	0	**"Short Cell" Received** Interrupt signal which flags received cells with fewer than 53 bytes. This condition is detected when receiving Start-of-Cell command bytes with fewer than 53 bytes between them."
3	sticky	0	**Transmit Parity Error** If Bit 4 of the Master Control Register (Transmit Data Parity Check) is set, this interrupt flags a transmit data parity error condition. Odd parity is used.
2	sticky	0	**Receive Signal Condition change** This interrupt is set when the received 'signal' changes either from 'bad to good' or from 'good to bad'.
1	sticky	0	**Received Symbol Error** Set when an undefined 5-bit symbol is received.
0	sticky	0	**Receive FIFO Overflow** Interrupt which indicates when the receive FIFO has filled and cannot accept additional data.

Diagnostic Control Register

Address: 0x02

Bit	Type	Initial State	Function
7	R/W	0 = normal	**Force TxCLAV Deassert** This feature can be used during line loopback mode to prevent cells from being passed across the Utopia bus for transmission.
6	R/W	0 = UTOPIA	**RxCLAV Operation Select** The UTOPIA standard dictates that during cell mode operation, if the receive FIFO no longer has a complete cell available for transfer from PHY, RxCLAV is deasserted following transfer of the last byte out of the PHY to the upstream system. With this bit set, early deassertion of this signal will occur coincident with the end of Payload byte 44 (as in octet mode for TxCLAV). This provides early indication to the upstream system of this impending condition. 0 = "Standard UTOPIA RxCLAV" 1 = "Cell mode = Byte mode"
5	R/W	1 = tri-state	**Single/Multi-PHY Configuration Select** 0 = single: Never tri-state RxDATA, RxPARITY and RxSOC 1 = Multi-PHY mode: Tri-state RxDATA, RxPARITY and RxSOC when $\overline{\text{RxEN}}$ = 1
4	R/W	0 = normal	**RFLUSH = Clear Receive FIFO** This signal is used to tell the TC to flush (clear) all data in the receive FIFO. The TC signals this completion by clearing this bit.
3	R/W	0 = normal	**Insert Transmit Payload Error** Tells TC to insert cell payload errors in transmitted cells. This can be used to test error detection and recovery systems at destination station, or, under loopback control, at the local receiving station. This payload error is accomplished by flipping bit 0 of the last cell payload byte.
2	R/W	0 = normal	**Insert Transmit HEC Error** Tells TC to insert HEC error in Byte 5 of transmitted cells. This can be used to test error detection and recovery systems in downstream switches, or, under loopback control, the local receiving station. The HEC error is accomplished by flipping bit 0 of the HEC byte.
1, 0	R/W	00 = normal	**Loopback Control** **bit # 1 0** 0 0 Normal mode (receive from network) 1 0 PHY Loopback[1] 1 1 Line Loopback 0 1 PHY Loopback (with clock recovery)

1. When Bits [1:0] in the Diagnostic Control Registers are set to 10, the PHY loopback mode works only if clock multiplier is 1x. For higher multiplies, these bits must be set to 01.

LED Driver and HEC Status/Control Register

Address: 0x03

Bit	Type	Initial State	Function
7	R	0	**Reserved**
6	R/W	0 = enable checking	**Disable Receive HEC Checking (HEC Enable)** When not set, the HEC is calculated on first 4 bytes of received cell, and compared against the 5th byte. When set (= 1), the HEC byte is not checked.
5	R/W	0 = enable calculate & replace	**Disable Transmit HEC Calculate & Replace** When set, the 5th header byte of cells queued for transmit is not replaced with the HEC calculated across the first four bytes of that cell.
4,3	R/W	00 = 1 cycle	**$\overline{\text{RxREF}}$ Pulse Width Select** bit # 4 3 0 0 $\overline{\text{RxREF}}$ active for 1 cycle of the recovered clock 0 1 $\overline{\text{RxREF}}$ active for 2 cycles of the recovered clock 1 0 $\overline{\text{RxREF}}$ active for 4 cycles of the recovered clock 1 1 $\overline{\text{RxREF}}$ active for 8 cycles of the recovered clock
2	R	1 = empty	**Transmit FIFO Status** 1 = TxFIFO empty 0 = TxFIFO not empty
1	R	1	**TxLED Status** 0 = Cell Transmitted 1 = Cell Not Transmitted
0	R	1	**RxLED Status** 0 = Cell Received 1 = Cell Not Received

Low Byte Counter Register [7:0]

Address: 0x04

Bit	Type	Initial State	Function
[7:0]	R	0x00	Provides low-byte of counter value selected via the Counter Select Register.

High Byte Counter Register [15:8]

Address: 0x05

Bit	Type	Initial State	Function
[7:0]	R	0x00	Provides high-byte of counter value selected via the Counter Select Register.

Counter Select Register

Address: 0x06

Bit	Type	Initial State	Function
7	—	0	**Reserved**
6	—	0	**Reserved**
5	—	0	**Reserved**
4	—	0	**Reserved**
3	W	0	**Symbol Error Counter**
2	W	0	**Tx Cell Counter**
1	W	0	**Rx Cell Counter** Does not count HEC errored cells. even when bit 6 of the Master Control Register is Cleared.
0	W	0	**Receive Hec Error Counter**

Note: For proper operation, only one bit may be set in the Counter Selected Register at any time.

Interrupt Mask Register

Address: 0x07

Bit	Type	Initial State	Function
7		0	**Reserved**
6		0	**Reserved**
5	R/W	0 = interrupt enabled	**HEC Error Cell**
4	R/W	0 = interrupt enabled	**Short Cell Error**
3	R/W	0 = interrupt enabled	**Transmit Parity Error**
2	R/W	0 = interrupt enabled	**Receive Signal Condition Change**
1	R/W	0 = interrupt enabled	**Received Cell Symbol Error**
0	R/W	0 = interrupt enabled	**Receive FIFO Overflow**

Note: When set to "1", these bits mask the corresponding interrupt pin ($\overline{INT}$). When set to "0", the interrupts are unmasked. These interrupts correspond to the interrupt status bits in the interrupt Status Registers.

Enhanced Control 1 Register

Address: 0x08

Bit	Type	Initial State	Function
7	W	0 = not reset	**Software Reset** 1 = Reset. This bit is self-clearing; it isn't necessary to write "0" to exit reset.
6	R/W	0 = OSC	**Transmit Line Clock (or Loop Timing Mode)** When set to 0, the OSC input is used as the transmit line clock. When set to 1, the recovered receive clock is used as the transmit line clock.
5-0		0	**Reserved**

Enhanced Control 2 Registers

Addresses: 0x09

Bit	Type	Initial State	Function
7-6	R/W	00	**Line Rate Control** These bits determine the line bit rate relative to the reference clock, as well as the pre-driver strength for the TXD+/- outputs. 00 Clock multiplier = 1x, pre-driver strength is "standard" 01 Clock multiplier = 2x, pre-driver strength is "standard" 10 Clock multiplier = 4x, pre-driver strength is "strong" 11 Reserved
5		0	**Reserved**
4		0	**Reserved**
3		0	**Reserved**
2		0	**Reserved**
1		0	**Reserved**
0		0	**Reserved**

Absolute Maximum Ratings

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +5.5	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +120	°C
I_{OUT}	DC Output Current	50	mA

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Digital Supply Voltage	3.0	3.3	3.6	V
GND	Digital Ground Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	5.25	V
VIL	Input Low Voltage	-0.3	—	0.8	V
AVDO	Analog Supply Voltage	3.0	3.3	3.6	V
AGND	Analog Ground Voltage	0	0	0	V
VDIF	VDD - AVDD	-0.5	0	0.5	V

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND, AGND	VDD, ADD
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

Capacitance (TA = +25°C, F = 1MHz)

Symbol	Parameter	Conditions	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{IO}	I/O Capacitance	V_{OUT} = 0V	10	pF

DC Electrical Characteristics (All Pins except TX+/- and RX+/-)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	Gnd ≤ VIN ≤ VDD	-5	5	µA
I_{LO}	/O (as input) Leakage Current	Gnd ≤ VIN ≤ VDD	-10	10	µA
V_{OH1}[1]	Output Logic "1" Voltage	I_{OH} = -2mA, VDD = min.	2.4	—	V
V_{OH2}[2]	Output Logic "1" Voltage	I_{OH} = -8mA, VDD = min.	2.4	—	V
V_{OL}[3]	Output Logic "0" Voltage	I_{OL} = -8mA, VDD = min.	—	0.4	V
I_{DD1}[4, 5]	Digital Power Supply Current - VDD	OSC = 32 MHz, all outputs unloaded	—	90	mA
		OSC = 64 MHz, all outputs unloaded	—	132	mA
		OSC = 256 MHz, all outputs unloaded	—	146	mA
I_{DD2}[5]	Analog Power Supply Current - AVDD	OSC = 32 MHz, all outputs unloaded	—	17	mA
		OSC = 64 MHz, all outputs unloaded	—	19	mA
		OSC = 256 MHz, all outputs unloaded	—	34	mA

1. For AD[7:0] pins only.
2. For all output pins except AD[7:0], $\overline{INT}$ and TX+/-.
3. For all output pins except TX+/-.
4. Add 15mA for each TX+/- pair that is driving a load.
5. Total supply current is the sum of IDD1 and IDD2

DC Electrical Characteristics (TX+/- Output Pins Only)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output Logic High Voltage	I_{OH} = -20mA	VDD - 0.5V	—	V
V_{OL}	Output Logic Low Voltage	I_{OL} = -20mA	—	0.5	V

DC Electrical Characteristics (RXD+/- Input Pins Only)

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{IR}	RXD+/- input voltage range	0	—	VDD	V
V_{IP}	RXD+/- input peak-to-peak differential voltage	0.6	—	2*VDD	V
V_{ICM}	RXD+/- input common mode voltage	1.0	VDD/2	VDD-0.5	V

Notes: 1. Differential signal amplitude is twice the amplitude of the individual signals which constitute the differential signal.

UTOPIA Level 1 Bus Timing Parameters

Symbol	Parameter	Min.	Max.	Unit
t31	TXCLK Frequency	0.2	50	MHz
t32	TXCLK Duty Cycle (% of t31)	40	60	%
t33	TXDATA[7:0], TXPARITY Setup Time to TXCLK	4	—	ns
t34	TXDATA[7:0], TXPARITY Hold Time to TXCLK	1.5	—	ns
t35	TXSOC, $\overline{\text{TXEN}}$[3:0] Setup Time to TXCLK	4	—	ns
t36	TXSOC, $\overline{\text{TXEN}}$[3:0] Hold Time to TXCLK	1.5	—	ns
t37	TXCLK to TXCLAV[3:0] Invalid (min) and Valid (max)	2	10	ns
t39	RXCLK Frequency	0.2	50	MHz
t40	RXCLK Duty Cycle (% of t39)	40	60	%
t41	$\overline{\text{RXEN}}$[3:0] Setup Time to RXCLK	4	—	ns
t42	$\overline{\text{RXEN}}$[3:0] Hold Time to RXCLK	1.5	—	ns
t43	RXCLK to RXCLAV[3:0] Invalid (min) and Valid (max)	2	10	ns
t44	RXCLK to RXSOC High-Z	2	10	ns
t45	RXCLK to RXSOC Low-Z (min) and Valid (max)	2	10	ns
t46	RXCLK to RXDATA, RXPARITY High-Z	2	10	ns
t47	RXCLK to RXDATA, RXPARITY Low-Z (min) and Valid (max)	2	10	ns

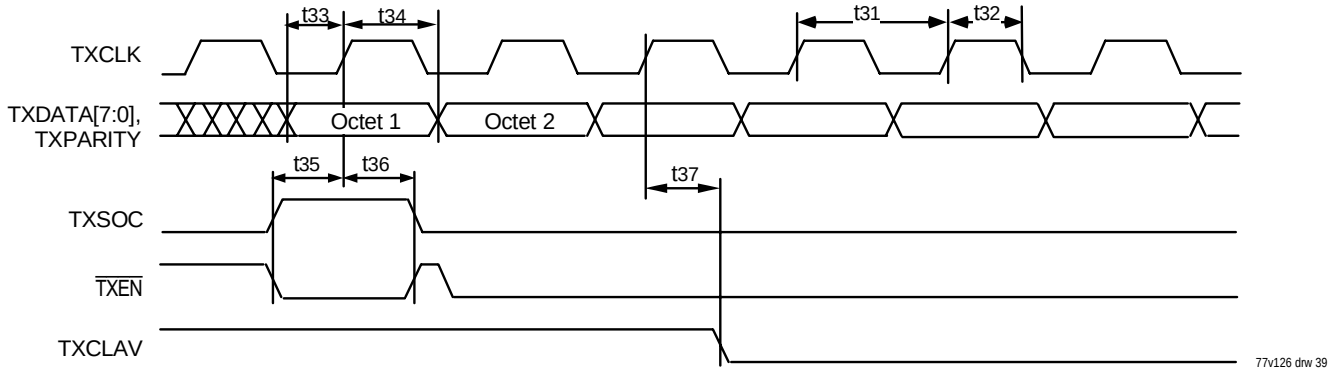


Figure 17 UTOPIA 1 Transmit Timing Waveforms

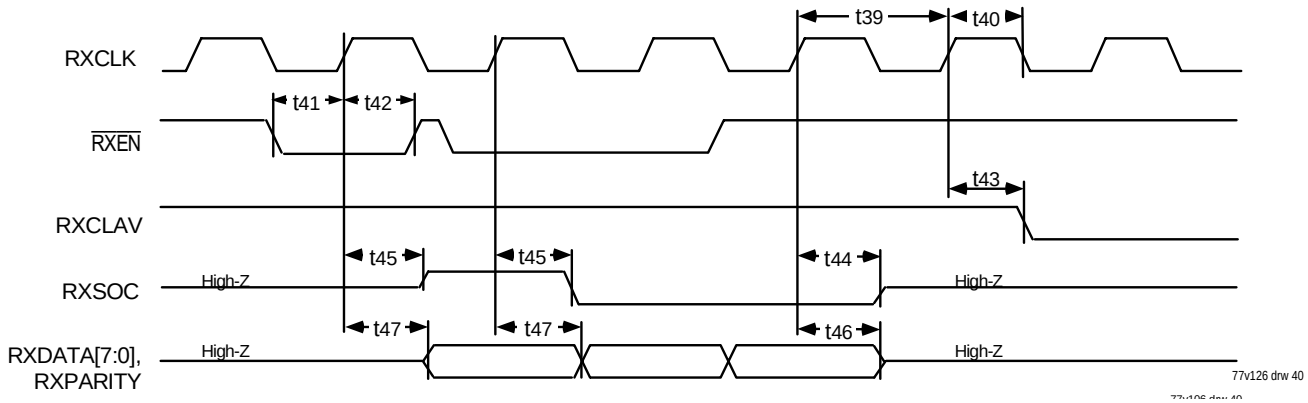


Figure 18 UTOPIA 1 Receive Timing Waveforms

Utility Bus Read Cycle

Name	Min	Max	Unit	Description
Tas	10	—	MHz	Address setup to ALE
Tcsrd	0	—	%	Chip select to read enable
Tah	5	—	ns	Address hold to ALE
Tapw	10	—	ns	ALE min pulse width
Ttria	0	—	ns	Address tri-state to $\overline{RD}$ assert
Trdpw	20	—	ns	Min. $\overline{RD}$ pulse width
Tdh	0	—	ns	Data Valid hold time
Tch	0	—	ns	$\overline{RD}$ deassert to $\overline{CS}$ deassert
Ttrid	—	10	ns	$\overline{RD}$ deassert to data tri-state
Trd	—	18	ns	Read Data access
Tar	5	—	ns	ALE low to start of read
Trdd	0	—	ns	Start of read to Data low-Z

Utility Bus Write Cycle

Name	Min	Max	Unit	Description
Tapw	10	—	ns	ALE min pulse widt
Tas	10	—	ns	Address set up to ALE
Tah	5	—	ns	Address hold time to ALE
Tcswr	0	—	ns	$\overline{CS}$ Assert to $\overline{WR}$
Twrpw	20	—	ns	Min. $\overline{WR}$ pulse width
Tdws	20	—	ns	Write Data set up
Tdwh	10	—	ns	Write Data hold time
Tch	0	—	ns	$\overline{WR}$ deassert to $\overline{CS}$ deassert
Taw	20	—	ns	ALE low to end of write

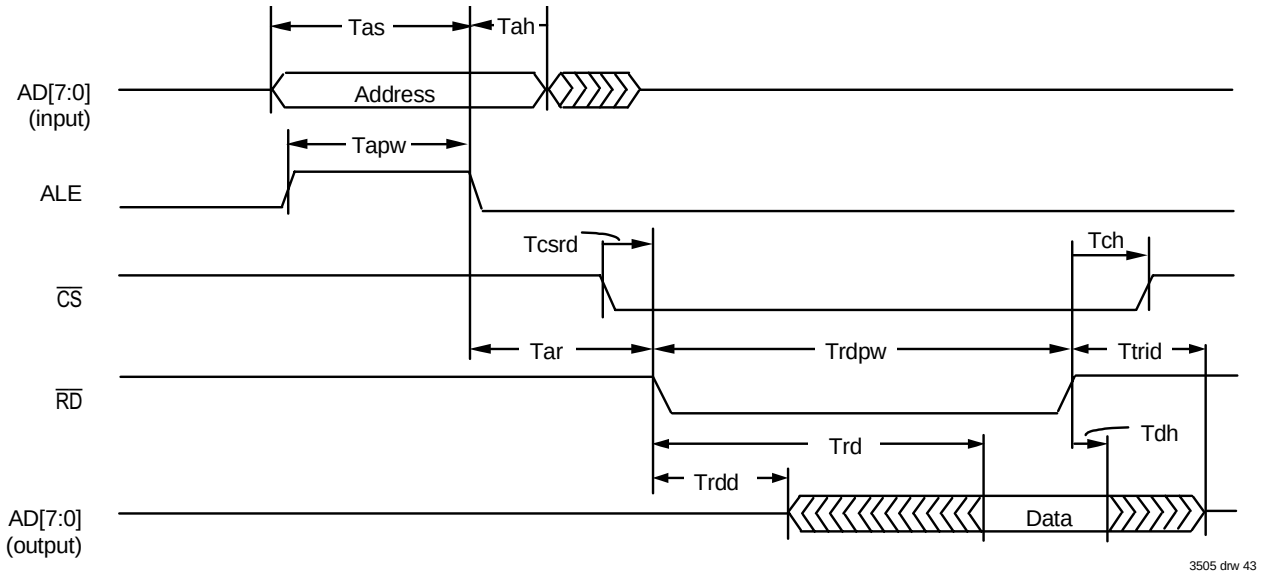


Figure 19 Utility Bus Read Cycle

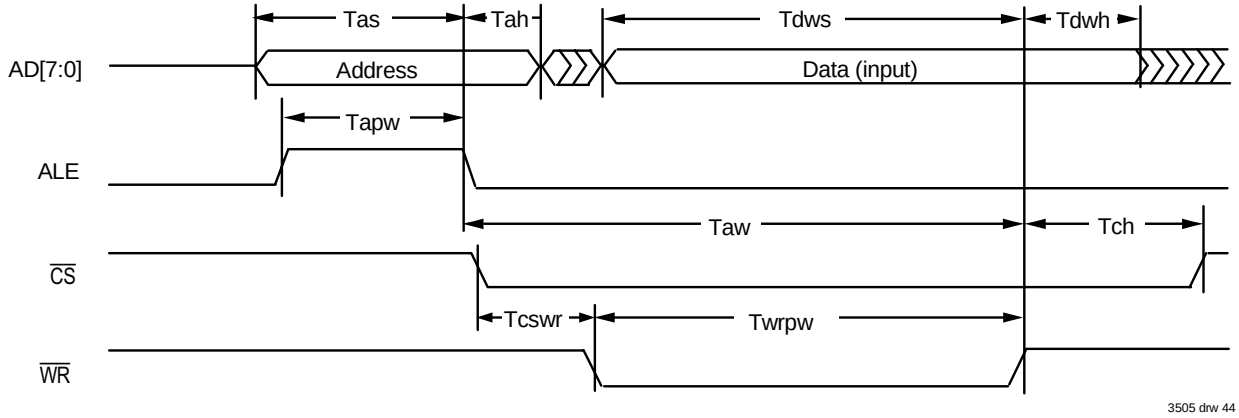


Figure 20 Utility Bus Write Cycle

OSC, $\overline{\text{TXREF}}$ and Reset Timing

Symbol	Parameter	Min	Typ	Max	Unit
Tcyc	OSC cycle period (25.6 Mbps) (51.2 Mbps)	30 15	31.25 15.625	33 16.5	ns ns
Tckh	OSC high time	40	—	60	%
Tckl	OSC low time	40	—	60	%
Tcc	OSC cycle to cycle period variation	—	—	1	%
Ttrh	$\overline{\text{TXREF}}$ High Time	35	—	—	ns
Ttrl	$\overline{\text{TXREF}}$ Low Time	35	—	—	ns
Trspw	Minimum $\overline{\text{RST}}$ Pulse Width	two OSC cycles	—	—	—
Trrpw	$\overline{\text{RXREF}}$ Pulse Width (For default setting in register 0x03 and 25.6 Mbps. Can be programmed for multiples of this amount.)	0.9	1 (31.25ns)	1.1	Receive Data Bit Period

Note: The minimum $\overline{\text{RESET}}$ Pulse Width is either two RxCLK cycles, two TxCLK cycles, or two OSC cycles, whichever is greater (and applicable).

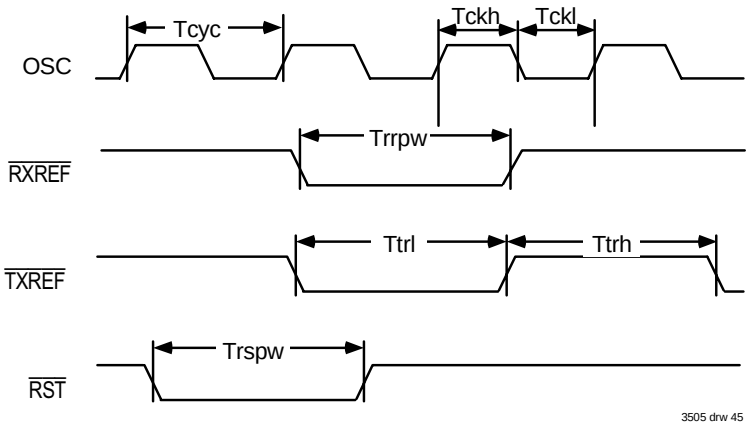
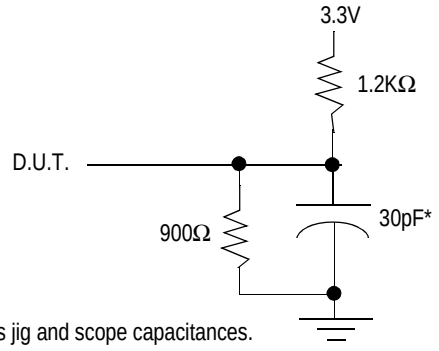


Figure 21 OSC, $\overline{\text{TXREF}}$ and Reset Timing

AC Test Conditions

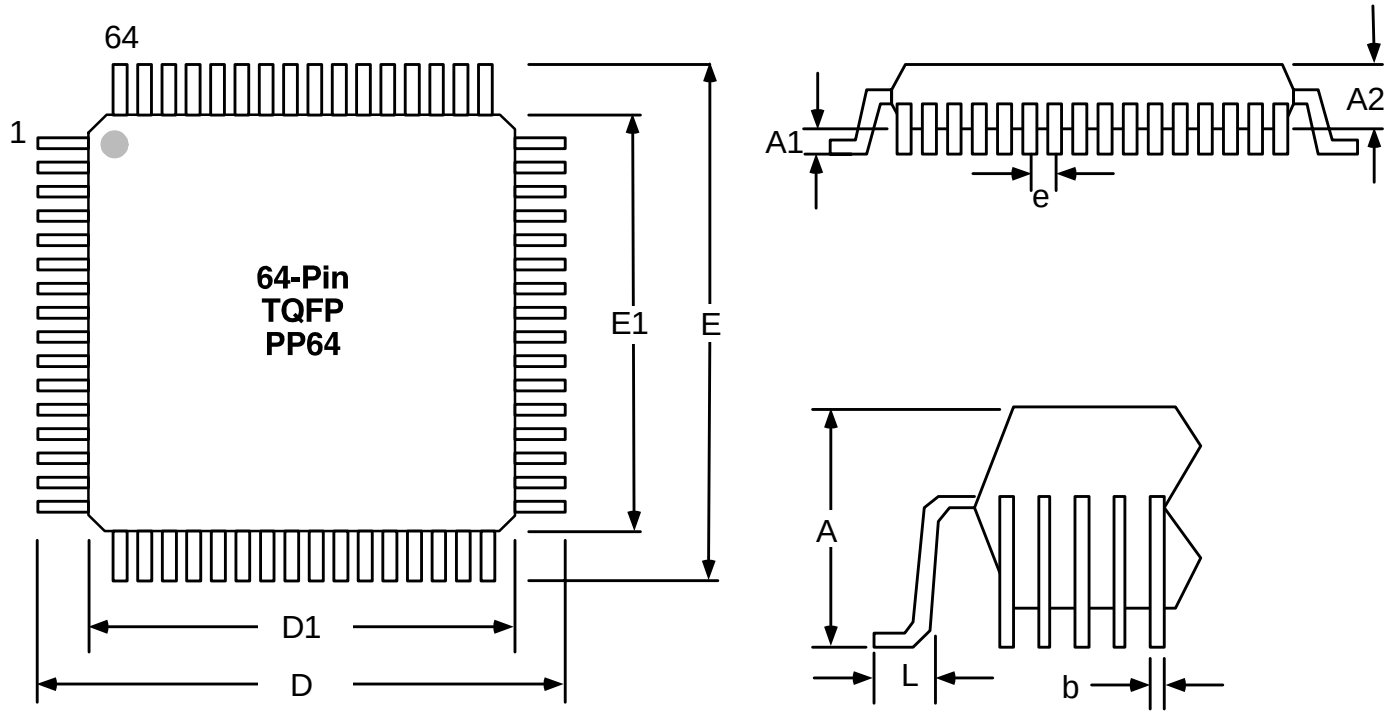
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 22



* Includes jig and scope capacitances.

Figure 22 Output Load

Package Dimensions



SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	.05	.10	.15
A2	1.35	1.40	1.45
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
N		64	
e		.50 BSC	
b	.17	.22	.27
b1	.17	.20	.23
ccc	-	-	.08
ddd	-	-	.08

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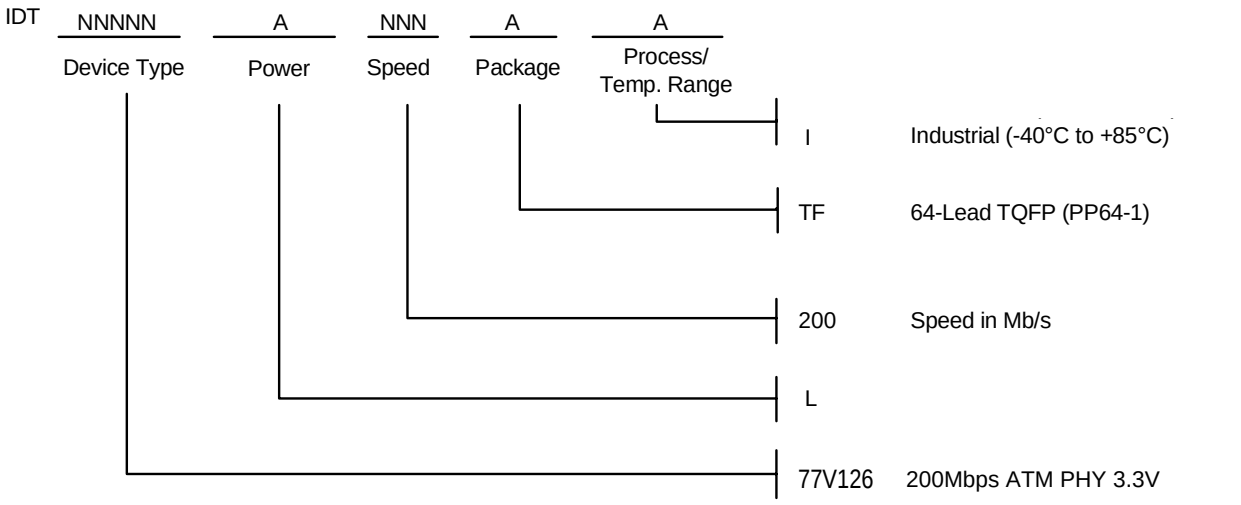
Dimensions are in millimeters

PSC-4046 is a more comprehensive package outline drawing which is available from the packaging section of the IDT web site.

Ordering Information



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Revision History

September 20, 2001: Initial publication.

December 9, 2004: Removed Commerical Temperature Range from Datasheet and updated to current template.

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