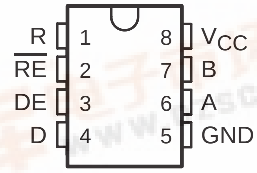
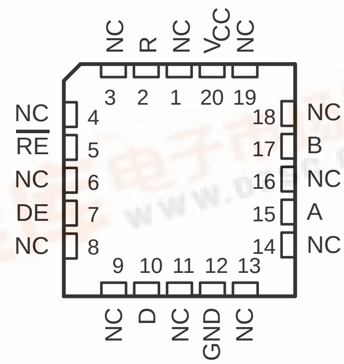
SN55LBC176, SN65LBC176, SN65LBC176Q, SN75LBC176
DIFFERENTIAL BUS TRANSCEIVERS

- **Bidirectional Transceiver**
- **Meets or Exceeds the Requirements of ANSI Standard TIA/EIA−485−A and ISO 8482:1987(E)**
- **High-Speed Low-Power LinBiCMOS™ Circuitry**
- **Designed for High-Speed Operation in Both Serial and Parallel Applications**
- **Low Skew**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Very Low Disabled Supply Current . . . 200 μA Maximum**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Thermal-Shutdown Protection**
- **Driver Positive-and Negative-Current Limiting**
- **Open-Circuit Failsafe Receiver Design**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operates From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Available in Q-Temp Automotive**
  - **HighRel Automotive Applications**
  - **Configuration Control / Print Support**
  - **Qualification to Automotive Standards**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC − No internal connection

description

The SN55LBC176, SN65LBC176, SN65LBC176Q, and SN75LBC176 differential bus transceivers are monolithic, integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. They are designed for balanced transmission lines and meet ANSI Standard TIA/EIA−485−A (RS-485) and ISO 8482:1987(E).

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_{IA} - V_{IB}$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

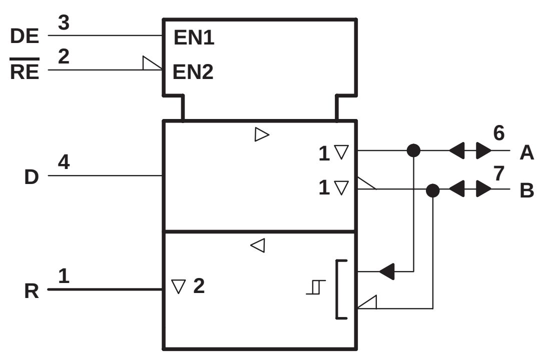
description (continued)

The SN55LBC176, SN65LBC176, SN65LBC176Q, and SN75LBC176 combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can externally connect together to function as a direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications. Very low device supply current can be achieved by disabling the driver and the receiver.

These transceivers are suitable for ANSI Standard TIA/EIA−485 (RS-485) and ISO 8482 applications to the extent that they are specified in the operating conditions and characteristics section of this data sheet. Certain limits contained in TIA/EIA−485−A and ISO 8482:1987 (E) are not met or cannot be tested over the entire military temperature range.

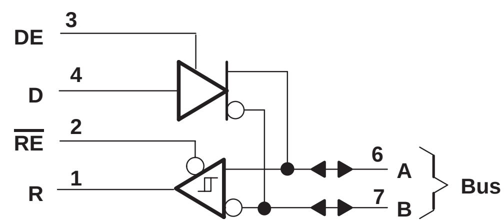
The SN55LBC176 is characterized for operation from −55°C to 125°C. The SN65LBC176 is characterized for operation from −40°C to 85°C, and the SN65LBC176Q is characterized for operation from −40°C to 125°C. The SN75LBC176 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

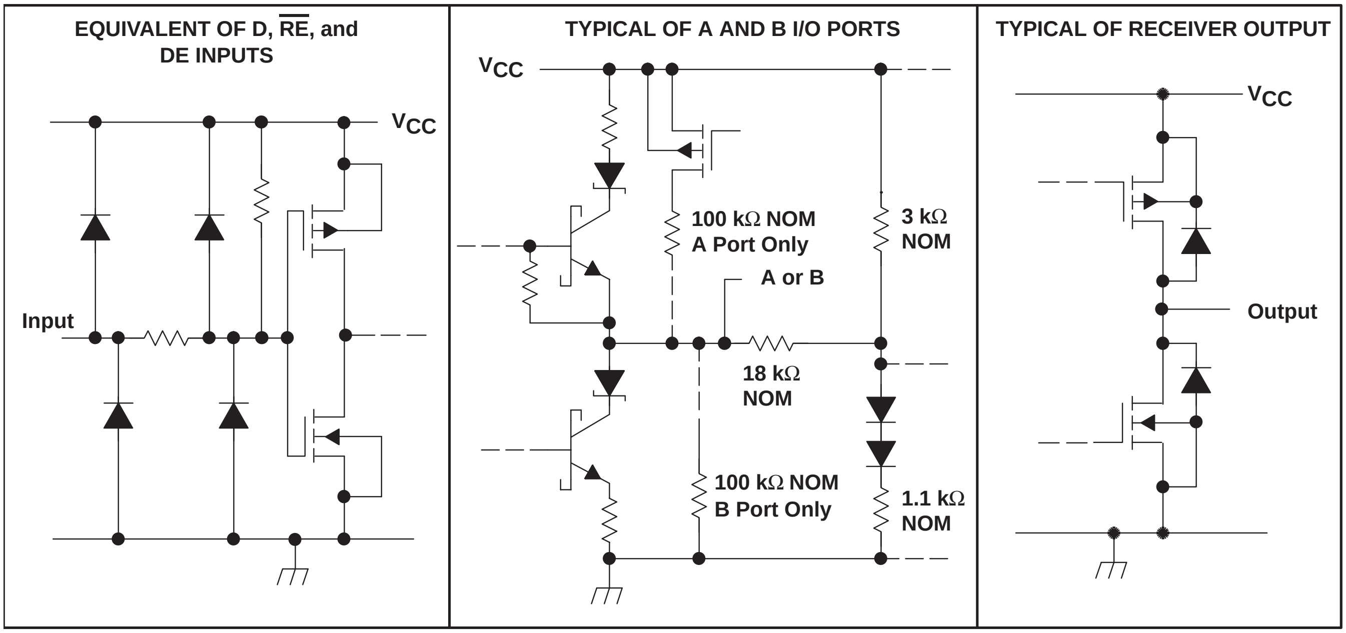
logic diagram (positive logic)



AVAILABLE OPTIONS

T_A	PACKAGE	PART NUMBER	PART MARKING
0°C to 70°C	SOP	SN75LBC176D	7LB176
	PDIP	SN75LBC176P	75LBC176
−40°C to 85°C	SOP	SN65LBC176D	6LB176
	PDIP	SN65LBC176P	65LBC176
−40°C to 110°C	SOP	SN65LBC176QD	LB176Q
	SOP	SN65LBC176QDR	LB176Q
−55°C to 125°C	LCCC	SNJ55LBC176FK	SNJ55LBC176FK
	CDIP	SNJ55LBC176JG	SNJ55LBC176

schematics of inputs and outputs



absolute maximum ratings†

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Voltage range at any bus terminal . . . . −10 V to 15 V
Input voltage, V_I (D, DE, R, or $\overline{RE}$) . . . . −0.3 V to V_{CC} + 0.5 V
Receiver output current, I_O . . . . ±10 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	THERMAL MODEL	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 110°C POWER RATING
D	Low K†	526 mW	5.0 mW/°C	301 mW	226 mW	—
	High K‡	882 mW	8.4 mW/°C	504 mW	378 mW	—
P		840 mW	8.0 mW/°C	480 mW	360 mW	—
JG		1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
FK		1375 mW	11.0 mW/°C	880 mW	715 mW	440 mW

† In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51−3.
‡ In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51−7.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)		−12		12	V
High-level output current, I_{OH}	Driver	−60			mA
	Receiver	−400			µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Junction temperature, T_J				140	°C
Operating free-air temperature, T_A	SN55LBC176	−55		125	°C
	SN65LBC176	−40		85	
	SN65LBC176Q	−40		125	
	SN75LBC176	0		70	

NOTE 2: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA			−1.5		V
V_O	Output voltage	$I_O = 0$			0	6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$			1.5	6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	$R_L = 54\ \Omega$, See Note 3	See Figure 1,	55LBC176, 65LBC176, 65LBC176Q	1.1		V
				75LBC176	1.5	5	
V_{OD3}	Differential output voltage	$V_{test} = -7$ V to 12 V, See Note 3	See Figure 2,	55LCB176, 65LCB176, 65LBC176Q	1.1		V
				75LBC176	1.5	5	
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage †	$R_L = 54\ \Omega$ or $100\ \Omega$,	See Figure 1		−0.2	0.2	V
V_{OC}	Common-mode output voltage				−1	3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage†				−0.2	0.2	V
I_O	Output current	Output disabled, See Note 4	$V_O = 12$ V			1	mA
			$V_O = -7$ V		−0.8		
I_{IH}	High-level input current	$V_I = 2.4$ V			−100		μA
I_{IL}	Low-level input current	$V_I = 0.4$ V			−100		μA
I_{OS}	Short-circuit output current	$V_O = -7$ V			−250		mA
		$V_O = 0$			−150		
		$V_O = V_{CC}$				250	
		$V_O = 12$ V					
I_{CC}	Supply current	$V_I = 0$ or V_{CC}, No load	Receiver disabled and driver enabled	55LBC176, 65LBC176Q		1.75	mA
				65LBC176, 75LBC176		1.5	
			Receiver and driver disabled	55LBC176, 65LBC176Q		0.25	
				65LBC176, 75LBC176		0.2	

† $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.

NOTES: 3. This device meets the V_{OD} requirements of TIA/EIA−485−A above 0°C only.
4. This applies for both power on and off; refer to TIA/EIA−485−A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	SN55LBC176 SN65LBC176Q			SN65LBC176 SN75LBC176			UNIT
			MIN	TYP	MAX	MIN	TYP†	MAX	
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω, C_L = 50 pF, See Figure 3	8		31	8		25	ns
$t_{t(OD)}$	Differential output transition time			12			12		ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(ODH)} - t_{d(ODL)} \rvert$)				6		0	6	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 4			65			35	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 5			65			35	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 4			105			60	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 5			105			35	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-485
V_O	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$	V_t (test termination measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	None
I_O	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA		−0.2‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$) (see Figure 4)					50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA			−1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OH} = −400 μA,		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 8 mA,				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V			−20		20	μA
I_I	Line input current	Other input = 0 V, See Note 5	V_I = 12 V				1	mA
			V_I = −7 V		−0.8			
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V			−100			μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V			−100			μA
r_I	Input resistance				12			kΩ
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver enabled and driver disabled				3.9	mA
			Receiver and driver disabled	SN55LBC176, SN65LBC176, SN65LBC176Q			0.25	mA
				SN75LBC176			0.2	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet.
NOTE 5: This applies for both power on and power off. Refer to ANSI Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF

PARAMETER		TEST CONDITIONS	SN55LBC176 SN65LBC176Q		SN65LBC176 SN75LBC176			UNIT
			MIN	MAX	MIN	TYP†	MAX	
t_{PLH}	Propagation delay time, low- to high-level single-ended output	V_{ID} = −1.5 V to 1.5 V, See Figure 7	11	37	11		33	ns
t_{PHL}	Propagation delay time, high- to low-level single-ended output		11	37	11		33	ns
$t_{sk(p)}$	Pulse skew (| $t_{PLH} - t_{PHL}$ |)			10		3	6	ns
t_{PZH}	Output enable time to high level	See Figure 8		35			35	ns
t_{PZL}	Output enable time to low level			35			30	ns
t_{PHZ}	Output disable time from high level	See Figure 8		35			35	ns
t_{PLZ}	Output disable time from low level			35			30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

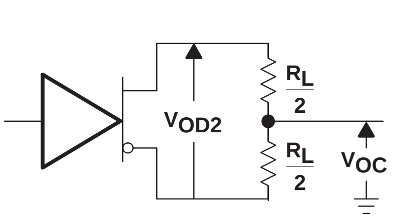


Figure 1. Driver V_{OD} and V_{OC}

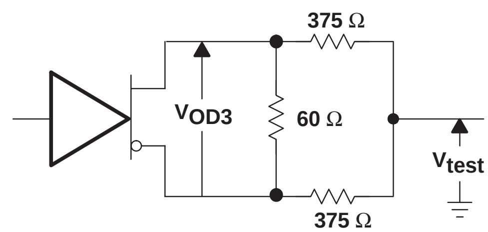
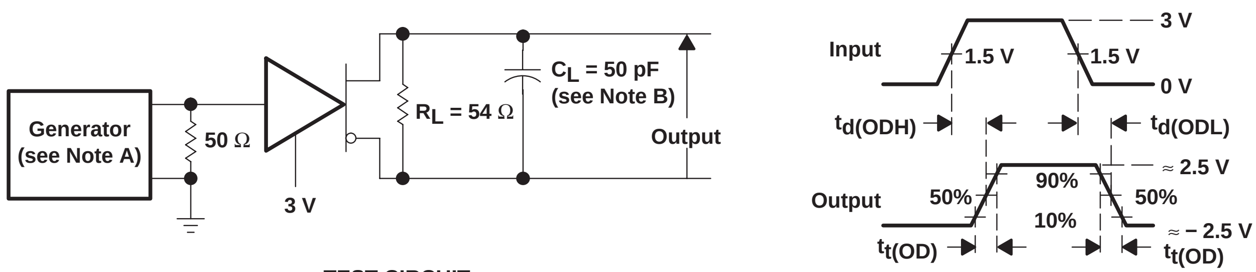


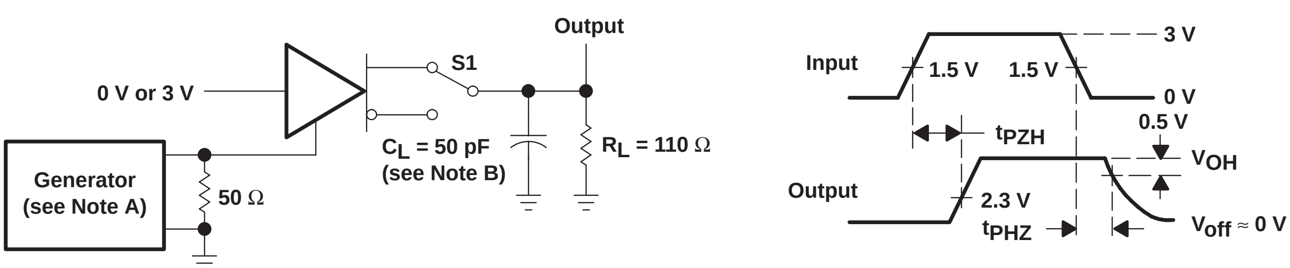
Figure 2. Driver V_{OD3}



TEST CIRCUIT

VOLTAGE WAVEFORMS

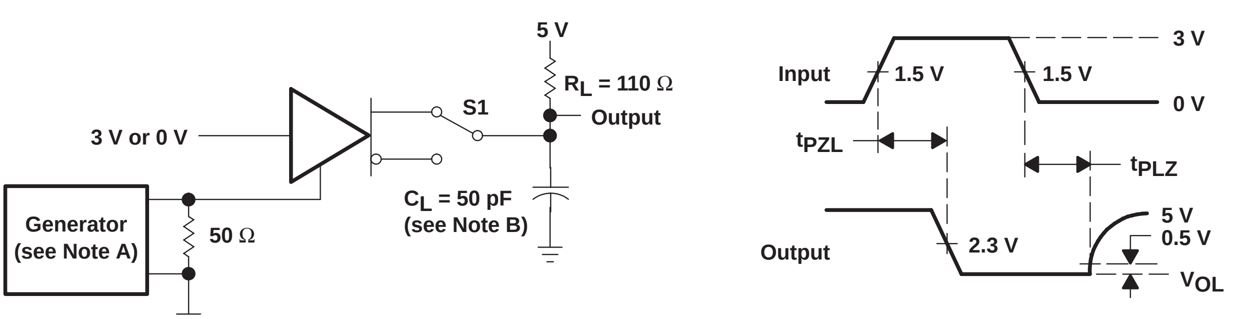
Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

VOLTAGE WAVEFORMS

Figure 4. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

VOLTAGE WAVEFORMS

Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

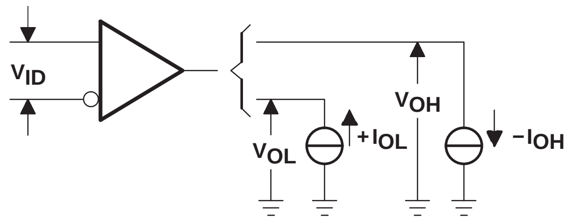
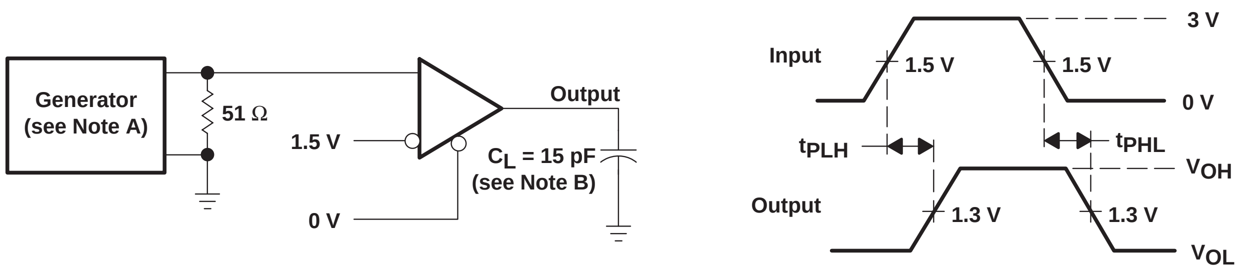


Figure 6. Receiver V_{OH} and V_{OL}



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

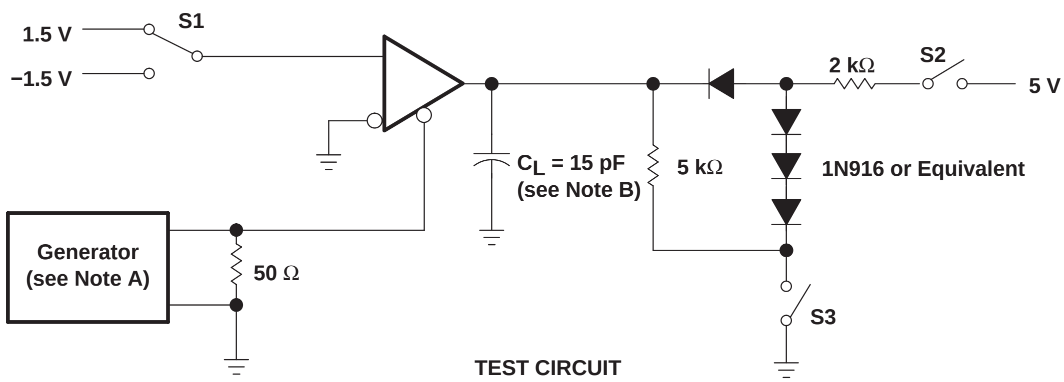
Figure 7. Receiver Test Circuit and Voltage Waveforms

THERMAL CHARACTERISTICS − D PACKAGE

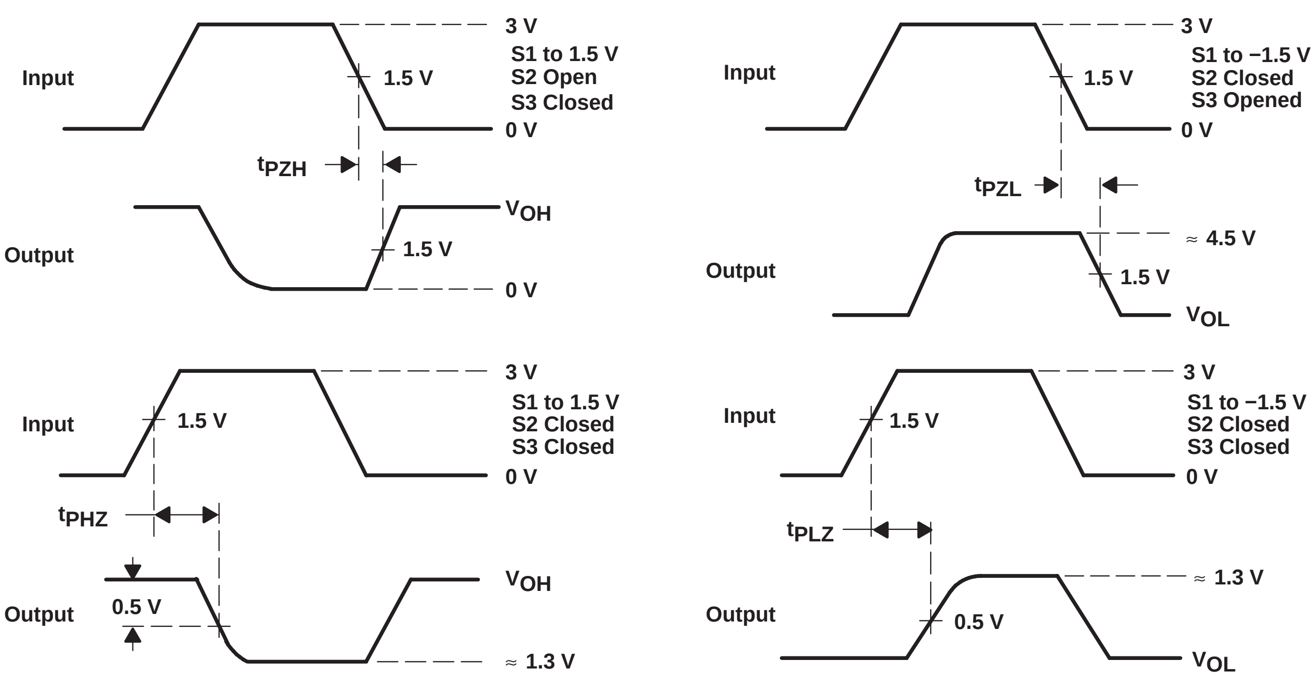
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Junction−to−ambient thermal reisistance, θ_{JA}†	Low-K board, no air flow		199.4		°C/W
	High-K board, no air flow		119		
Junction−to−board thermal reisistance, θ_{JB}	High-K board, no air flow		67		
Junction−to−case thermal reisistance, θ_{JC}			46.6		
Average power dissipation, $P_{(AVG)}$	R_L = 54 Ω, input to D is 10 Mbps 50% duty cycle square wave, V_{CC} = 5.25 V, T_J = 130 °C.			330	mW
Thermal shutdown junction temperature, T_{SD}			165		°C

† See TI application note literature number SZZA003, Package Thermal Characterization Methodologies, for an explanation of this parameter.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 8. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

THERMAL CHARACTERISTICS OF IC PACKAGES

Θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

Θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

Θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. Θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives *best case* in−use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in Θ_{JA} can be measured between these two test cards

Θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

Θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with Θ_{JB} in 1-dimensional thermal simulation of a package system.

Θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold−plate structure. Θ_{JB} is only defined for the high-k test card.

Θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see Figure 1).

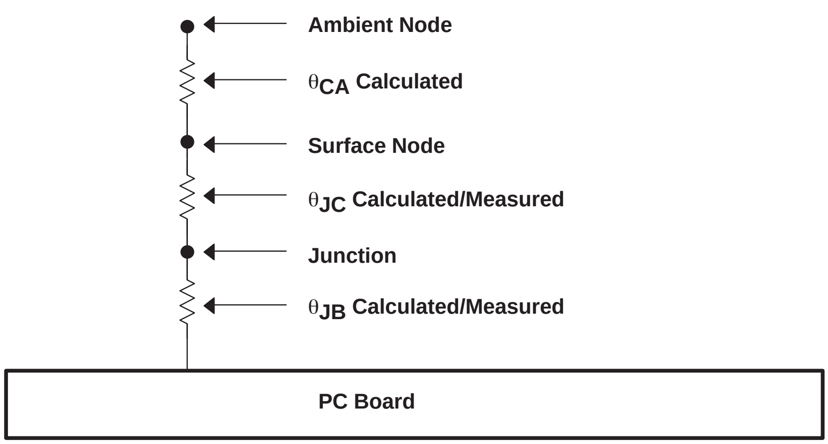
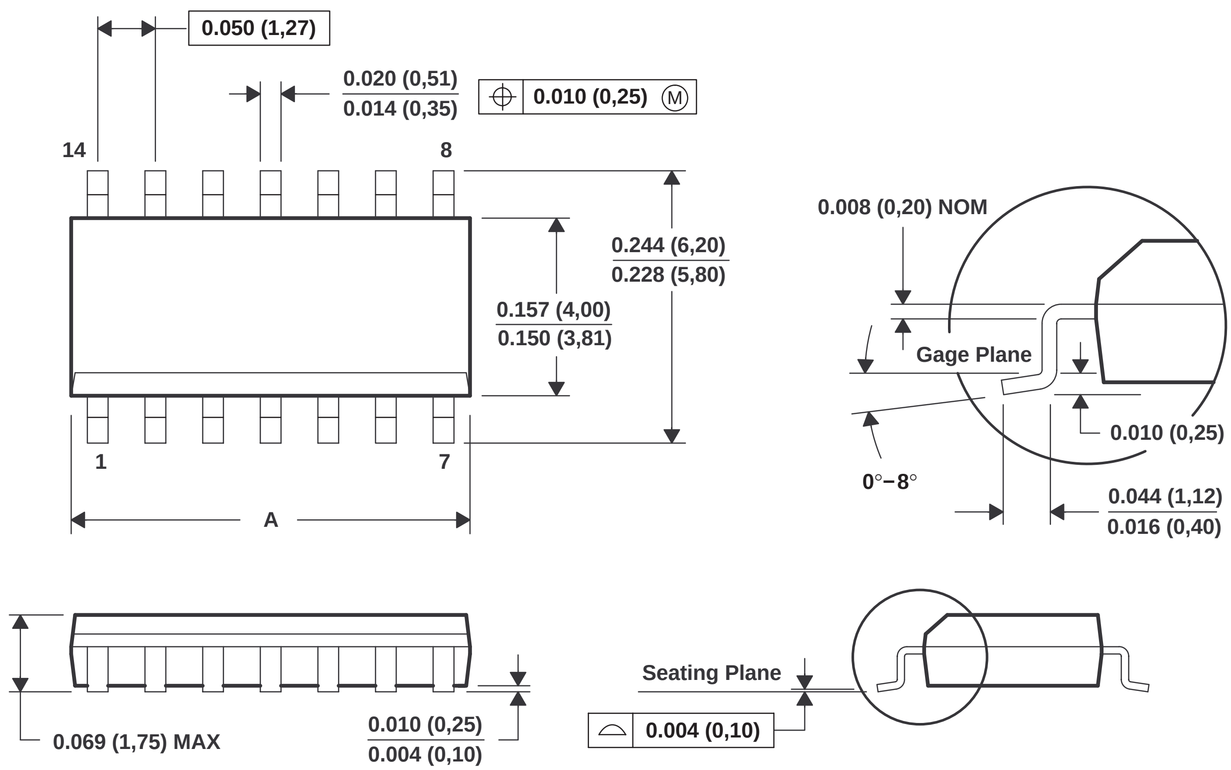


Figure 1. Thermal Resistance

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

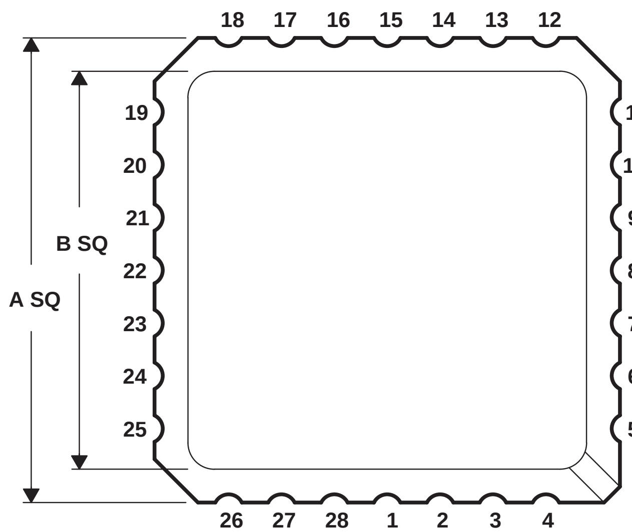
4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

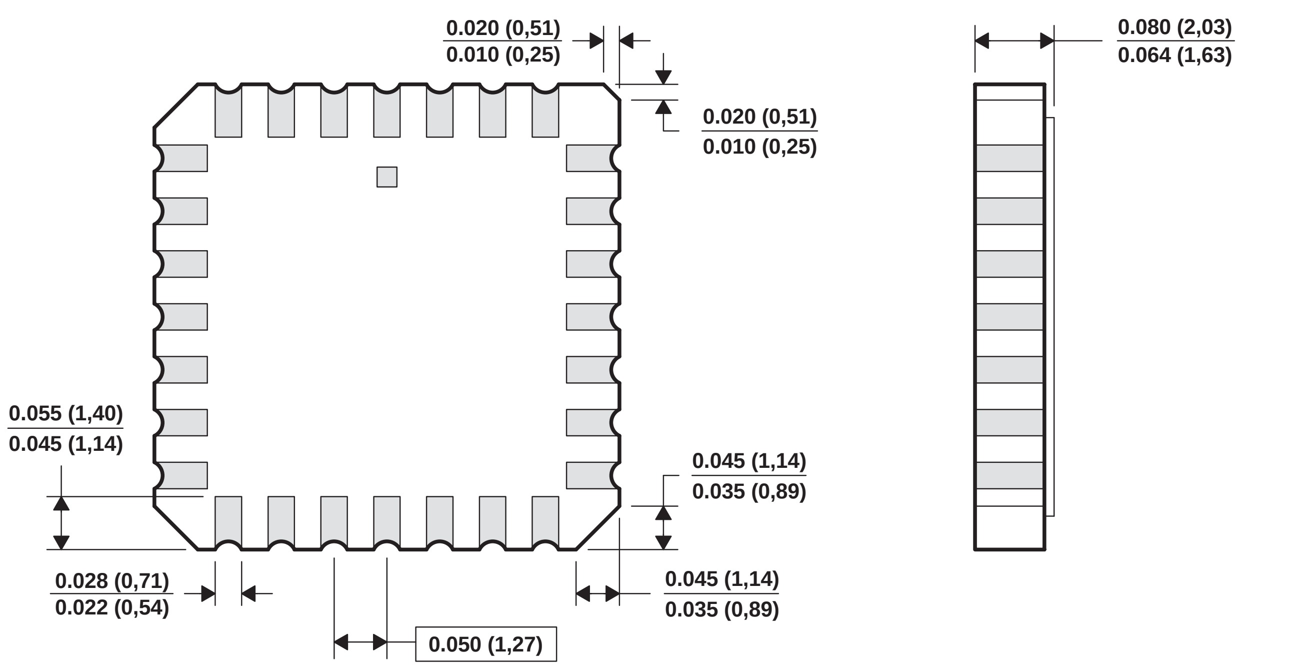
MECHANICAL INFORMATION

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINALS SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

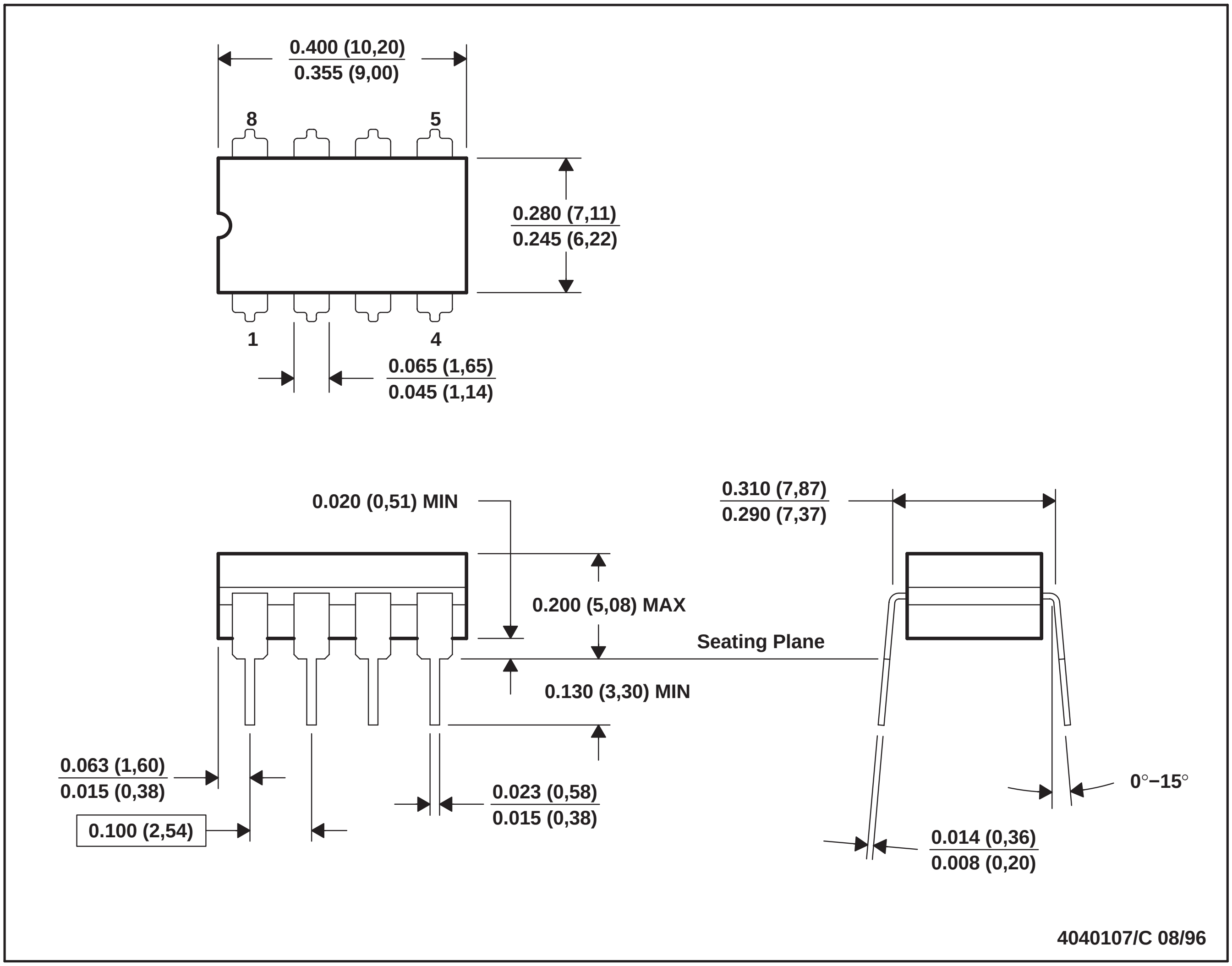


4040140 / C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold-plated.
E. Falls within JEDEC MS-004

MECHANICAL INFORMATION

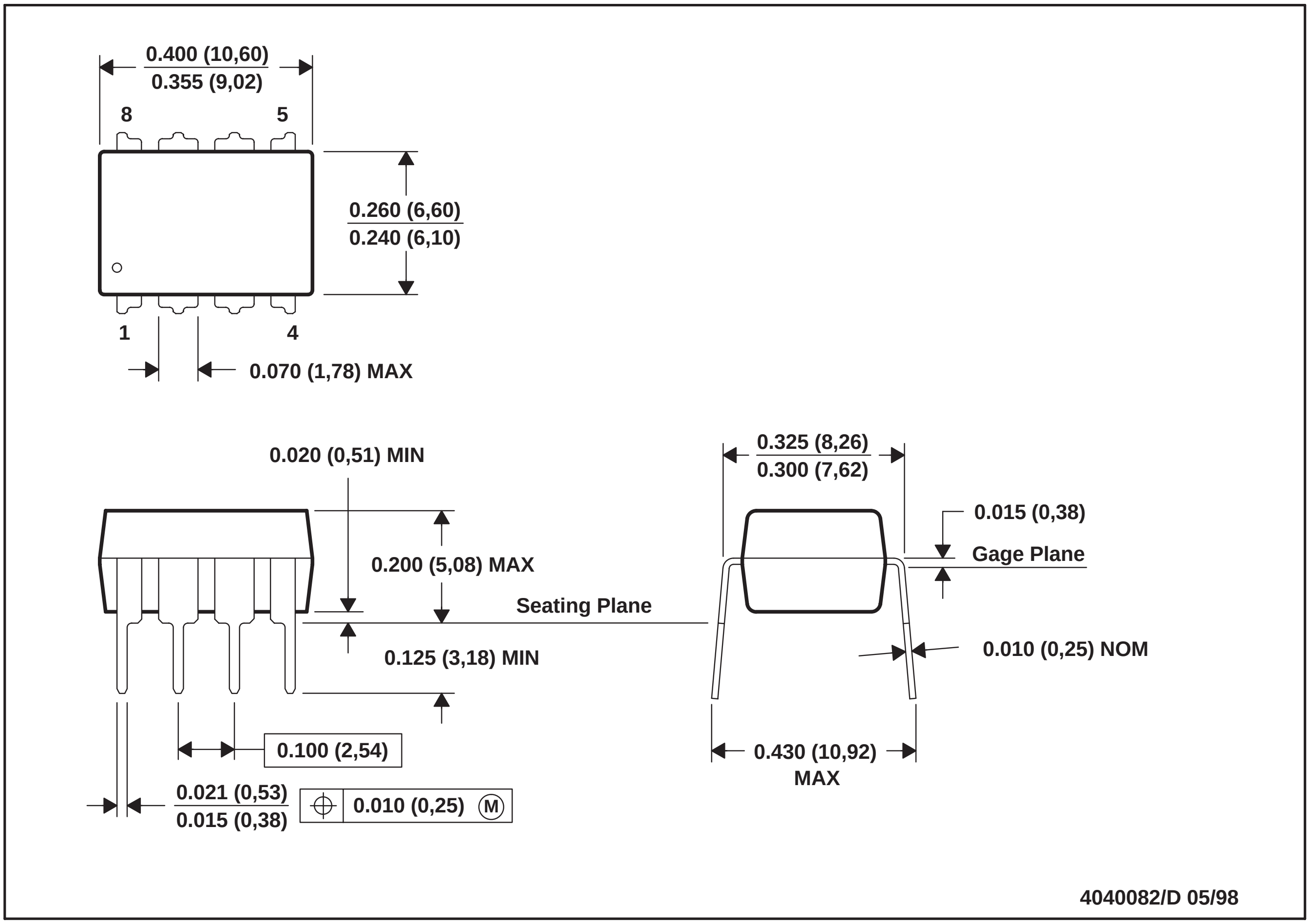
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL INFORMATION

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9318301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9318301QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
SN65LBC176D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC176DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC176DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC176DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC176P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65LBC176PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65LBC176QD	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LBC176QDR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN75LBC176D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC176DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC176DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC176DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC176P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75LBC176PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ55LBC176FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ55LBC176JG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

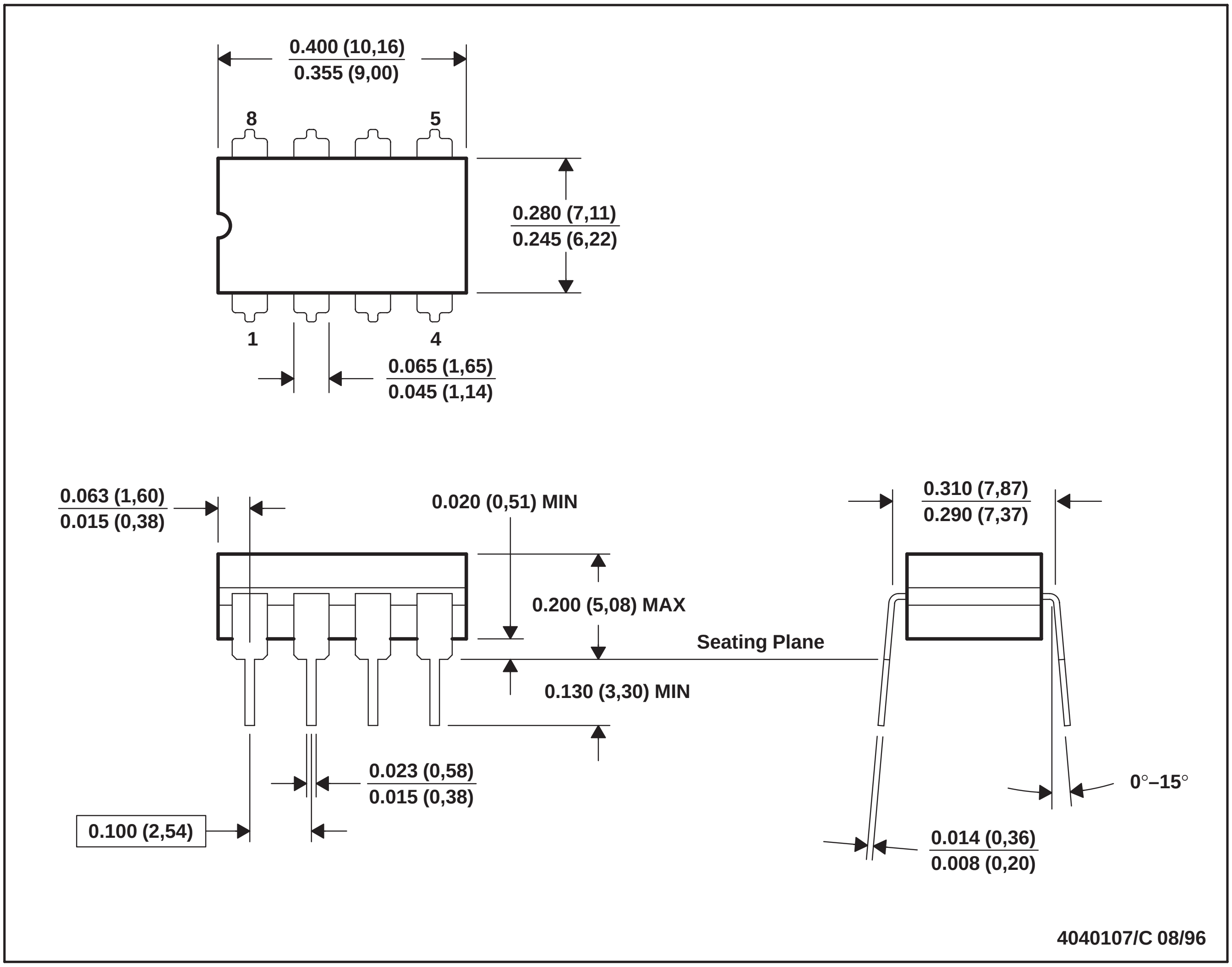
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder

temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

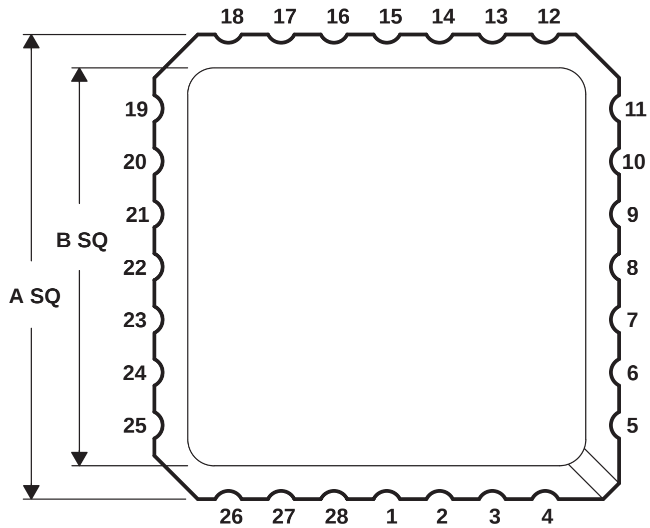
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



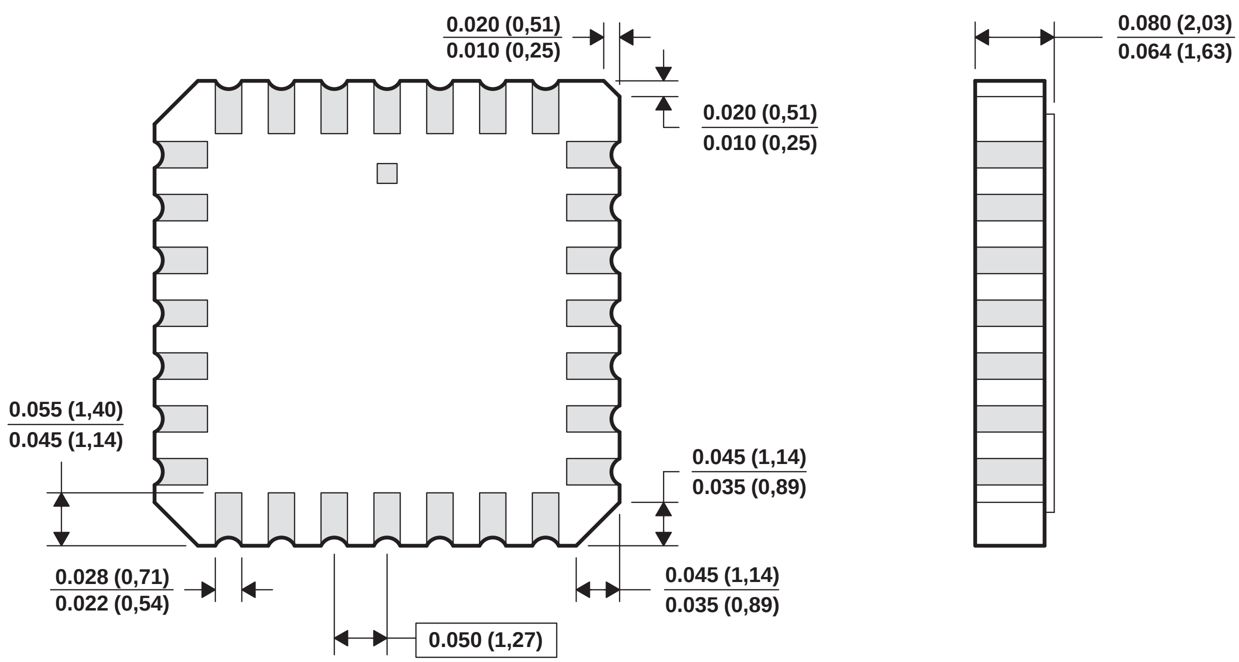
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



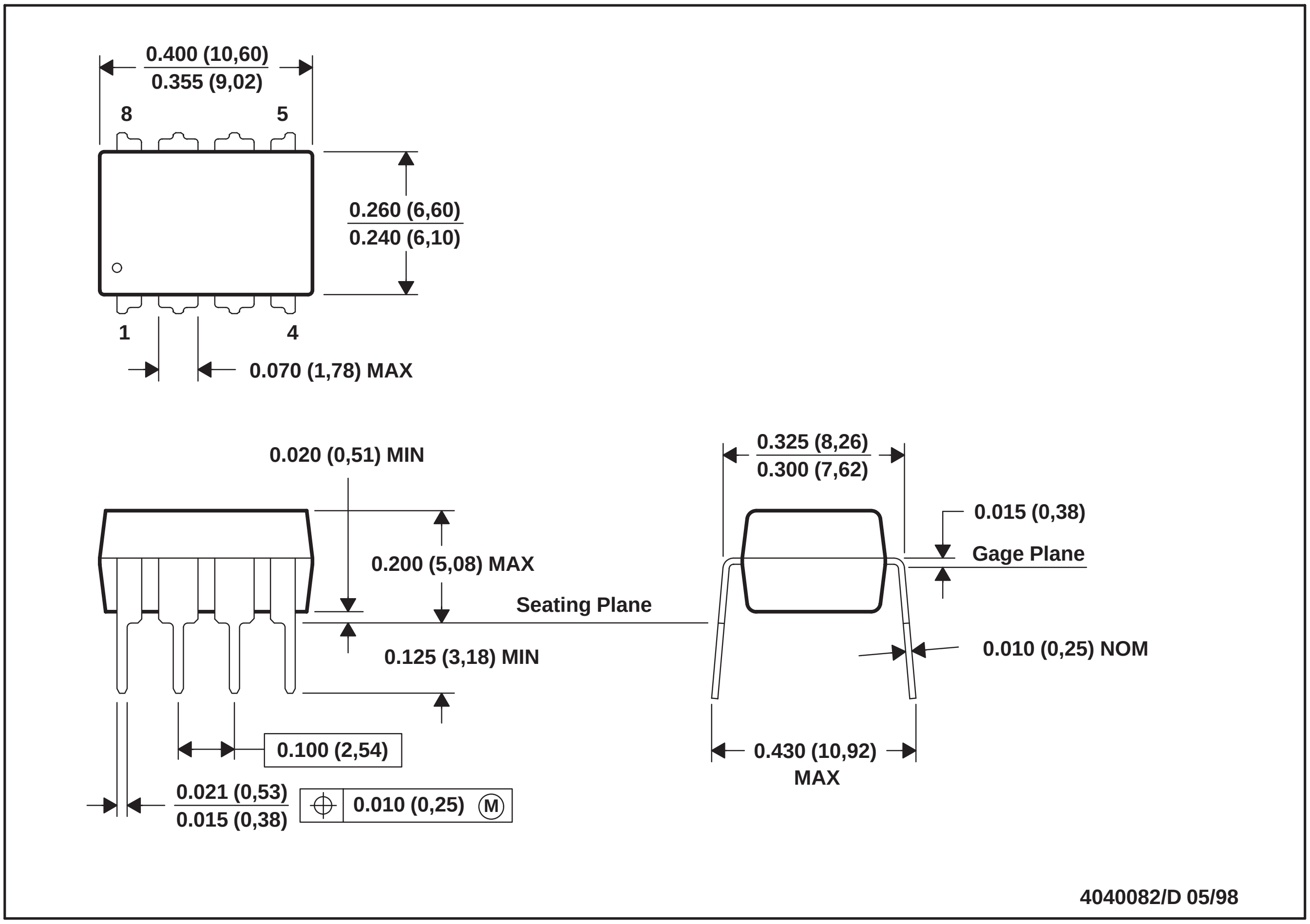
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140 / D 10/96

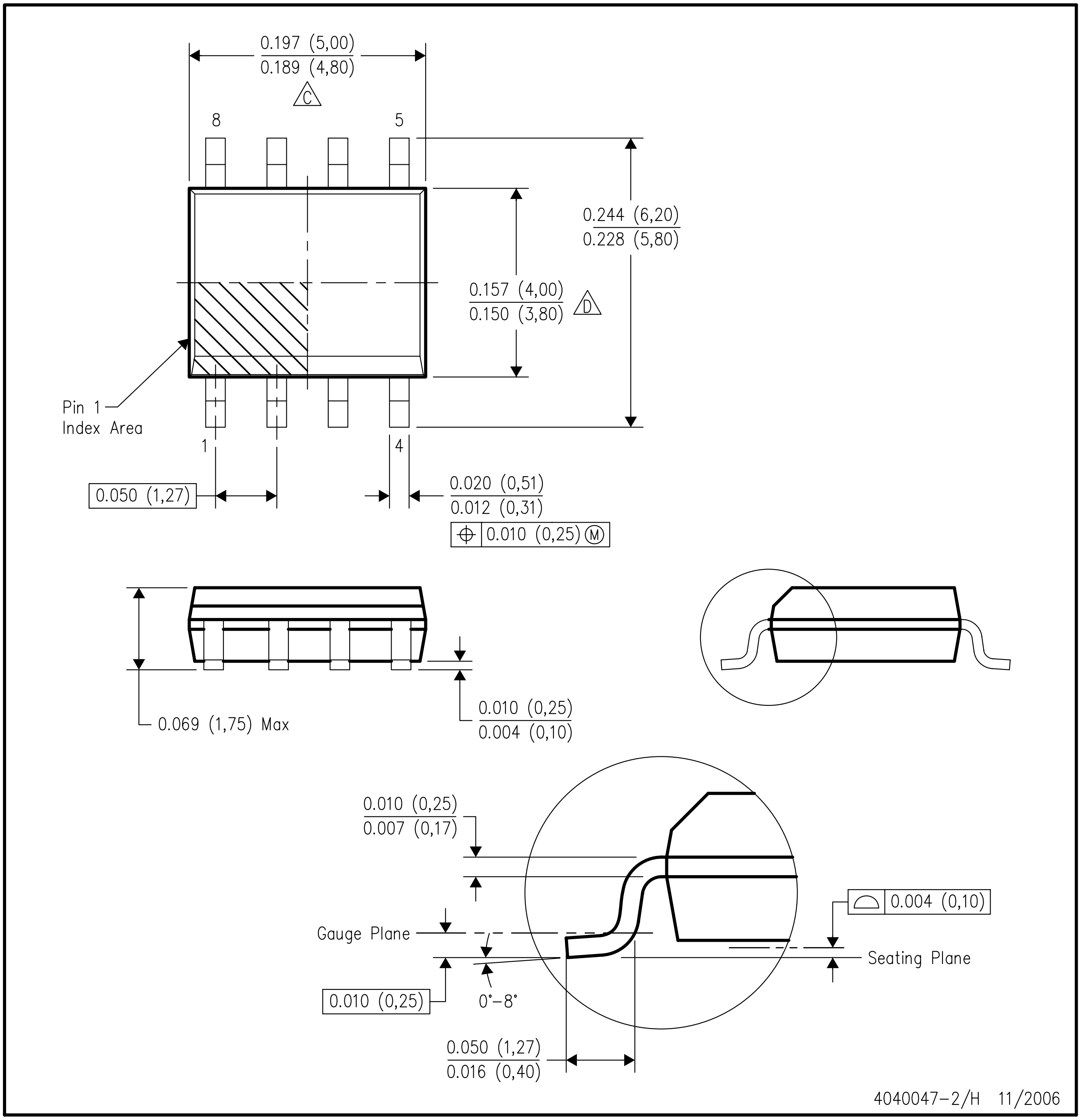
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265