



UNISONIC TECHNOLOGIES CO., LTD

MC34072

LINEAR INTEGRATED CIRCUIT

HIGH SLEW RATE, WIDE BANDWIDTH, SINGLE SUPPLY OPERATIONAL AMPLIFIER

DESCRIPTION

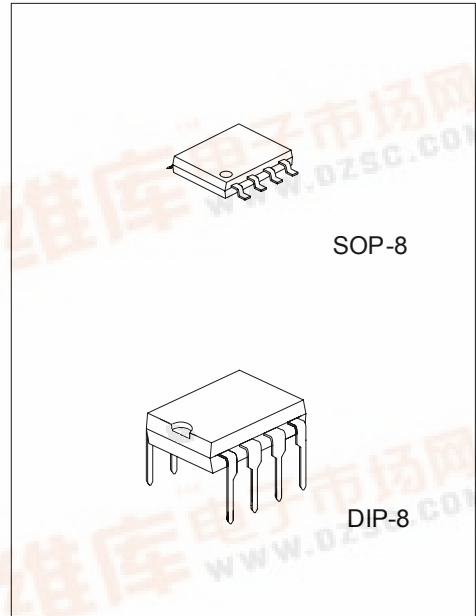
The UTC MC34072 offer 4.5MHz of gain bandwidth product, 13V/ μ s slew rate and fast setting time without the use of JFET device technology. Although it can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With A Darlington input stage, it exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

FEATURES

- * Wide bandwidth: 4.5 MHz
- * High slew rate: 13V/ μ s
- * Fast settling time: 1.1 μ s to 0.1%
- * Wide single supply operation: 3.0V to 44V
- * Wide input common mode voltage range:
Includes Ground (V_{EE})
- * Low input offset voltage: 3.0mV maximum
- * Large output voltage swing: -14.7V to +14V
(with \pm 15V supplies)
- * Large Capacitance Drive Capability: 0pF to 10,000 pF
- * Low total harmonic distortion: 0.02%
- * Excellent phase margin: 60°
- * Excellent gain margin: 12dB
- * Output short circuit protection
- * ESD Diodes/Clamps provide input protection

ORDERING INFORMATION

Order Number		Package	Packing
Normal	Lead Free Plating		
MC34072-D08-T	MC34072L-D08-T	DIP-8	Tube
MC34072-S08-R	MC34072L-S08-R	SOP-8	Tape Reel
MC34072-S08-T	MC34072L-S08-T	SOP-8	Tube



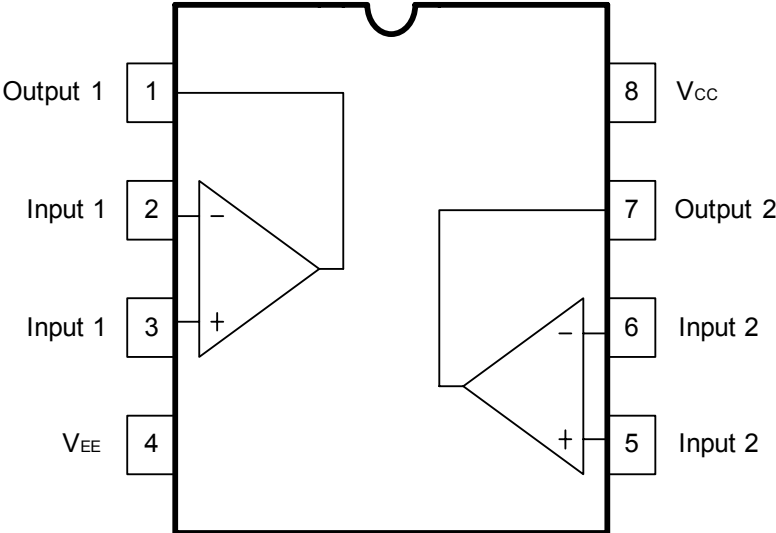
*Pb-free plating product number: MC34072L

MC34072L-D08-R

- (1)Packing Type
- (2)Package Type
- (3)Lead Plating

- (1) R: Tape Reel, T: Tube
- (2) D08: DIP-8, S08: SOP-8
- (3) L: Lead Free Plating Blank: Pb/Sn

■ PIN DESCRIPTION



■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (from V _{EE} to V _{CC})	V _S	+44	V
Differential Input Voltage	V _{I(DIFF)}	Note 1	V
Input Voltage	V _{IN}	Note 1	V
Output Short Circuit Duration (Note 2)	t _{SC}	Indefinite	sec
Junction Temperature	T _J	+125	°C
Operating Temperature	T _{OPR}	-20 ~ +85	°C
Storage Temperature Range	T _{STG}	-40 ~ +150	°C

Note 1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.

2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (see Fig. 1)

3. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

4. The device is guaranteed to meet performance specification within 0°C~+70°C operating temperature range and assured by design from -20°C~+85°C.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=+15V, V_{EE}=-15V, R_L=connected to ground, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	V _{I(OFF)}	R _S =100Ω, V _{CC} =+15V, V _{EE} =-15V, Ta=+25°C		0.5	3.0	mV
		V _{CM} =0V, V _{CC} =+5V, V _{EE} =0V, Ta=+25°C		0.5	3.0	mV
		V _{OUT} =0V, V _{CC} =+15V, V _{EE} =-15V, Ta=0°C to 70°C				5.0
Average Temperature Coefficient of Input Offset Voltage	ΔV _{IO} /ΔT	R _S =10Ω, V _{CM} =0V, V _{OUT} =0V, Ta=0°C to 70°C		10		μV/°C
Input Bias Current	I _{I(BIAS)}	V _{CM} =0V, V _{OUT} =0V		100	500	nA
			Ta=+25°C			700
Input Offset Current	I _{I(OFF)}	V _{CM} =0V, V _{OUT} =0V		6.0	50	nA
			Ta=0°C to 70°C			300
Input Common Mode Voltage	V _{ICR}	Ta=+25°C		V _{EE} to (V _{CC} -1.8)		V
		Ta=0°C to 70°C		V _{EE} to (V _{CC} -2.2)		V
Large Signal Voltage Gain	G _V	V _{OUT} =±10V, R _L =2.0kΩ		50	100	V/mV
			Ta=0°C to 70°C	25		
Output Voltage Swing (V _{ID} =±1.0V)	V _{OH}	V _{CC} =+5.0V, V _{EE} =0V, R _L =2.0kΩ, Ta=+25°C	3.7	4.0		V
		V _{CC} =+15.0V, V _{EE} =-15V, R _L =10kΩ, Ta=+25°C	13.6	14		V
		V _{CC} =+15.0V, V _{EE} =-15V, R _L =2.0kΩ, Ta=0°C to 70°C	13.4			V
Output Voltage Swing (V _{ID} =±1.0V)	V _{OL}	V _{CC} =+5.0V, V _{EE} =0V, R _L =2.0kΩ, Ta=+25°C		0.1	0.3	V
		V _{CC} =+15.0V, V _{EE} =-15V, R _L =10kΩ, TA=+25°C		-14.7	-14.3	V
		V _{CC} =+15.0V, V _{EE} =-15V, R _L =2.0kΩ, T _A =0°C to 70°C			-13.5	V
Output Short Circuit current	I _{SC}	V _{I(DIFF)} =1.0V, V _{OUT} =0V, Ta=25°C	Source	10	30	mA
			Sink	20	30	
Common Mode Rejection	CMR	R _S ≤10kΩ, V _{CM} =V _{ICR} , Ta=25°C	80	97		dB
Power Supply Rejection (R _S =100Ω)	SVR	V _{CC} /V _{EE} =+16.5V/-16.5V to +13.5/-13.5V, Ta=25°C	80	97		dB

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Current (Per Amplifier, No Load)	I _D	V _{CC} =+5.0V, V _{EE} =0V, V _{OUT} =+2.5V, Ta=+25°C		1.6	2.0	mA
		V _{CC} =+15.0V, V _{EE} =-15V, V _{OUT} =0V, Ta=+25°C		1.9	2.5	mA
		V _{CC} =+15.0V, V _{EE} =-15V, V _{OUT} =0V, Ta=0°C to 70°C			2.8	mA
Slew Rate	SR	V _{IN} =-10V to +10V, R _L =2.0kΩ, C _L =500pF	Av=+1.0	8.0	10	V/μs
			Av=-1.0		13	
Setting Time	ts	10 Setp, Av=-1.0 to 0.1% (+1/2 LSB of 9-Bits) to 0.01% (+1/2 LSB of 12-Bits)		1.1 2.2		μs
Gain Bandwidth Product	GB _W	f=100kHz	3.5	4.5		MHz
Power Bandwidth	B _W	Av=+1.0, R _L =2kΩ, V _{OUT} =20Vpp, THD=5.0%		160		kHz
Phase Margin	fm	R _L =2kΩ		60		Deg
		R _L =2kΩ, C _L =300pF		40		Deg
Gain Margin	Am	R _L =2kΩ		12		dB
		R _L =2kΩ, C _L =300pF		4		dB
Equivalent Input Noise Voltage	eN	Rs=100Ω, f=1.0kHz		32		nV/√Hz
Equivalent Input Noise Current	eN	f=1.0kHz		0.22		pA/√Hz
Differential Input Resistance	R _{IN}	V _{CM} =0V		150		MΩ
Differential Input Capacitance	C _{IN}	V _{CM} =0V		2.5		pF
Total Harmonic distortion	THD	Av=+10, R _L =2.0kΩ, 2.0Vpp≤V _{OUT} ≤20Vpp, f=10kHz		0.02		%
Channel Separation		f=10kHz		120		dB
Open Loop Output Impedance	I _{ZoI}	f=1.0MHz		30		W

■ REPRESENTATIVE SCHEMATIC DIAGRAM

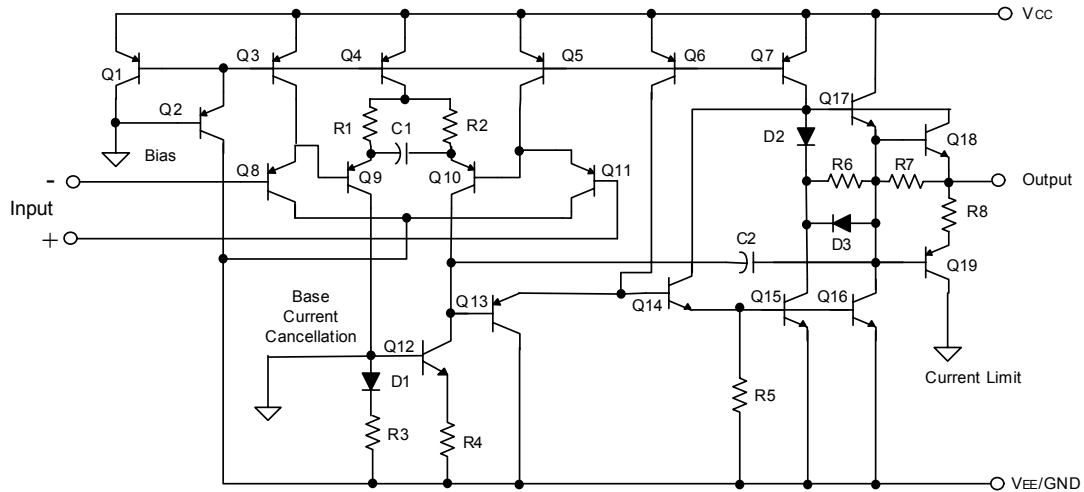
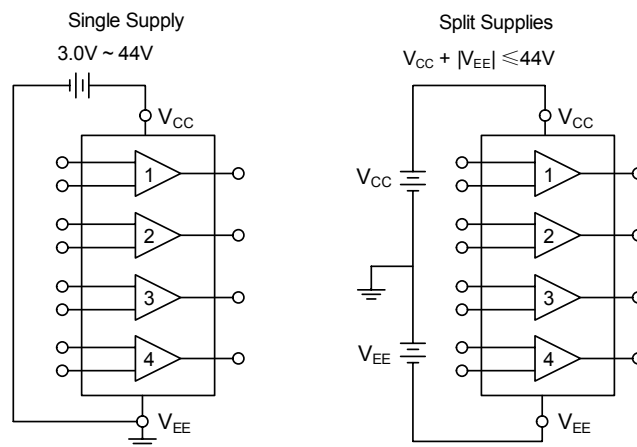
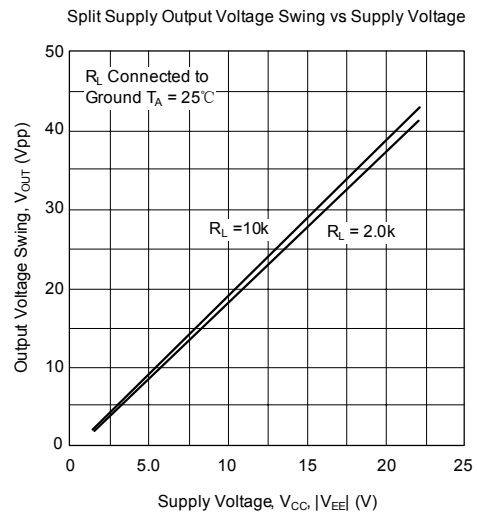
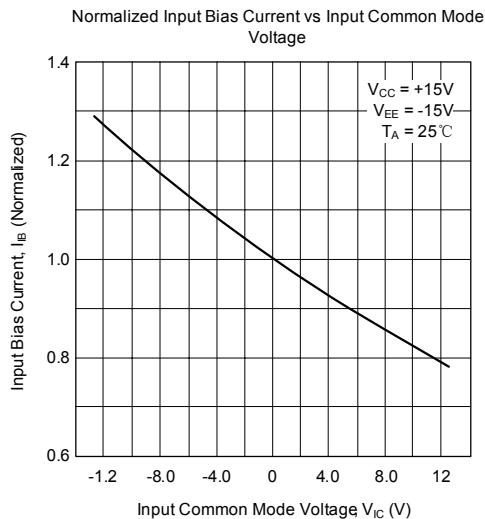
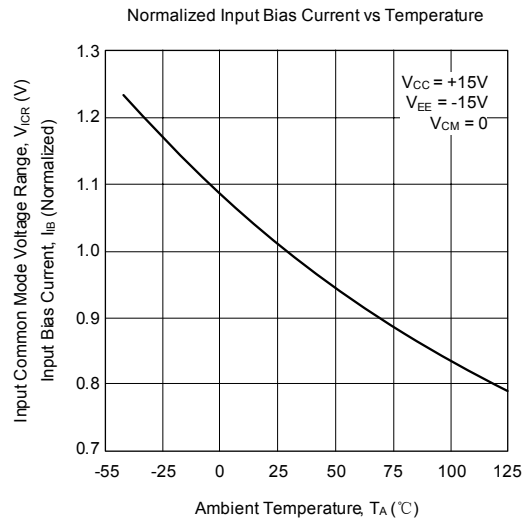
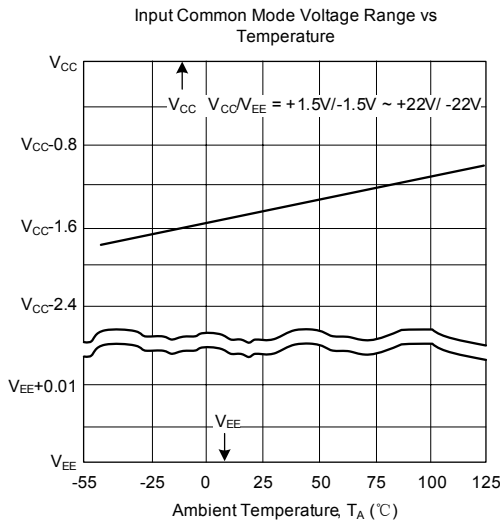
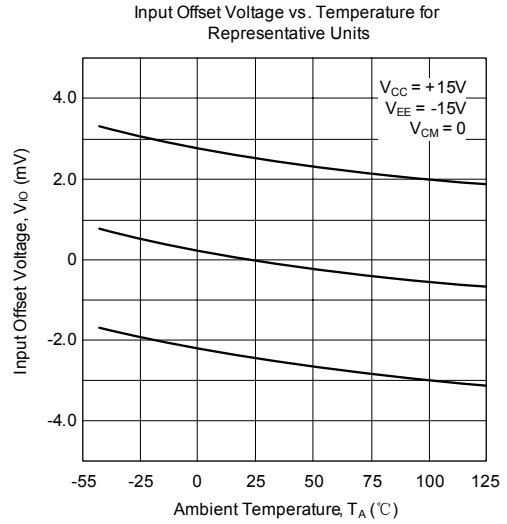
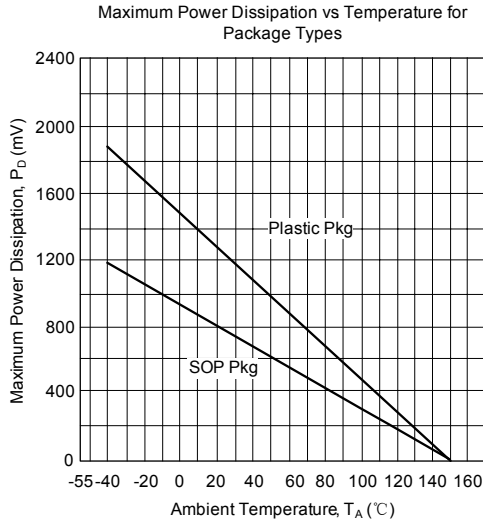


FIG.1

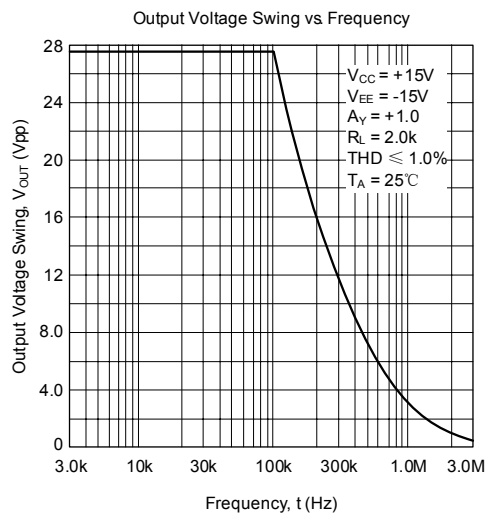
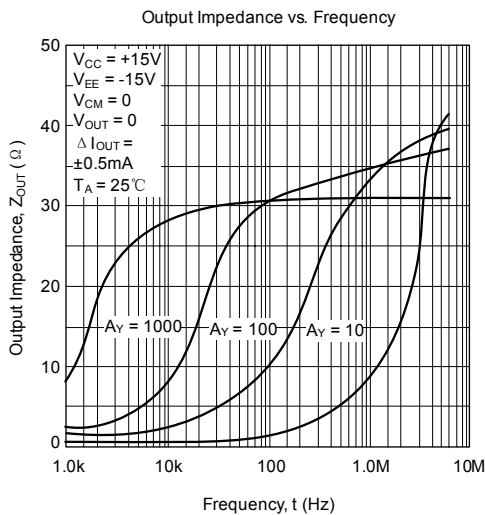
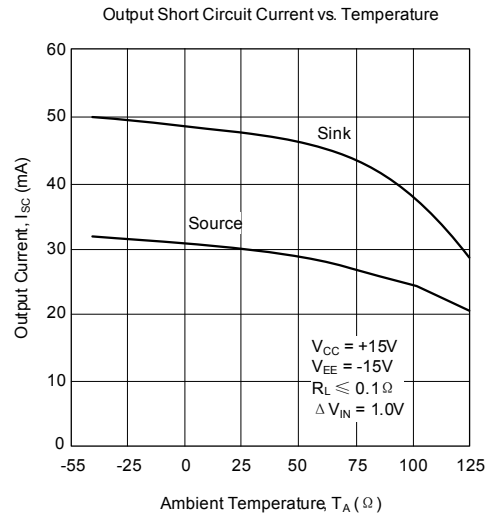
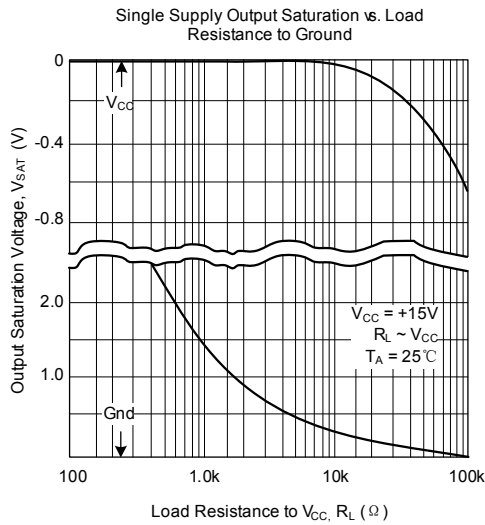
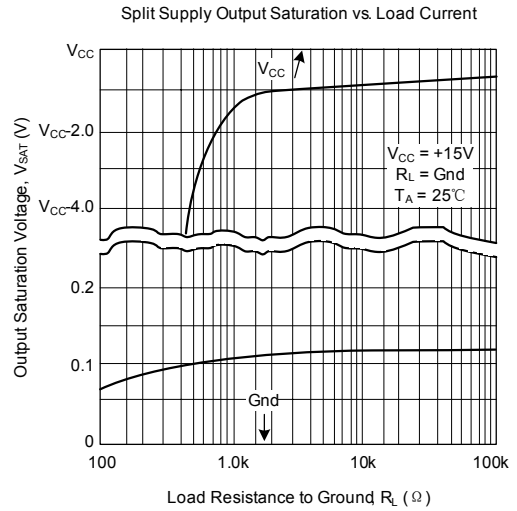
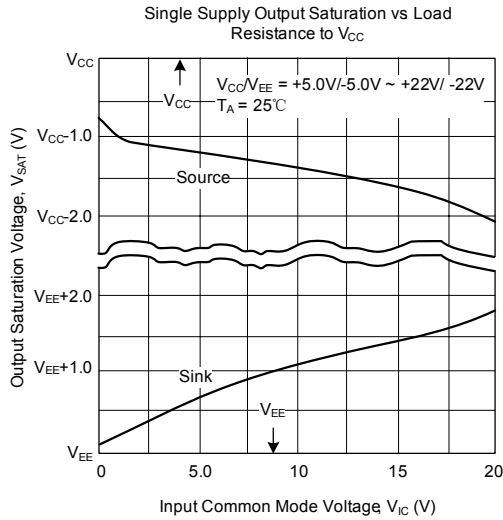
■ POWER SUPPLY CONFIGURATIONS



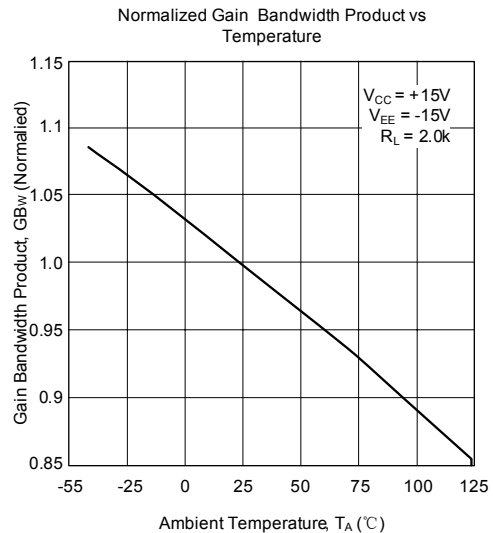
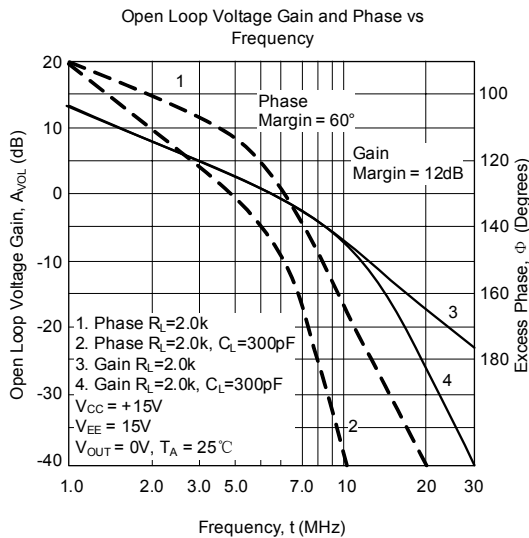
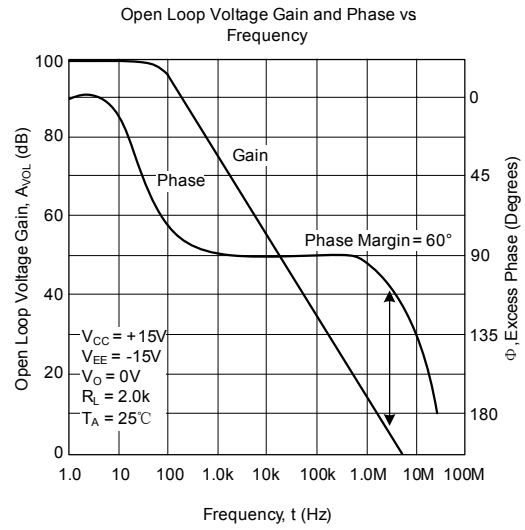
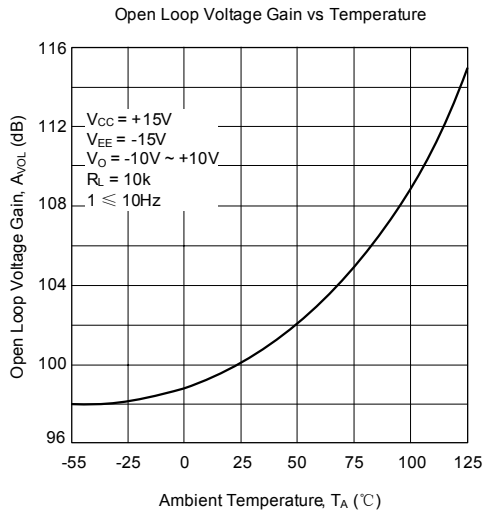
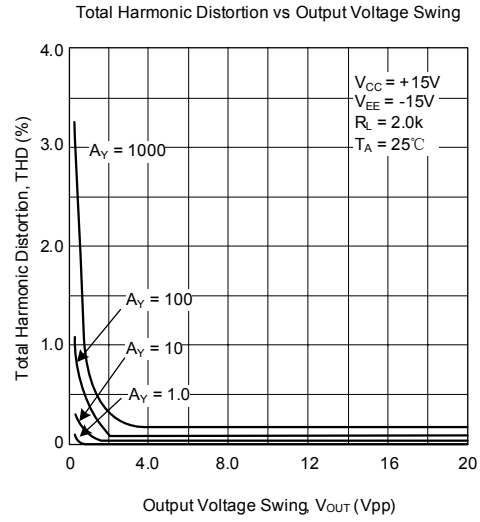
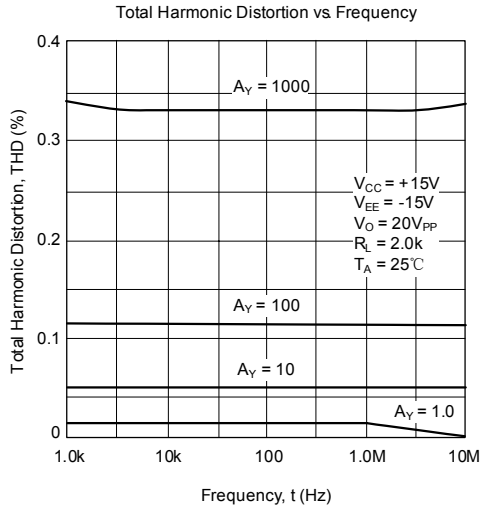
TYPICAL CHARACTERISTICS



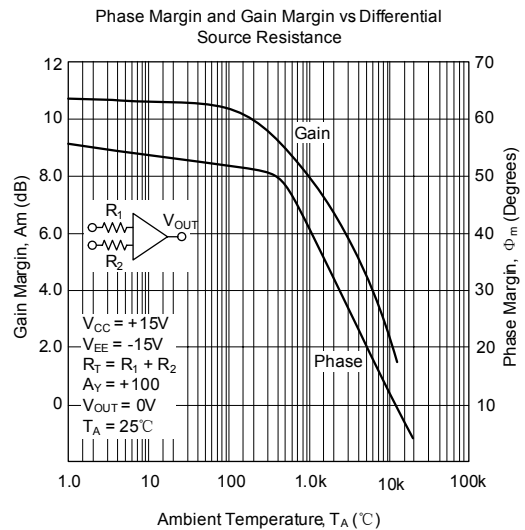
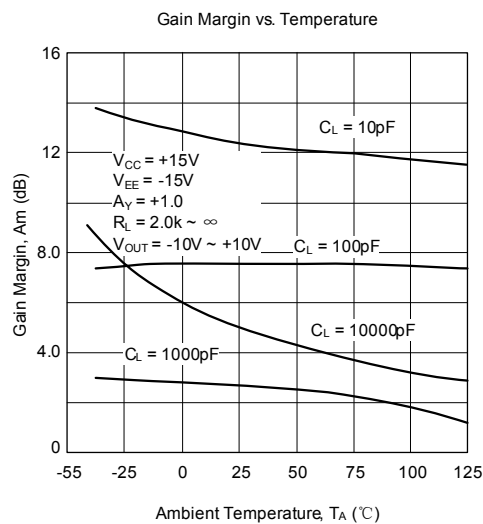
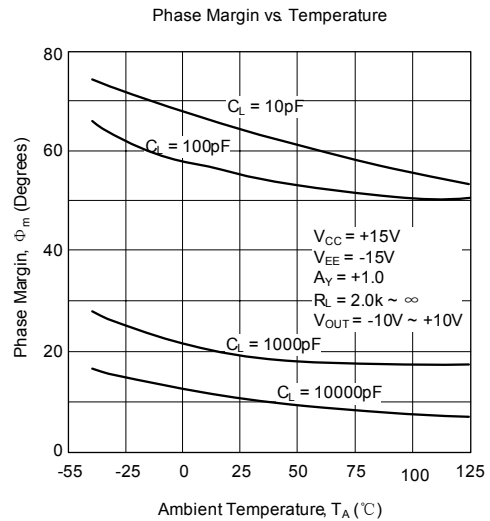
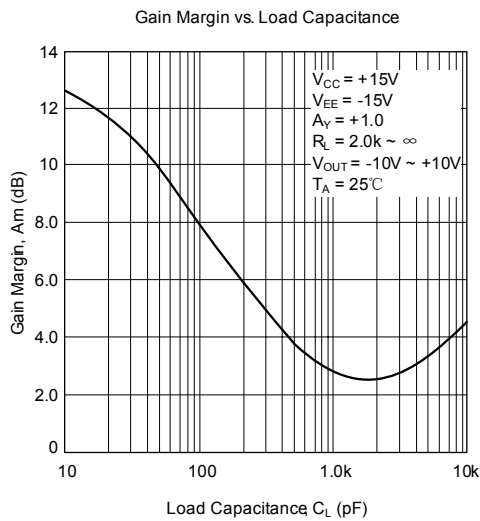
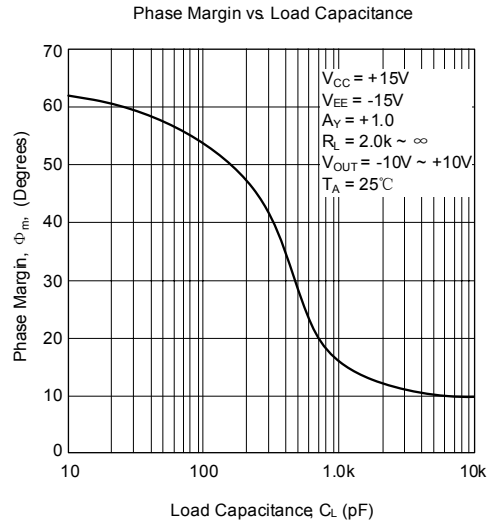
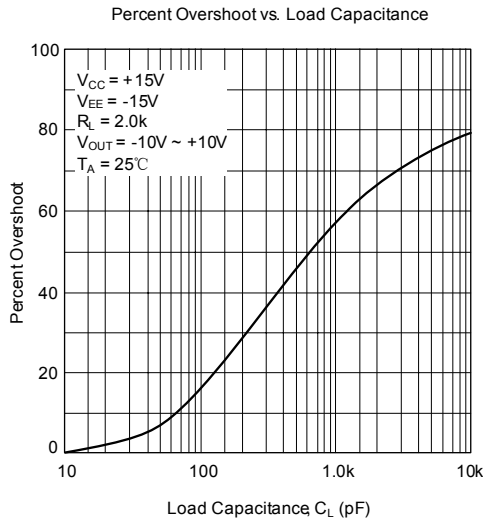
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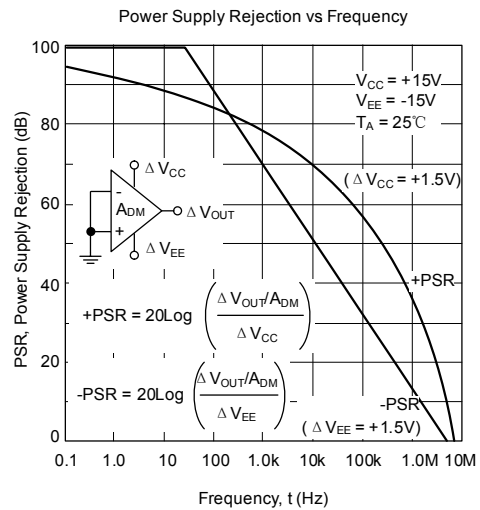
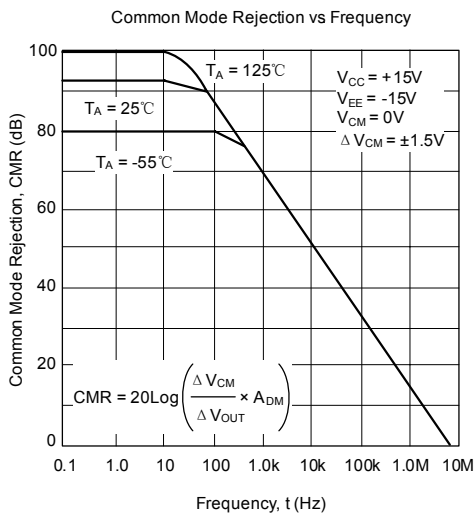
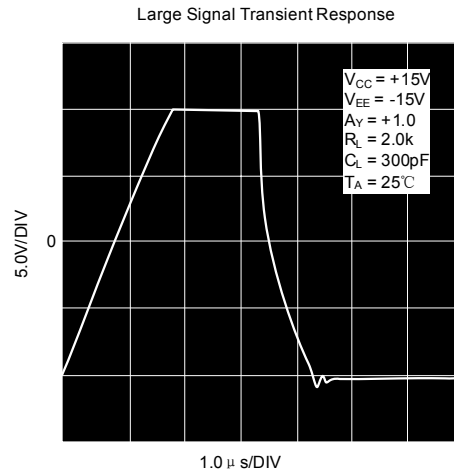
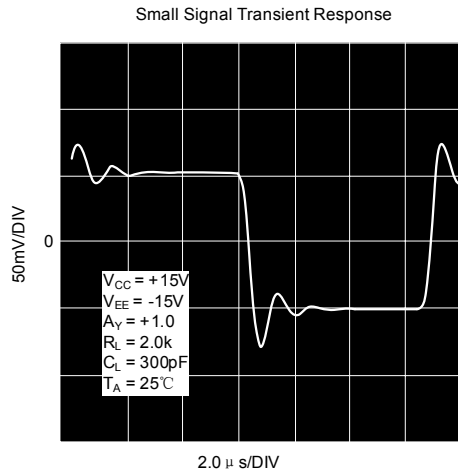
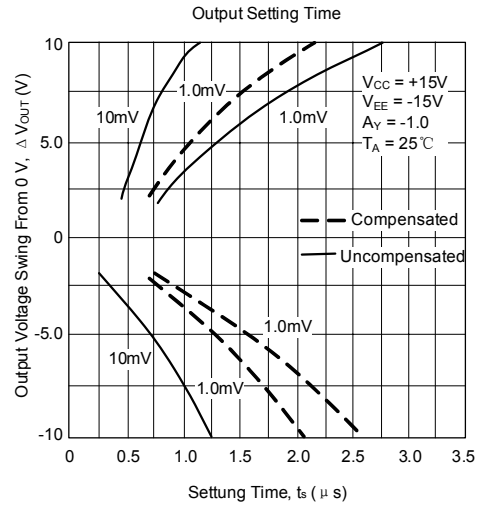
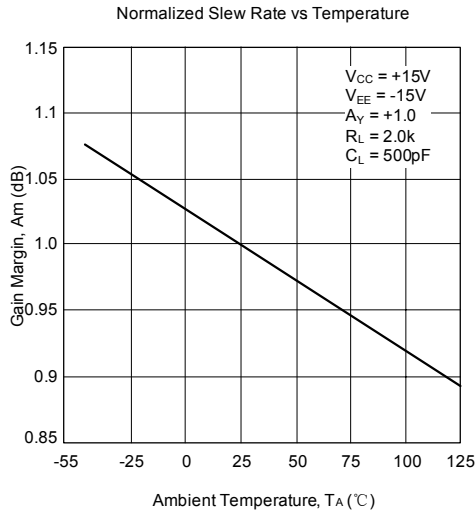
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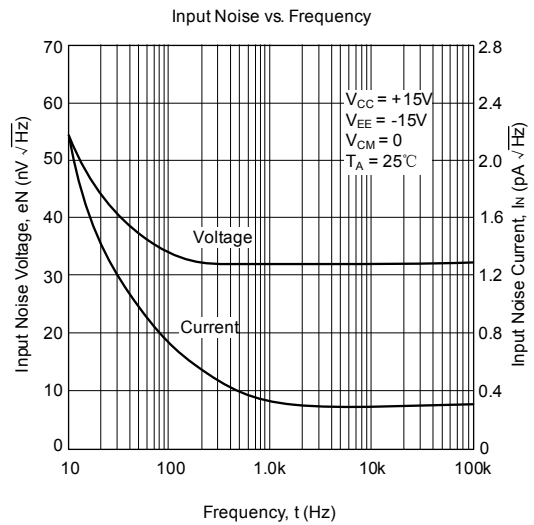
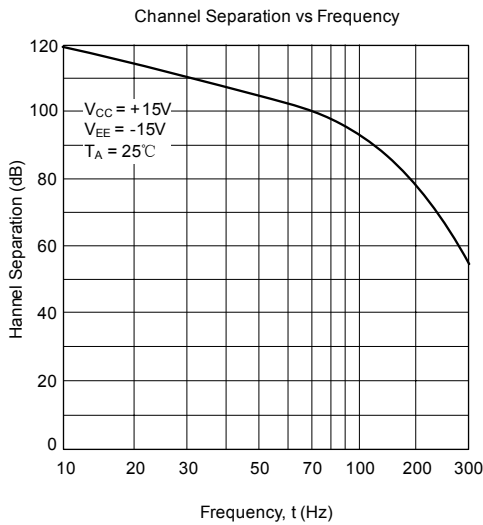
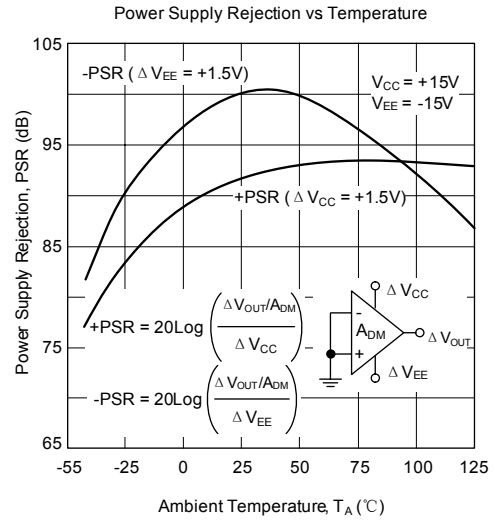
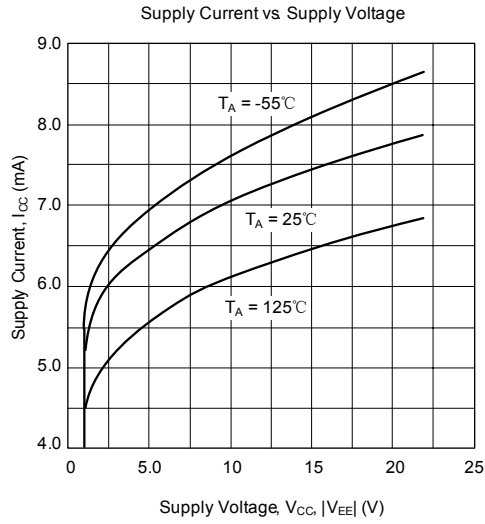
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■ TYPICAL CHARACTERISTICS(Cont.)



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