OKI

Oki, Network Solutions for a Global Society

FEDR27T401E-02-01 Issue Date: Apr. 17, 2002

OKI Semiconductor

MR27T401E

512K-Word × 8-Bit P2ROM

FEATURES

 \cdot 524,288-word \times 8-bit

- · 2.7 V to 3.6 V power supply
- Access timeOperating current100 ns MAX25 mA MAX
- · Standby current 10 µA MAX
- · Input/Output TTL compatible
- · Three-state output

PACKAGES

- · MR27T401E-xxxMA 32-pin plastic SOP (SOP32-P-525-1.27-K)
- MR27T401E-xxxTA

 32-pin plastic TSOP (TSOP I 32-P-814-0.50-1K)

P2ROM ADVANCED TECHNOLOGY

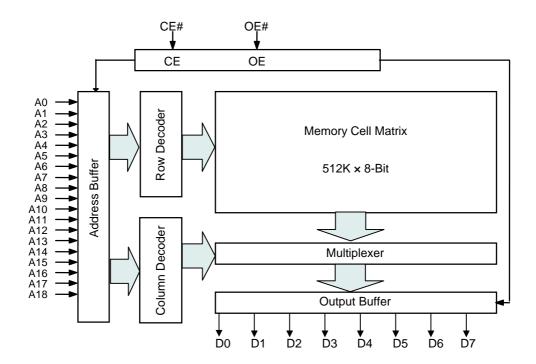
P2ROM stands for Production Programmed ROM. This exclusive Oki technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

- Short lead time, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
- No mask charge, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
- No additional programming charge, unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
- · Custom Marking is available at no additional charge.

PIN CONFIGURATION (TOP VIEW) DC A16 A18 A15 A17 A12 A14 A13 Α8 A9 A11 А3 OF# 23 A1 22 CE 21 D7 20 D6 19 D5 18 D4 17 D3 A2 A10 A1 CE# A0 D0 D1 14 D2 VSS 16 OF# A9 Α8 CE# A13 D7 A14 D6 A17 D5 D4 25 D3 Vcc DC Vss A16 D2 A15 D1 A12 12 D0 A7 13 0 A0 A6 9 A1 14 15 A5 8 A2 A4 7 A3



BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin name	Functions
A0 to A18	Address inputs
D0 to D7	Data outputs
CE#	Chip enable input
OE#	Output enable input
Vcc	Power supply voltage
V _{SS}	Ground
DC	Don't Care *,

^{* :} Logical input level is ignored . However the pin is connected to internal circuit.

FUNCTION TABLE

Mode	CE#	OE#	Vcc	D0 to D7
Read	L	L		Dout
Output disable	L	Н	3.0 V	Hi-Z
Standby	Н	*		Hi-Z

^{*:} Don't Care (H or L)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	Та		0 to 70	°C
Storage temperature	Tstg	_	-55 to 125	°C
Input voltage	VI		-0.5 to V _{CC} +0.5	V
Output voltage	Vo	relative to V _{SS}	-0.5 to V _{CC} +0.5	V
Power supply voltage	V _{CC}		–0.5 to 5	V
Power dissipation per package	P_D	_	1.0	W

RECOMMENDED OPERATING CONDITIONS

 $(Ta = 0 \text{ to } 70^{\circ}C)$

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
V _{CC} power supply voltage	V_{CC}		2.7	_	3.6	٧
Input "H" level	V_{IH}	$V_{CC} = 2.7 \text{ to } 3.6 \text{ V}$	2.2	_	V _{CC} +0.5*	V
Input "L" level	V_{IL}		-0.5**	_	0.6	V

Voltage is relative to V_{SS}.

* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

PIN CAPACITANCE

 $(V_{CC} = 3.0 \text{ V}, \text{ Ta} = 25^{\circ}\text{C}, \text{ f} = 1 \text{ MHz})$

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input	C _{IN1}	V ₁ = 0 V	_	_	8	
DC	C _{IN2}	V ₁ = 0 V	_	_	200	pF
Output	Соит	V _O = 0 V	_	_	10	

^{**: -1.5}V(Min.) when pulse width of undershoot is less than 10ns.

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ELECTRICAL CHARACTERISTICS

DC Characteristics

 $(V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}, \text{ Ta} = 0 \text{ to } 70^{\circ}\text{C})$

(**************************************							
Parameter	Symbol	Condition		Min.	Тур.	Max.	Unit
Input leakage current	ILI	$V_I = 0$ to V_{CC}		_	_	10	μΑ
Output leakage current	I _{LO}	$V_O = 0$ to V_{CC}		_	_	10	μΑ
V _{CC} power supply current	Iccsc	CE# = V _{CC}		_	_	10	μΑ
(Standby)	Iccst	CE# = V _{IH}		_	_	1	mA
V _{CC} power supply current	I _{CCA1}	CE# = V _{IL}	tc = 100 ns	_	_	25	mA
(Read)	I _{CCA2}	OE# = V _{IH}	tc = 200 ns	_	_	20	mA
Input "H" level	V _{IH}	_		2.2	_	V _{CC} +0.5*	V
Input "L" level	V _{IL}	_		-0.5**	_	0.6	V
Output "H" level	V _{OH}	I _{OH} = −1 mA		2.4	_	_	V
Output "L" level	V _{OL}	I _{OL} =	: 2 mA	_	_	0.4	V

Voltage is relative to V_{SS} .

- * : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.
- **: -1.5V(Min.) when pulse width of undershoot is less than 10ns

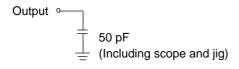
AC Characteristics

 $(V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}, \text{ Ta} = 0 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t _C	_	100	_	ns
Address access time	t _{ACC}	CE# = OE# = V _{IL}	_	100	ns
CE# access time	t _{CE}	OE# = V _{IL}	_	100	ns
OE# access time	t _{OE}	CE #= V _{IL}	_	40	ns
Output disable time	t _{CHZ}	OE# = V _{IL}	0	35	ns
Output disable time	t _{OHZ}	CE# = V _{IL}	0	30	ns
Output hold time	t _{OH}	CE #= OE# = V _{IL}	0	_	ns

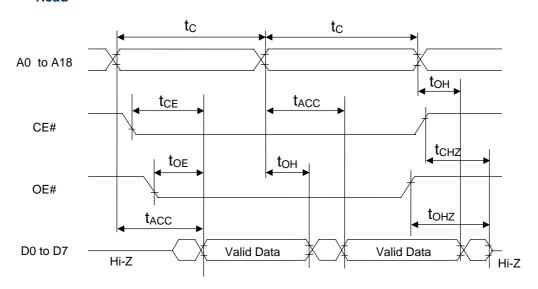
Measurement conditions

Output load



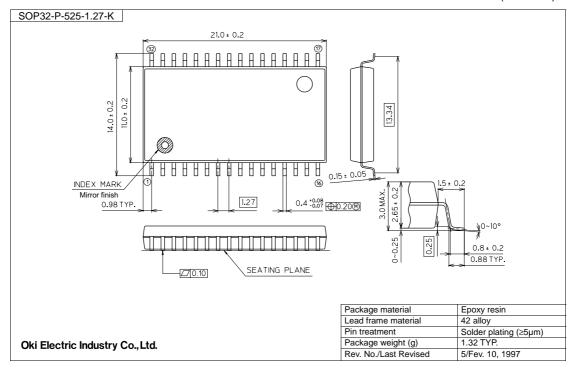
TIMING CHART (READ CYCLE)

Read



PACKAGE DIMENSIONS

(Unit: mm)

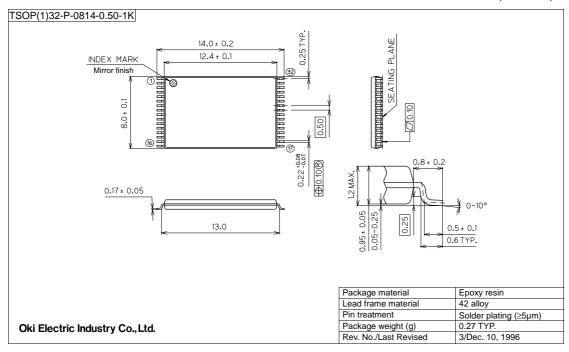


Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)



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REVISION HISTORY

Document	ocument		ige		
No.	Date	Previous Edition	Current Edition	Description	
FEDR27T401E-02-01	Apr. 17, 2002	-	-	Final edition 1	

NOTICE

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