



THIS SPEC IS OBSOLETE

Spec No: 38-07131

Spec Title: CY26187-2 Broadcom Reference Design Clock Generator

Sunset Owner: RGL

Replaced by: NA



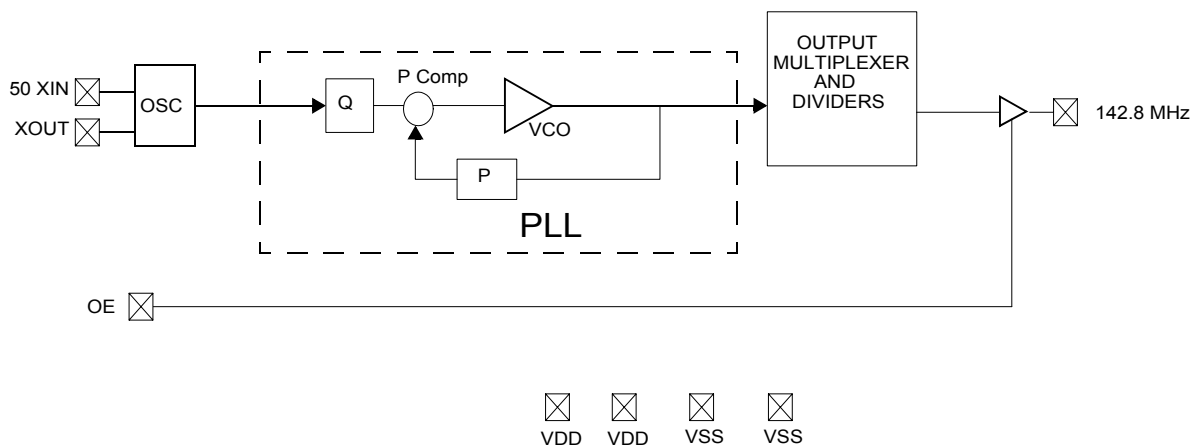
**CY26187-2**

## Broadcom Reference Design Clock Generator

| Features                                      | Benefits                                                     |
|-----------------------------------------------|--------------------------------------------------------------|
| • Integrated phase-locked loop                | Highest Performance PLL tailored for multimedia applications |
| • Low skew, low jitter, high accuracy outputs | Meets critical timing requirements in complex system designs |
| • 3.3V Operation                              |                                                              |

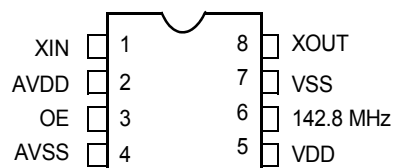
| Part Number | Outputs | Broadcom Reference Design | Input Frequency | Output Frequencies         |
|-------------|---------|---------------------------|-----------------|----------------------------|
| CY26187-2   | 1       | BCM5680_5404              | 50 MHz          | 1 copy of 142.8 MHz (3.3V) |

### Logic Block Diagram



### Pin Configuration

#### CY26187 8-pin SOIC



## Summary

| Name                | Pin Number | Description                 |
|---------------------|------------|-----------------------------|
| XIN <sup>[1]</sup>  | 1          | Reference Crystal Input     |
| AVDD                | 2          | Analog Voltage Supply       |
| OE                  | 3          | Output enable (0-off; 1-on) |
| AVSS                | 4          | Ground                      |
| VDD                 | 5          | Voltage Supply              |
| 142.8 MHz           | 6          | 142.8-MHz clock output      |
| VSS                 | 7          | Ground                      |
| XOUT <sup>[1]</sup> | 8          | Reference Crystal Output    |

## Absolute Maximum Conditions

| Parameter       | Description                                 | Min.                  | Max.                  | Unit |
|-----------------|---------------------------------------------|-----------------------|-----------------------|------|
| V <sub>DD</sub> | Supply Voltage                              |                       | 7.0                   | V    |
| T <sub>S</sub>  | Storage Temperature <sup>[2]</sup>          | -65                   | 125                   | °C   |
| T <sub>J</sub>  | Junction Temperature                        |                       | 125                   | °C   |
|                 | Digital Inputs                              | V <sub>SS</sub> - 0.3 | V <sub>DD</sub> + 0.3 | V    |
|                 | Digital Outputs referred to V <sub>DD</sub> | V <sub>SS</sub> - 0.3 | V <sub>DD</sub> + 0.3 | V    |
|                 | Electro-Static Discharge                    | 2                     |                       | kV   |

## Recommended Operating Conditions

| Parameter         | Description                                                                                    | Min.  | Typ. | Max.  | Unit |
|-------------------|------------------------------------------------------------------------------------------------|-------|------|-------|------|
| V <sub>DD</sub>   | Operating Voltage                                                                              | 3.135 | 3.3  | 3.465 | V    |
| T <sub>A</sub>    | Ambient Temperature                                                                            | 0     |      | 70    | °C   |
| C <sub>LOAD</sub> | Max. Load Capacitance                                                                          |       |      | 15    | pF   |
| P <sub>max</sub>  | Max. Output Power Dissipation, 8-pin package                                                   |       |      | 150   | mW   |
| f <sub>REF</sub>  | Reference Frequency                                                                            |       | 50   |       | MHz  |
| t <sub>PU</sub>   | Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic) | 0.05  |      | 500   | ms   |

## DC Electrical Characteristics

| Parameter | Name                  | Description                                                     | Min. | Typ. | Max. | Unit |
|-----------|-----------------------|-----------------------------------------------------------------|------|------|------|------|
|           | Output High Current   | V <sub>OH</sub> = V <sub>DD</sub> - 0.5, V <sub>DD</sub> = 3.3V | 12   | 24   |      | mA   |
|           | Output Low Current    | V <sub>OL</sub> = 0.5, V <sub>DD</sub> = 3.3V                   | 12   | 24   |      | mA   |
|           | Input Capacitance     |                                                                 |      |      | 7    | pF   |
|           | Input Leakage Current |                                                                 |      | 5    |      | μA   |
|           | I <sub>VDD</sub>      | 3.3V, All outputs @ 10 MHz                                      |      |      | 35   | mA   |

### Notes:

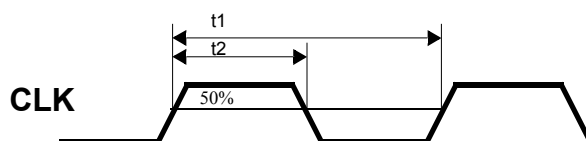
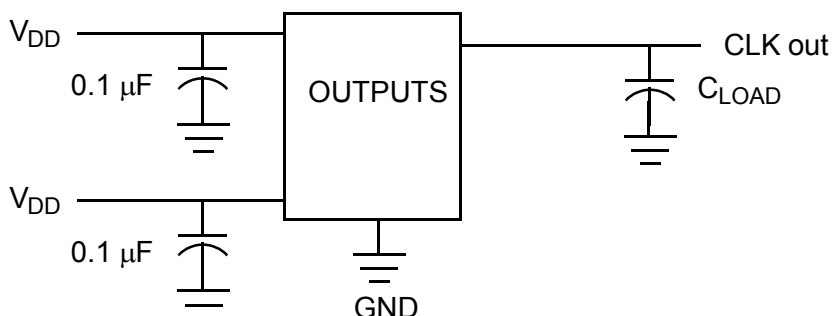
1. Float XOUT pin if XIN is driven by reference clock (as opposed to crystal).
2. Rated for 10 years.

**AC Electrical Characteristics (VDD = 3.3V) <sup>(3.)</sup>**

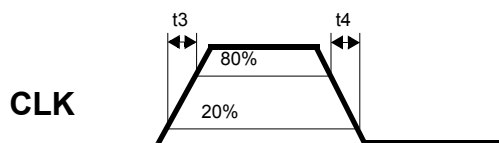
| Parameter | Name                   | Description                                                       | Min. | Typ. | Max. | Unit |
|-----------|------------------------|-------------------------------------------------------------------|------|------|------|------|
|           | Output Duty Cycle      | Duty Cycle is defined in <i>Figure 1</i> , 50% of V <sub>DD</sub> | 45   | 50   | 55   | %    |
| t3        | Rising Edge Slew Rate  | Output Clock Rise Time, 20%-80% of V <sub>DD</sub>                | 0.8  | 1.4  |      | V/ns |
| t4        | Falling Edge Slew Rate | Output Clock Fall Time, 80% to 20% of V <sub>DD</sub>             | 0.8  | 1.4  |      | V/ns |
| t9        | Clock Jitter           | Peak to Peak period jitter                                        |      |      | 200  | ps   |
| t10       | PLL Lock Time          |                                                                   |      |      | 3    | ms   |

**Note:**

3. Not 100% tested.

**Test Circuit**


**Figure 1. Duty Cycle Definition; DC = t<sub>2</sub>/t<sub>1</sub>.**



**Figure 2. Rise and Fall Time Definitions.**

**Ordering Information**

| Ordering Code | Package Name | Package Type | Operating Range | Operating Voltage |
|---------------|--------------|--------------|-----------------|-------------------|
| CY26187SC-2   | S8           | 8-Pin SOIC   | Commercial      | 3.3V              |



**Revision History**

| Document Title: CY26187-2 Broadcom Reference Design Clock Generator<br>Document Number: 38-07131 |         |            |                 |                                                                 |
|--------------------------------------------------------------------------------------------------|---------|------------|-----------------|-----------------------------------------------------------------|
| REV.                                                                                             | ECN NO. | Issue Date | Orig. of Change | Description of Change                                           |
| **                                                                                               | 110096  | 02/19/02   | CKN             | New data sheet                                                  |
| *A                                                                                               | 121872  | 12/14/02   | RBI             | Power up requirements added to Operating Conditions Information |
| OBS                                                                                              | 294822  | See ECN    | RGL             | TO Obsolete the DS                                              |