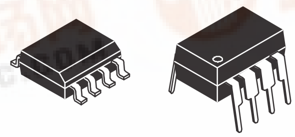


SN65HVD05, SN65HVD06
SN75HVD05, SN65HVD07
SN75HVD06, SN75HVD07

SLLS533D – MAY 2002 – REVISED JULY 2006

HIGH OUTPUT RS-485 TRANSCEIVERS

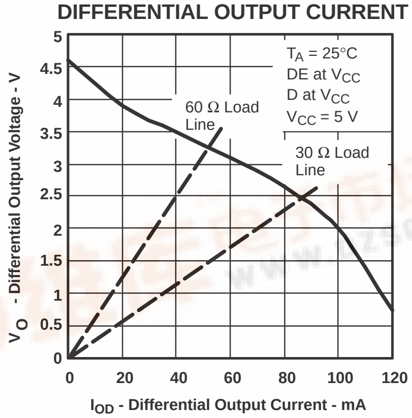
FEATURES

- **Minimum Differential Output Voltage of 2.5 V Into a 54-Ω Load**
- **Open-Circuit, Short-Circuit, and Idle-Bus Failsafe Receiver**
- **1/8th Unit-Load Option Available (Up to 256 Nodes on the Bus)**
- **Bus-Pin ESD Protection Exceeds 16 kV HBM**
- **Driver Output Slew Rate Control Options**
- **Electrically Compatible With ANSI TIA/EIA-485-A Standard**
- **Low-Current Standby Mode . . . 1 μA Typical**
- **Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications**
- **Pin Compatible With Industry Standard SN75176**

APPLICATIONS

- **Data Transmission Over Long or Lossy Lines or Electrically Noisy Environments**
- **Profibus Line Interface**
- **Industrial Process Control Networks**
- **Point-of-Sale (POS) Networks**
- **Electric Utility Metering**
- **Building Automation**
- **Digital Motor Control**

DIFFERENTIAL OUTPUT VOLTAGE
vs
DIFFERENTIAL OUTPUT CURRENT

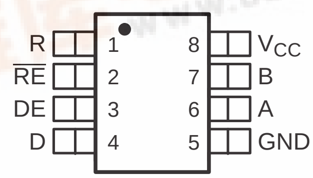


DESCRIPTION

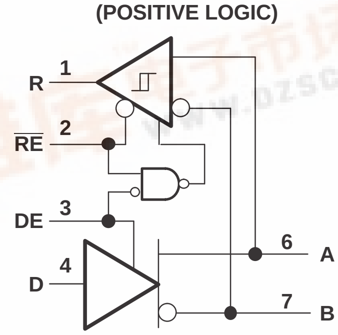
The SN65HVD05, SN75HVD05, SN65HVD06, SN75HVD06, SN65HVD07, and SN75HVD07 combine a 3-state differential line driver and differential line receiver. They are designed for balanced data transmission and interoperate with ANSI TIA/EIA-485-A and ISO 8482E standard-compliant devices. The driver is designed to provide a differential output voltage greater than that required by these standards for increased noise margin. The drivers and receivers have active-high and active-low enables respectively, which can be externally connected together to function as direction control.

The driver differential outputs and receiver differential inputs connect internally to form a differential input/ output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or not powered. These devices feature wide positive and negative common-mode voltage ranges, making them suitable for party-line applications.

D OR P PACKAGE
(TOP VIEW)



LOGIC DIAGRAM
(POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

SIGNALING RATE	UNIT LOAD	DRIVER OUTPUT SLOPE CONTROL	T_A	PART NUMBER(2)		MARKED AS: PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	MARKED AS: SMALL OUTLINE IC (SOIC) PACKAGE
40 Mbps	1/2	No	40°C to 85°C	SN65HVD05D	SN65HVD05P	65HVD05	VP05
10 Mbps	1/8	Yes		SN65HVD06D	SN65HVD06P	65HVD06	VP06
1 Mbps	1/8	Yes		SN65HVD07D	SN65HVD07P	65HVD07	VP07
40 Mbps	1/2	No	0°C to 70°C	SN75HVD05D	SN75HVD05P	75HVD05	VN05
10 Mbps	1/8	Yes		SN75HVD06D	SN75HVD06P	75HVD06	VN06
1 Mbps	1/8	Yes		SN75HVD07D	SN75HVD07P	75HVD07	VN07

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The D package is available taped and reeled. Add an R suffix to the device type (i.e., SN65HVD05DR).

PACKAGE DISSIPATION RATINGS

(See Figure 12 and Figure 13)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D(2)	710 mW	5.7 mW/°C	455 mW	369 mW
D(3)	1282 mW	10.3 mW/°C	821 mW	667 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3
(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)(2)

			SN65HVD05, SN65HVD06, SN65HVD07 SN75HVD05, SN75HVD06, SN75HVD07
Supply voltage range, V_{CC}			-0.3 V to 6 V
Voltage range at A or B			-9 V to 14 V
Input voltage range at D, DE, R or $\overline{RE}$			-0.5 V to V_{CC} + 0.5 V
Voltage input range, transient pulse, A and B, through 100 Ω (see Figure 11)			-50 V to 50 V
Receiver output current, I_O			–11 mA to 11mA
Electrostatic discharge	Human body model(3)	A, B, and GND	16 kV
		All pins	4 kV
	Charged-device model(4)	All pins	1 kV
Continuous total power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under "absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under" recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		5.5	V
Voltage at any bus terminal (separately or common mode) V_I or V_{IC}		-7[1]		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Figure 7)		-12		12	V
High-level output current, I_{OH}	Driver	-100			mA
	Receiver	-8			
Low-level output current, I_{OL}	Driver			100	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65HVD05	-40		85	°C
	SN65HVD06				
	SN65HVD07				
	SN75HVD05	0		70	°C
	SN75HVD06				
	SN75HVD07				

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

DRIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = -18 mA		-1.5			V
$\|V_{OD}\|$	Differential output voltage		No Load				V_{CC}	V
			R_L = 54 Ω, See Figure 4		2.5			
			V_{test} = -7 V to 12 V, See Figure 2		2.2			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage		See Figure 4 and Figure 2		-0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 3		2.2		3.3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				-0.1		0.1	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	HVD05	See Figure 3			600		mV
		HVD06				500		
		HVD07				900		
I_{OZ}	High-impedance output current		See receiver input currents					
I_I	Input current	D			-100		0	μA
		DE			0		100	
I_{OS}	Short-circuit output current		-7 V ≤ V_O ≤ 12 V		-250		250	mA
$C_{(diff)}$	Differential output capacitance		V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			16		pF
I_{CC}	Supply current		$\overline{RE}$ at V_{CC}, D & DE at V_{CC}, No load	Receiver disabled and driver enabled		9	15	mA
			$\overline{RE}$ at V_{CC}, D at V_{CC} DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	μA
			$\overline{RE}$ at 0 V, D & DE at V_{CC}, No load	Receiver enabled and driver enabled		9	15	mA

(1) All typical values are at 25°C and with a 5-V supply.

DRIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD05	R_L = 54 Ω, C_L = 50 pF, See Figure 4		6.5	11	ns
		HVD06			27	40	
		HVD07			250	400	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD05			6.5	11	ns
		HVD06			27	40	
		HVD07			250	400	
t_r	Differential output signal rise time	HVD05		2.7	3.6	6	ns
		HVD06		18	28	55	
		HVD07		150	300	450	
t_f	Differential output signal fall time	HVD05		2.7	3.6	6	ns
		HVD06		18	28	55	
		HVD07		150	300	450	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD05				2	ns
		HVD06				2.5	
		HVD07				10	
$t_{sk(pp)}$[(2)]	Part-to-part skew	HVD05				3.5	ns
		HVD06				14	
		HVD07				100	
t_{PZH1}	Propagation delay time, high-impedance-to-high-level output	HVD05	$\overline{RE}$ at 0 V, R_L = 110 Ω, See Figure 5			25	ns
		HVD06				45	
		HVD07				250	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD05				25	ns
		HVD06				60	
		HVD07				250	
t_{PZL1}	Propagation delay time, high-impedance-to-low-level output	HVD05	$\overline{RE}$ at 0 V, R_L = 110 Ω, See Figure 6			15	ns
		HVD06				45	
		HVD07				200	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD05				14	ns
		HVD06				90	
		HVD07				550	
t_{PZH2}	Propagation delay time, standby-to-high-level output		R_L = 110Ω , $\overline{RE}$ at 3 V, See Figure 5			6	µs
t_{PZL2}	Propagation delay time, standby-to-low-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, See Figure 6			6	µs

(1) All typical values are at 25°C and with a 5-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS			MIN	TYP (1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		I_O = -8 mA					0.01	V
V_{IT-}	Negative-going input threshold voltage		I_O = 8 mA			-0.2			V
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})						35		mV
V_{IK}	Enable-input clamp voltage		I_I = -18 mA			-1.5			V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = -8 mA,	See Figure 7	4			V
V_{OL}	Low-level output voltage		V_{ID} = -200 mV,	I_{OL} = 8 mA,	See Figure 7			0.4	V
I_{OZ}	High-impedance-state output current		V_O = 0 or V_{CC}	$\overline{RE}$ at V_{CC}		-1		1	µA
I_I	Bus input current	HVD05	Other inputat 0 V	V_A or V_B = 12 V			0.23	0.5	mA
				V_A or V_B = 12 V,	V_{CC} = 0 V		0.3	0.5	
				V_A or V_B = -7 V		-0.4	0.13		
				V_A or V_B = -7 V,	V_{CC} = 0 V	-0.4	0.15		
		HVD06 HVD07	Other inputat 0 V	V_A or V_B = 12 V			0.06	0.1	mA
				V_A or V_B = 12 V,	V_{CC} = 0 V		0.08	0.13	
				V_A or V_B = -7 V		-0.1	0.05		
				V_A or V_B = -7 V,	V_{CC} = 0 V	-0.05	0.03		
I_{IH}	High-level input current, $\overline{RE}$		V_{IH} = 2 V			-60	26.4		µA
I_{IL}	Low-level input current, $\overline{RE}$		V_{IL} = 0.8 V			-60	27.4		µA
$C_{(diff)}$	Differential input capacitance		V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V				16		pF
I_{CC}	Supply current		$\overline{RE}$ at 0 V, D & DE at 0 V, No load	Receiver enabled and driver disabled			5	10	mA
			$\overline{RE}$ at V_{CC}, DE at 0 V, D at V_{CC}, No load	Receiver disabled and driver disabled (standby)			1	5	µA
			$\overline{RE}$ at 0 V, D & DE at V_{CC}, No load	Receiver enabled and driver enabled			9	15	mA

(1) All typical values are at 25°C and with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output 1/2 UL	HVD05	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, See Figure 8		14.6	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output 1/2 UL	HVD05			14.6	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output 1/8 UL	HVD06			55	70	ns
		HVD07			55	70	
t_{PHL}	Propagation delay time, high-to-low-level output 1/8 UL	HVD06			55	70	ns
		HVD07			55	70	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL}$ - $t_{PLH}\rvert$)	HVD05				2	ns
		HVD06				4.5	
		HVD07				4.5	
$t_{sk(pp)}$[(2)]	Part-to-part skew	HVD05				6.5	ns
		HVD06				14	
		HVD07				14	
t_r	Output signal rise time		C_L = 15 pF, See Figure 8		2	3	ns
t_f	Output signal fall time				2	3	
t_{PZH1}	Output enable time to high level		C_L = 15 pF, DE at 3 V, See Figure 9			10	ns
t_{PZL1}	Output enable time to low level					10	
t_{PHZ}	Output disable time from high level					15	
t_{PLZ}	Output disable time from low level					15	
t_{PZH2}	Propagation delay time, standby-to-high-level output		C_L = 15 pF, DE at 0, See Figure 10			6	µs
t_{PZL2}	Propagation delay time, standby-to-low-level output					6	

(1) All typical values are at 25°C and with a 5-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

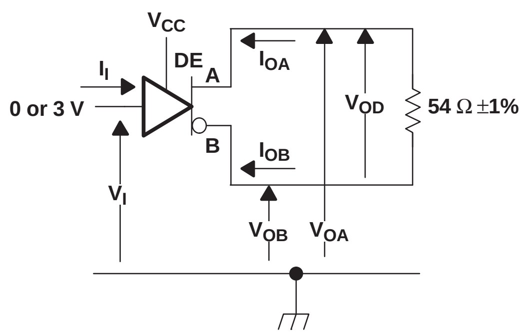


Figure 1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

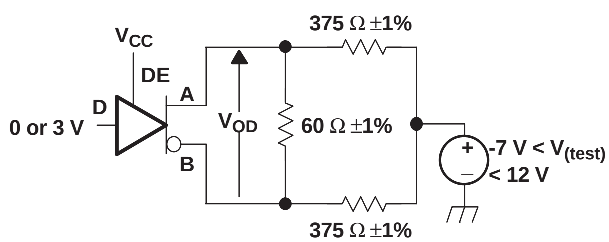
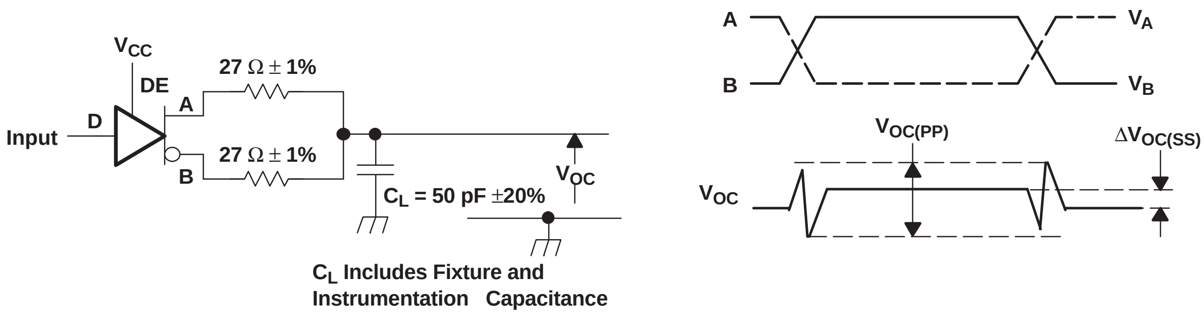


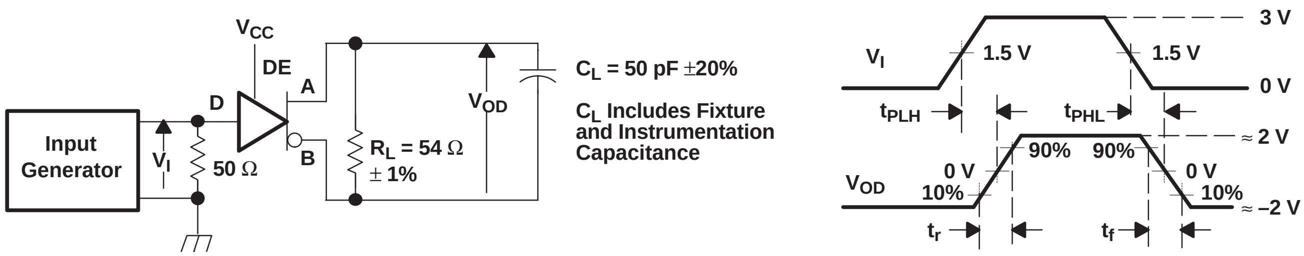
Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



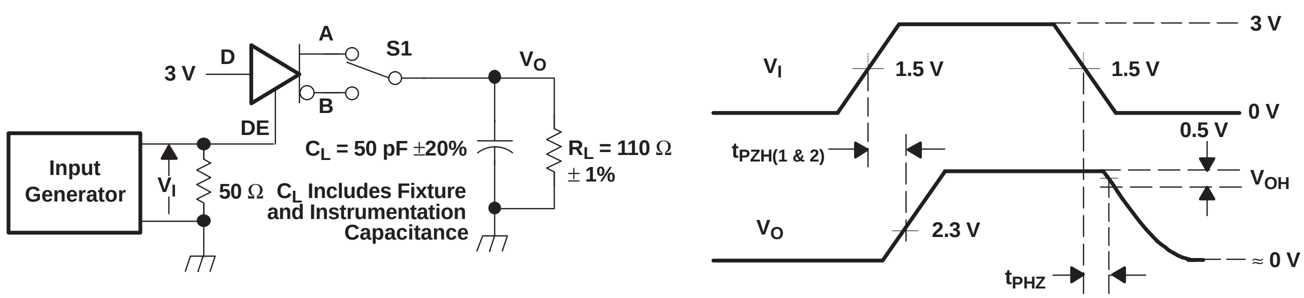
Input: PRR = 500 kHz, 50% Duty Cycle, t_r<6ns, t_f<6ns, Z_O = 50 Ω

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



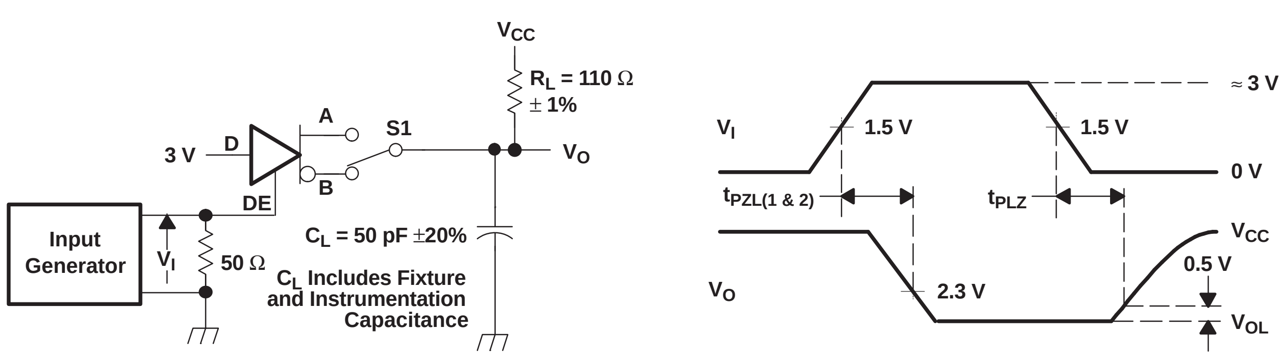
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 4. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

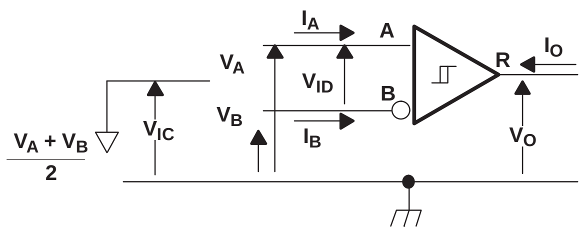


Figure 7. Receiver Voltage and Current Definitions

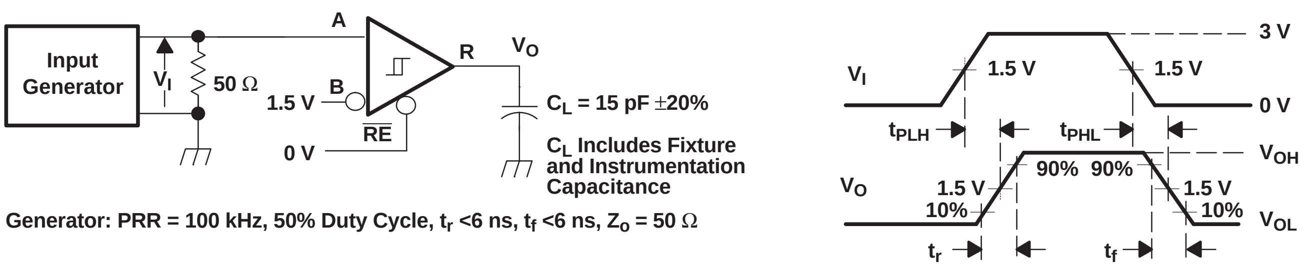


Figure 8. Receiver Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

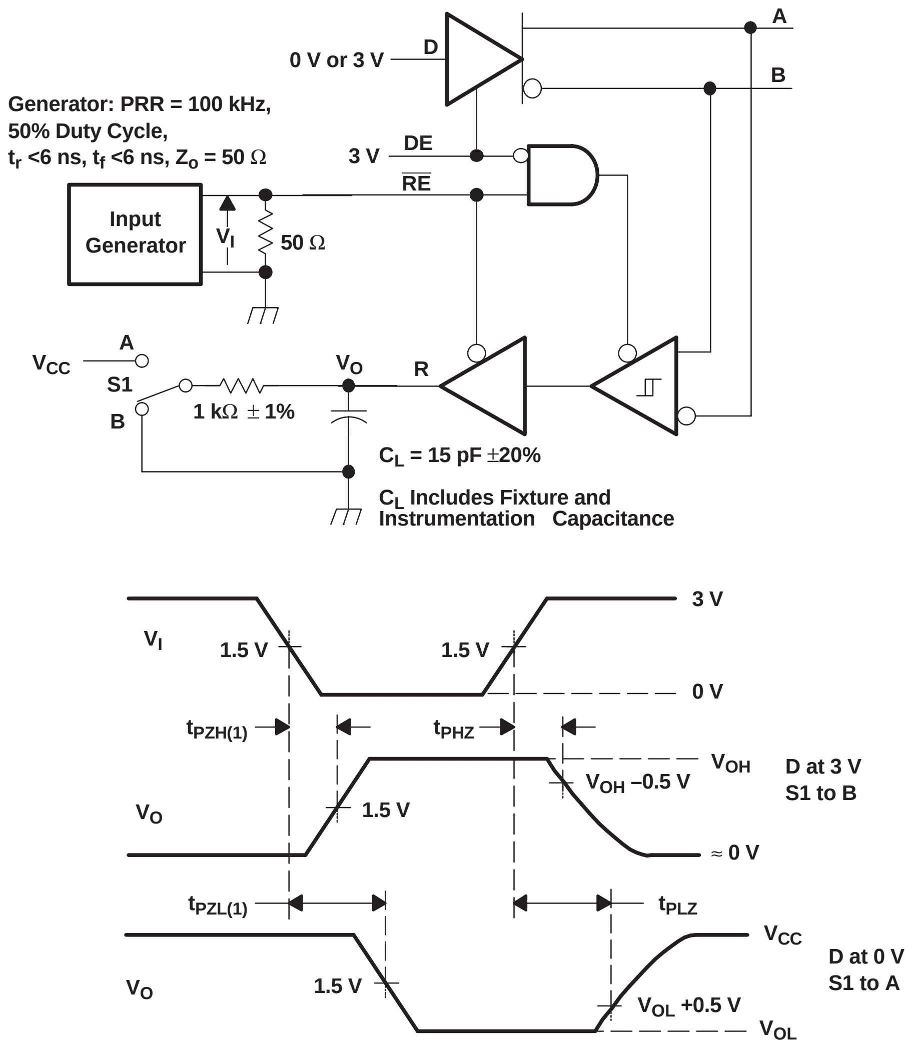


Figure 9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

PARAMETER MEASUREMENT INFORMATION (continued)

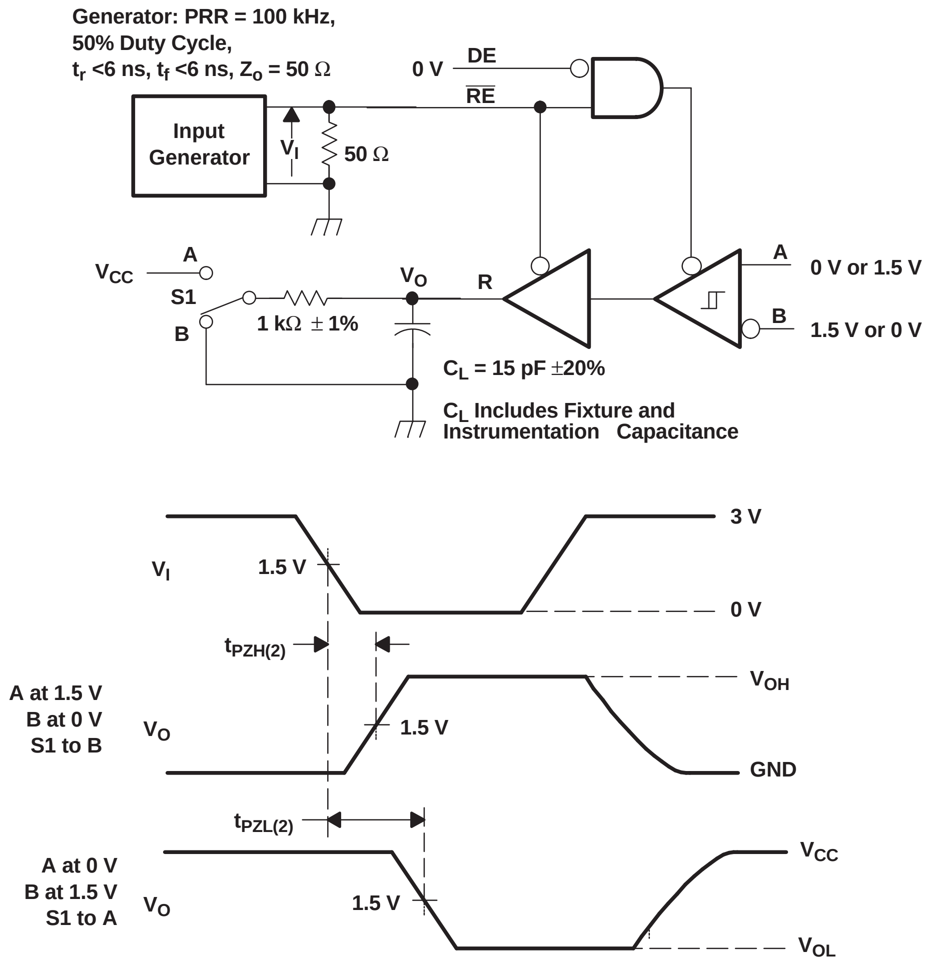
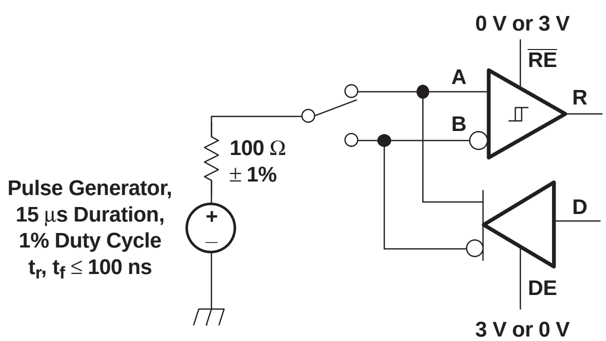


Figure 10. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 11. Test Circuit, Transient Over Voltage Test

FUNCTION TABLES

DRIVER

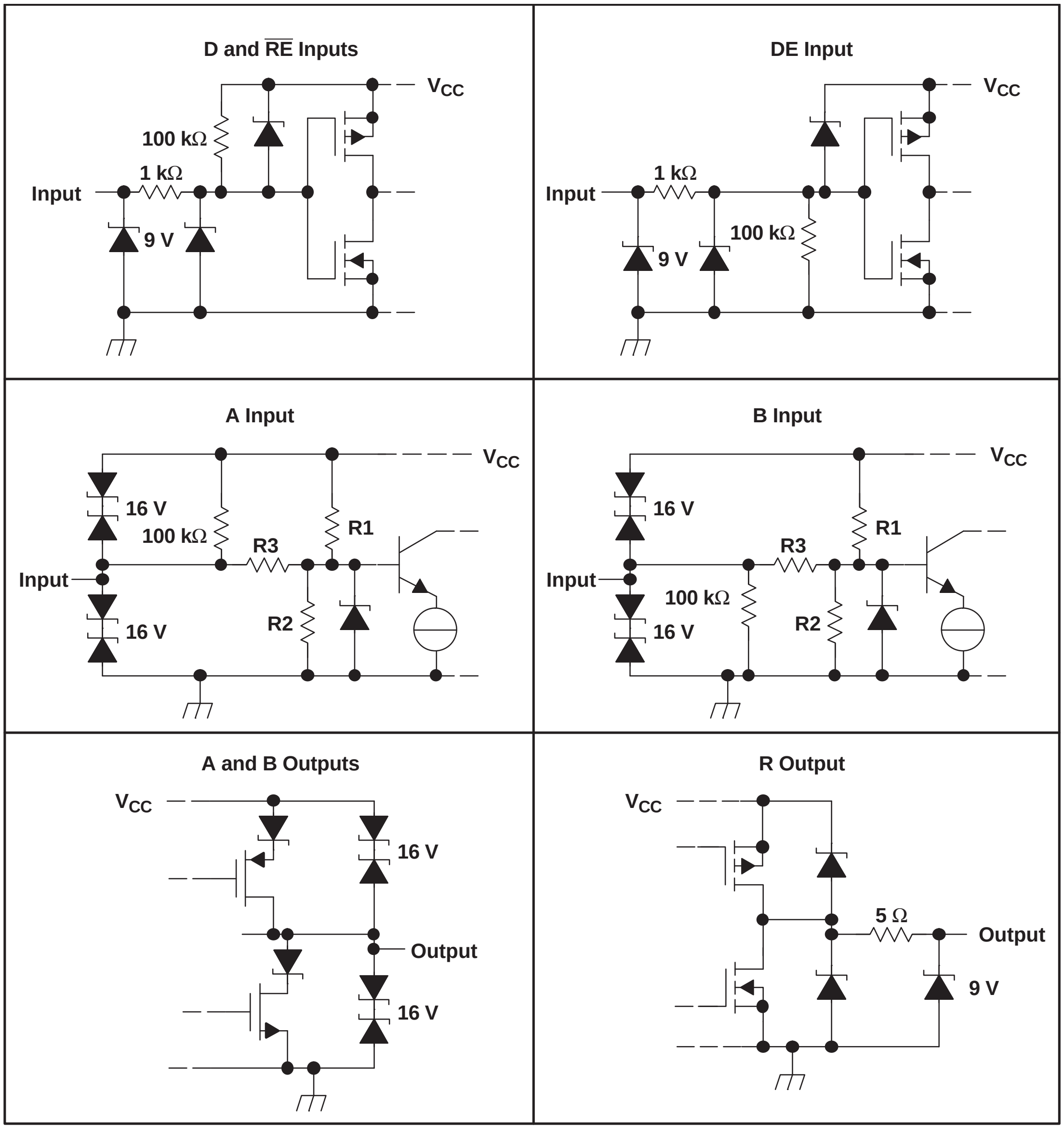
INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L
X	Open	Z	Z

RECEIVER(1)

DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \le -0.2$ V	L	L
$-0.2\ V < V_{ID} < -0.01$ V	L	?
$-0.01\ V \le V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short Circuit	L	H
X	Open	Z

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD05	9 kΩ	45 kΩ
SN65HVD06	36 kΩ	180 kΩ
SN65HVD07	36 kΩ	180 kΩ

TYPICAL CHARACTERISTICS

HVD05
MAXIMUM RECOMMENDED STILL-AIR
OPERATING TEMPERATURE
vs
SIGNALING RATE
(D-PACKAGE)

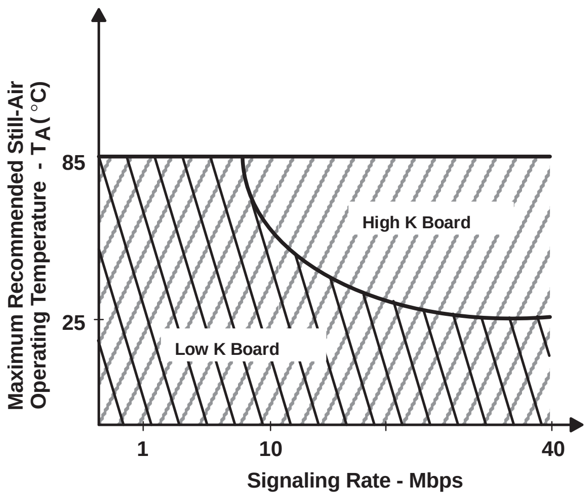


Figure 12.

HVD06
MAXIMUM RECOMMENDED STILL-AIR
OPERATING TEMPERATURE
vs
SIGNALING RATE
(D-PACKAGE)

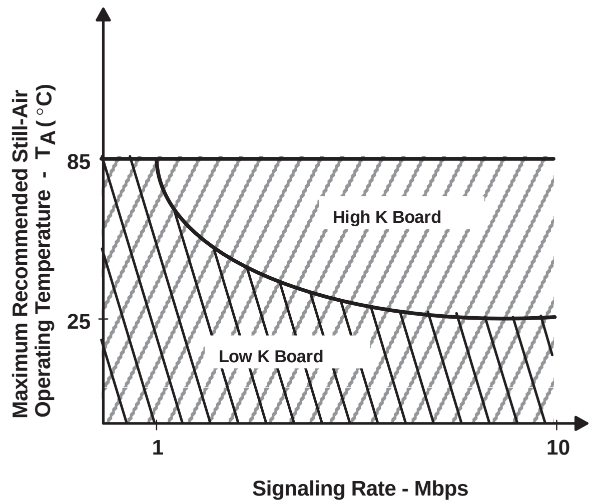


Figure 13.

HVD05
RMS SUPPLY CURRENT
vs
SIGNALILNG RATE

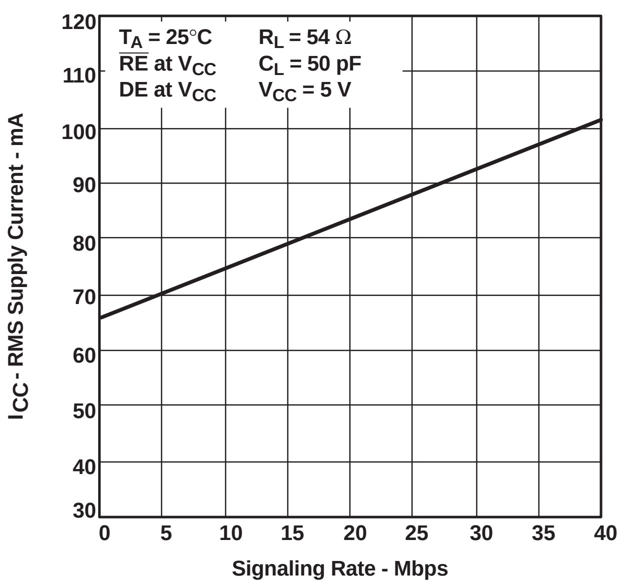


Figure 14.

HVD06
RMS SUPPLY CURRENT
vs
SIGNALING RATE

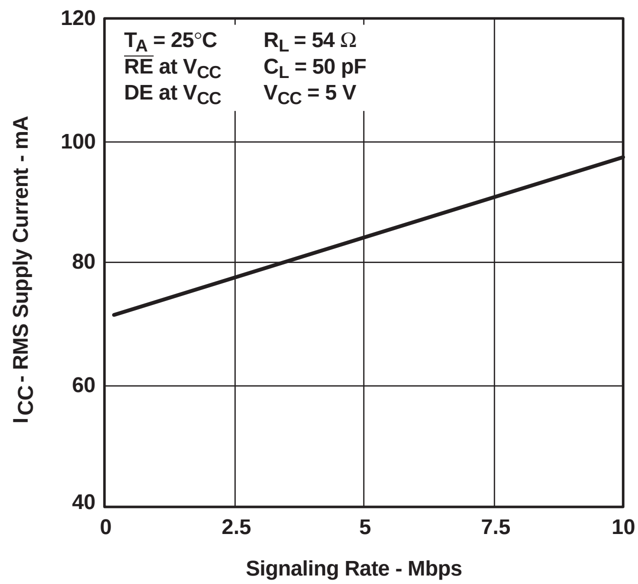


Figure 15.

TYPICAL CHARACTERISTICS (continued)

HVD07
RMS SUPPLY CURRENT
vs
SIGNALING RATE

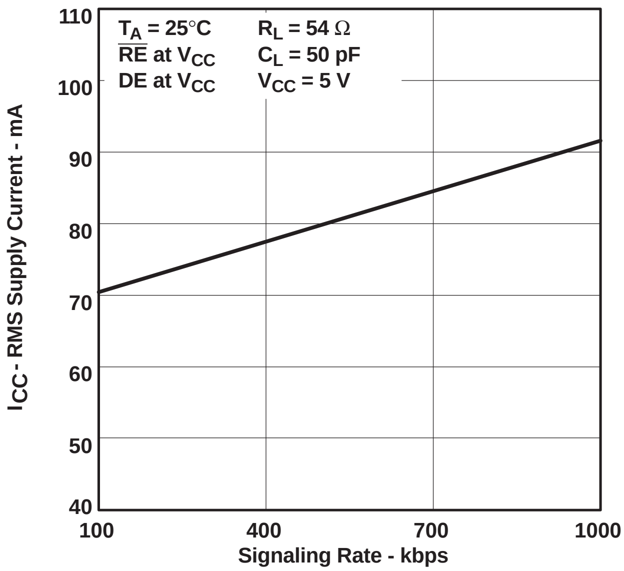


Figure 16.

BUS INPUT CURRENT
vs
BUS INPUT VOLTAGE

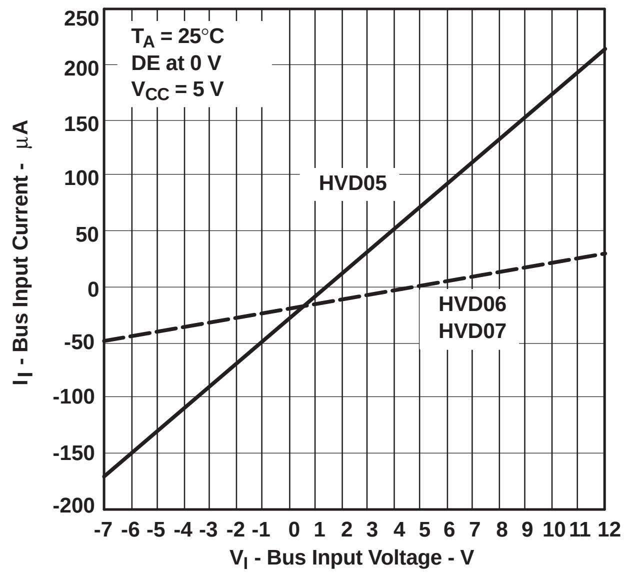


Figure 17.

DRIVER HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

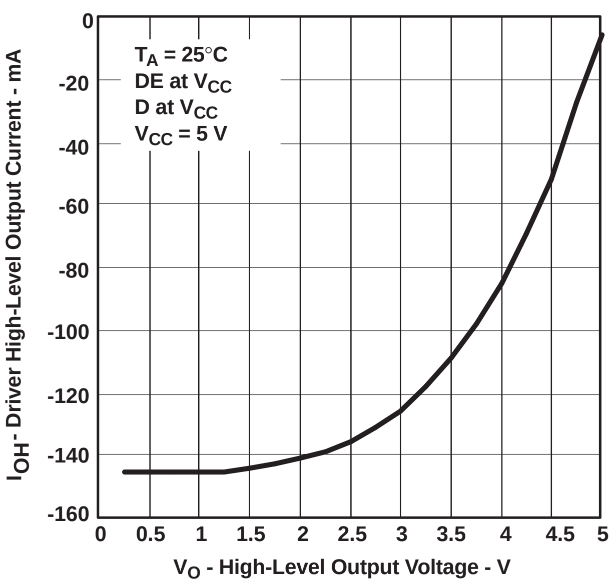


Figure 18.

DRIVER LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

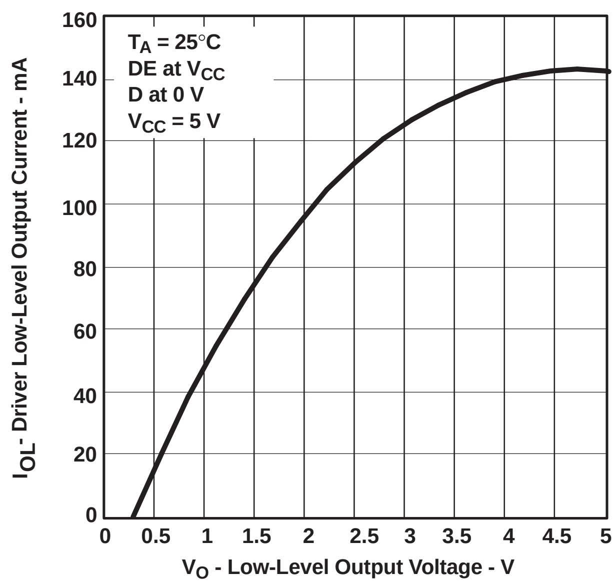


Figure 19.

TYPICAL CHARACTERISTICS (continued)

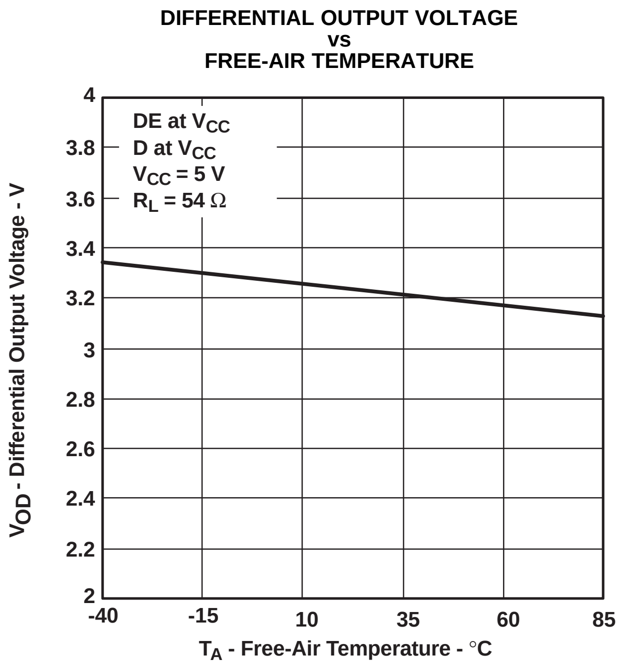


Figure 20.

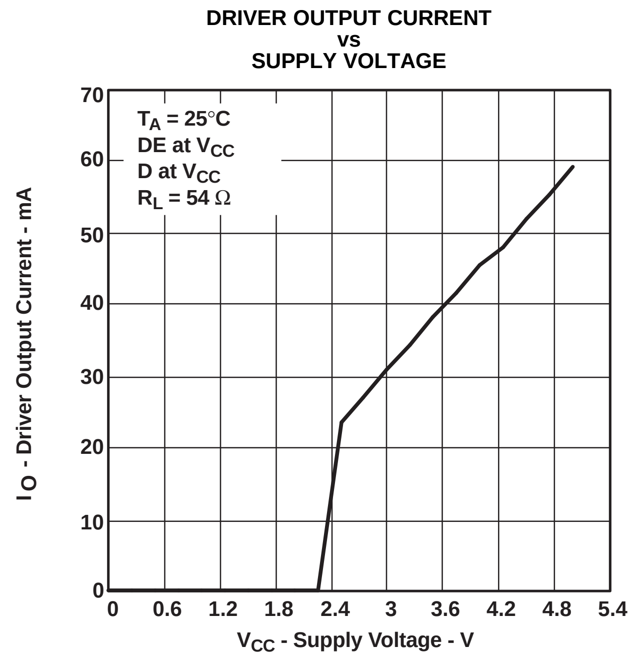


Figure 21.

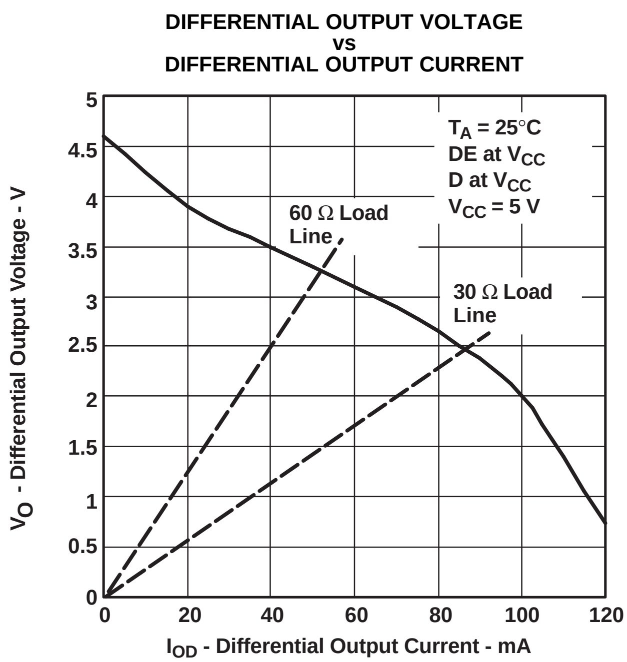


Figure 22.

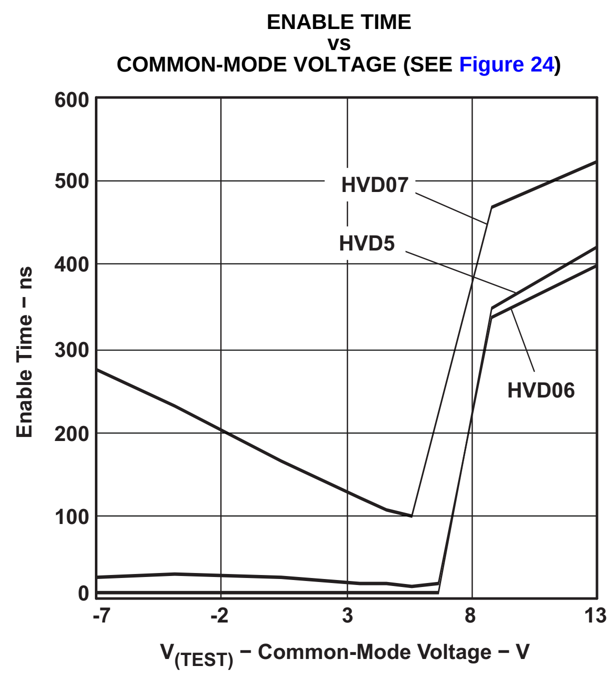


Figure 23.

TYPICAL CHARACTERISTICS (continued)

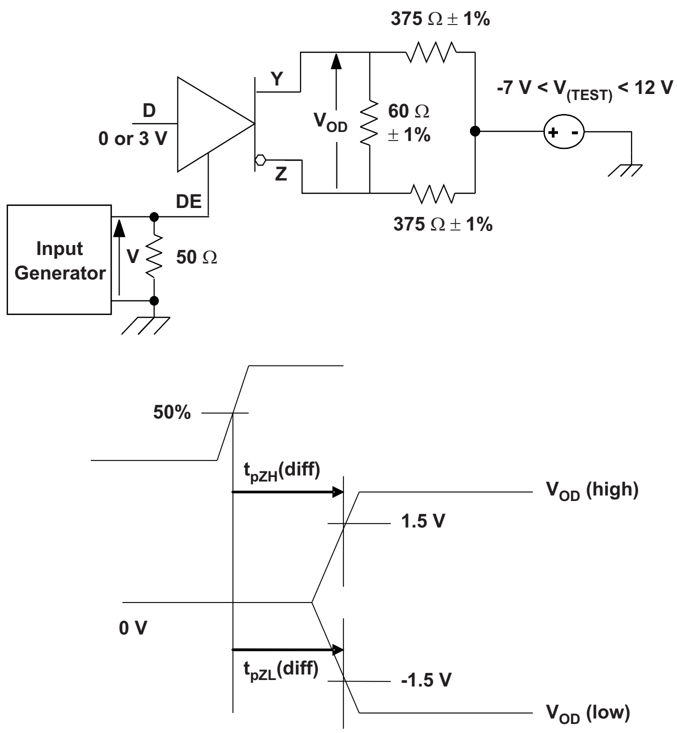
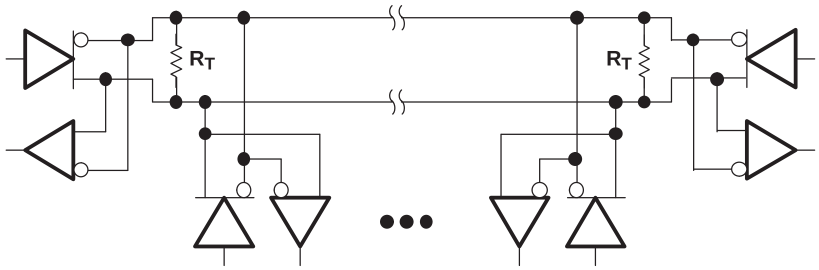


Figure 24. Driver Enable Time From DE to V_{OD}

The time t_{pZL}(x) is the measure from DE to V_{OD}(x). V_{OD} is valid when it is greater than 1.5 V.

APPLICATION INFORMATION



Device	Number of Devices on Bus
HVD05	64
HVD06	256
HVD07	256

NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 25. Typical Application Circuit

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65HVD05D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD05DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD05DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD05DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD05P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD05PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD06D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD06DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD06DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD06DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD06P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD06PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD07D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD07DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD07DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD07DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD07P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD07PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75HVD05D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD05DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD05DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD05DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD05P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75HVD05PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75HVD06D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75HVD06DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD06DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD06DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD06P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75HVD06PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75HVD07D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD07DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD07DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD07DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD07P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75HVD07PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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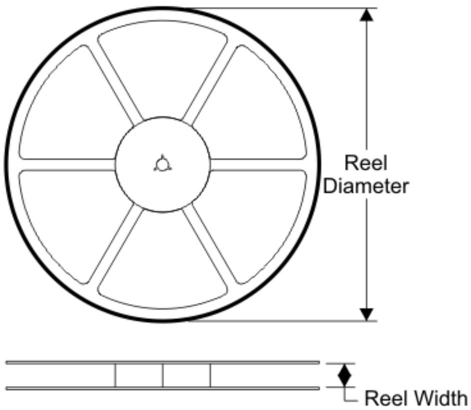
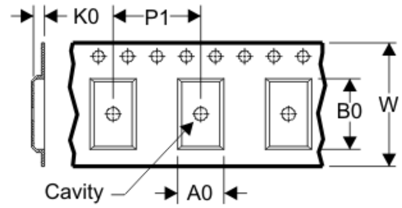
PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

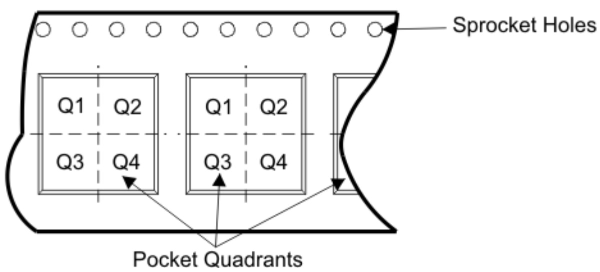


TAPE DIMENSIONS



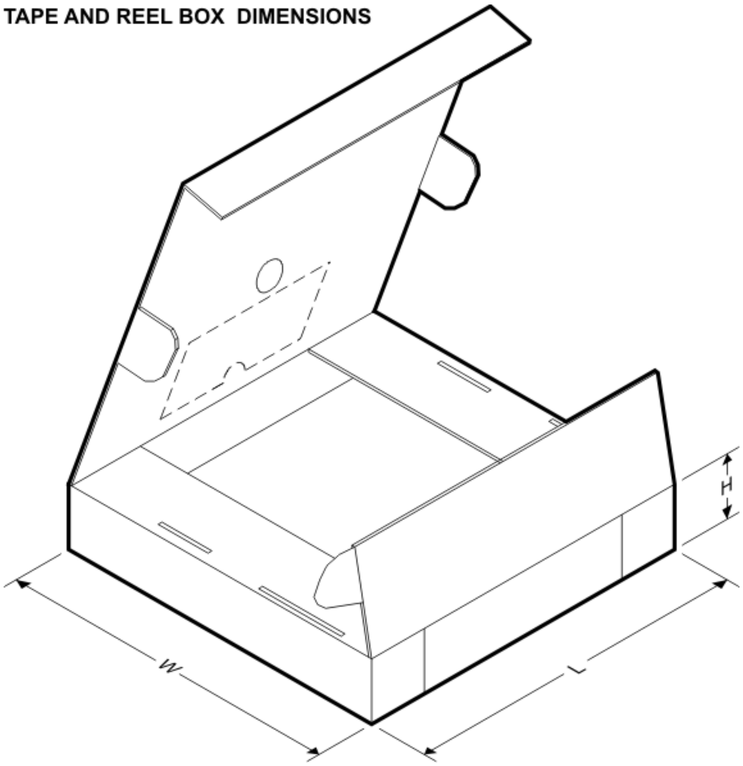
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



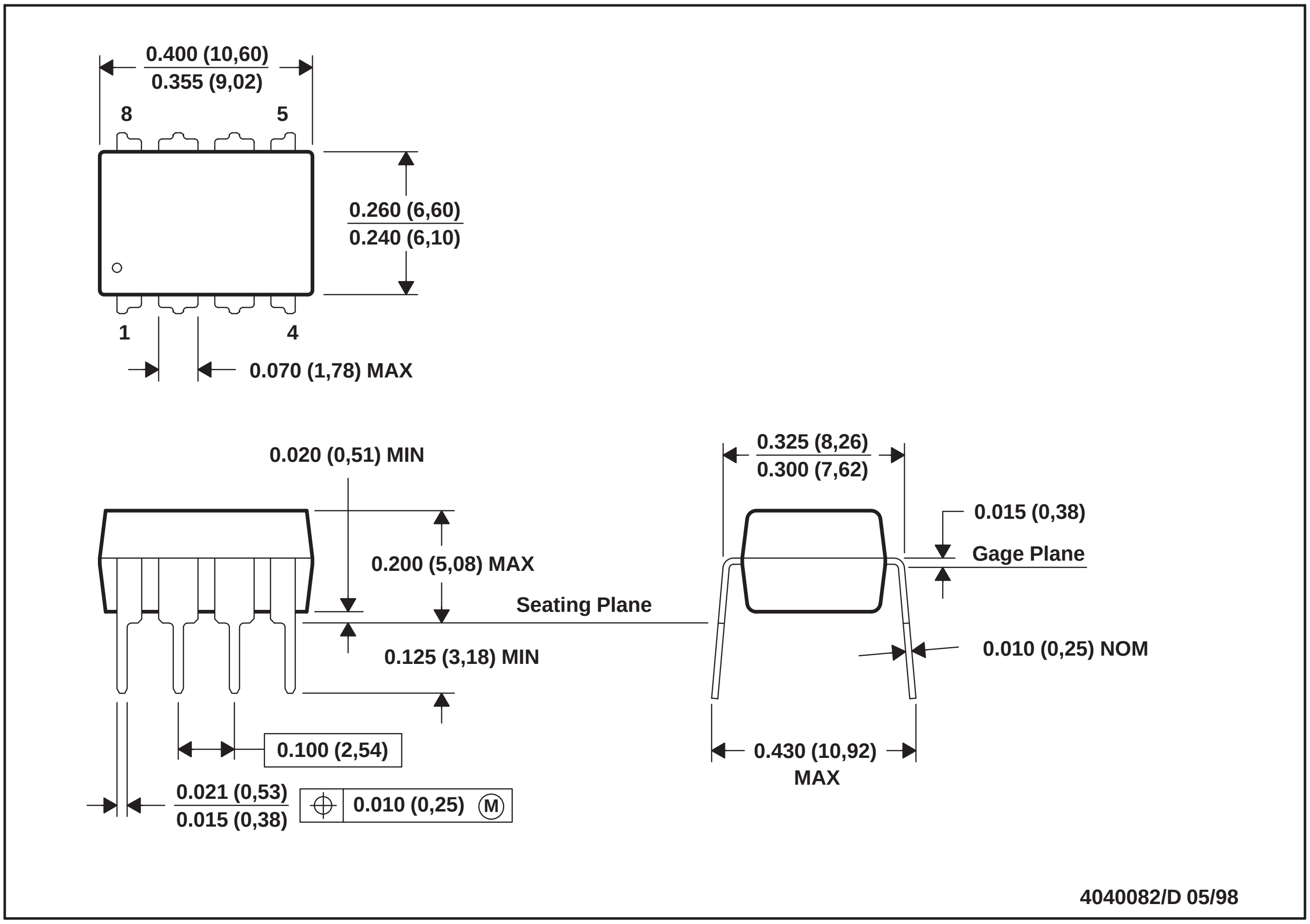
Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD05DR	D	8	SITE 27	330	0	6.4	5.2	2.1	8	12	Q1
SN65HVD06DR	D	8	SITE 27	330	0	6.4	5.2	2.1	8	12	Q1
SN65HVD07DR	D	8	SITE 27	330	0	6.4	5.2	2.1	8	12	Q1
SN75HVD05DR	D	8	SITE 27	330	0	6.4	5.2	2.1	8	12	Q1
SN75HVD06DR	D	8	SITE 27	330	0	6.4	5.2	2.1	8	12	Q1
SN75HVD07DR	D	8	SITE 27	330	0	6.4	5.2	2.1	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



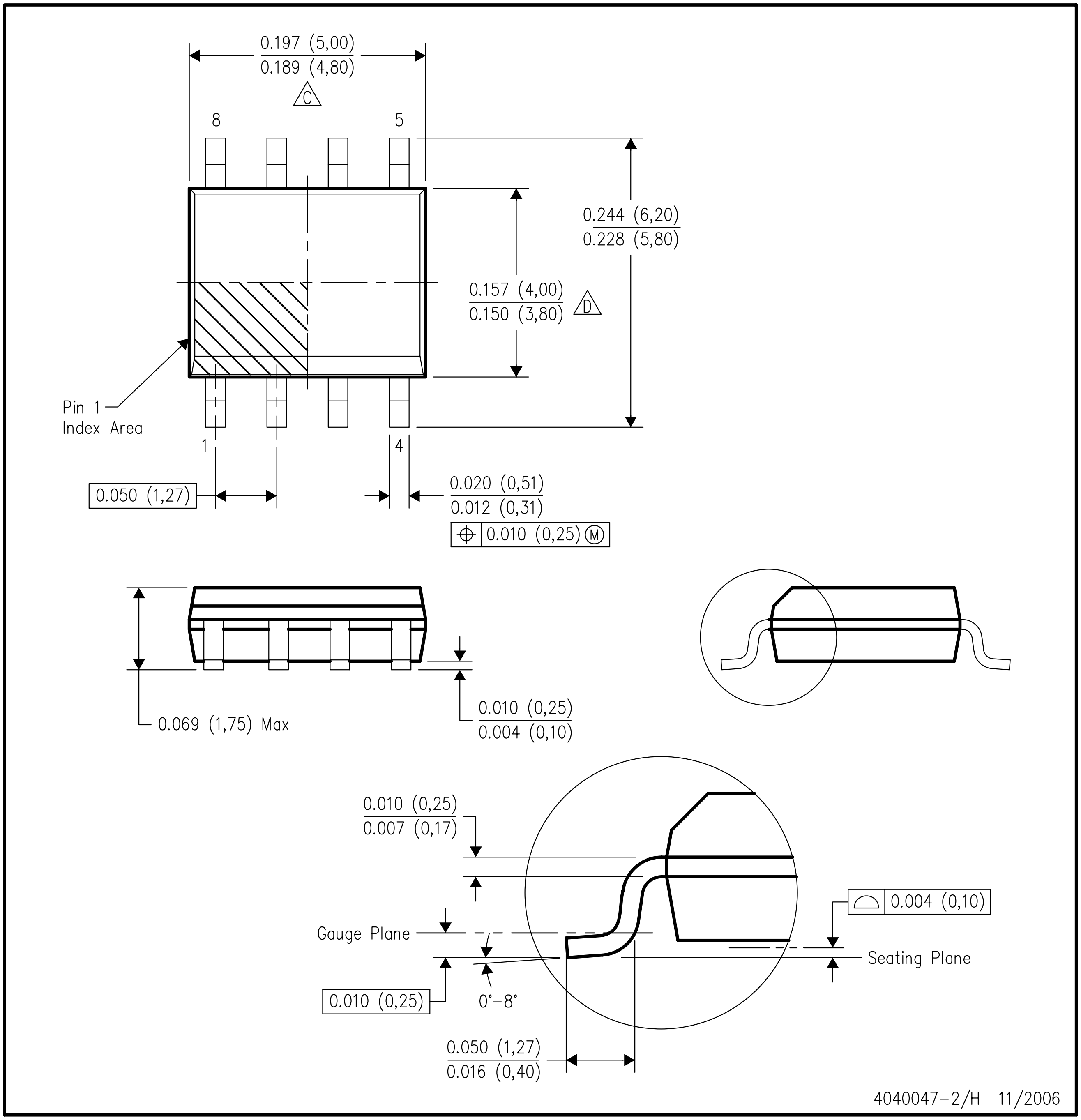
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN65HVD05DR	D	8	SITE 27	342.9	336.6	0.0
SN65HVD06DR	D	8	SITE 27	342.9	336.6	0.0
SN65HVD07DR	D	8	SITE 27	342.9	336.6	0.0
SN75HVD05DR	D	8	SITE 27	342.9	336.6	0.0
SN75HVD06DR	D	8	SITE 27	342.9	336.6	0.0
SN75HVD07DR	D	8	SITE 27	342.9	336.6	0.0

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS–012 variation AA.

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