PD - 95888

International
IOR Rectifier

SMPS MOSFET

IRFIB7N50L

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ typ.	Trr typ.	I_D
500V	320mΩ	85ns	6.8A

Applications

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications

Features and Benefits

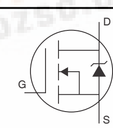
- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.

TO-220 Full-Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	6.8	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	4.3	
I_{DM}	Pulsed Drain Current ①	27	
P_D @T_C = 25°C	Power Dissipation	46	W
	Linear Derating Factor	0.37	W/°C
V_{GS}	Gate-to-Source Voltage	±30	V
dv/dt	Peak Diode Recovery dv/dt ③	24	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	6.8	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	27		
V_{SD}	Diode Forward Voltage	——	——	1.5	V	T_J = 25°C, I_S = 6.8A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	85	130	ns	T_J = 25°C, I_F = 6.8A
		——	130	200		T_J = 125°C, di/dt = 100A/μs ④
Q_{rr}	Reverse Recovery Charge	——	280	420	nC	T_J = 25°C, I_S = 6.8A, V_{GS} = 0V ④
		——	570	860		T_J = 125°C, di/dt = 100A/μs ④
I_{RRM}	Reverse Recovery Current	——	5.9	8.9	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

7/30/04

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.44	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.32	0.38	Ω	V_{GS} = 10V, I_D = 4.1A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	V_{DS} = 500V, V_{GS} = 0V
		—	—	2.0	mA	V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V
R_G	Internal Gate Resistance	—	0.88	—	Ω	f = 1MHz, open drain

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	4.7	—	—	S	V_{DS} = 50V, I_D = 4.1A
Q_g	Total Gate Charge	—	—	92	nC	I_D = 6.8A
Q_{gs}	Gate-to-Source Charge	—	—	24		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	44		V_{GS} = 10V, See Fig. 7 & 16 ④
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	V_{DD} = 250V
t_r	Rise Time	—	36	—		I_D = 6.8A
$t_{d(off)}$	Turn-Off Delay Time	—	47	—		R_G = 9.0Ω
t_f	Fall Time	—	19	—		V_{GS} = 10V, See Fig. 11a & 11b ④
C_{iss}	Input Capacitance	—	2220	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	230	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	23	—		ƒ = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	2780	—		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	—	63	—		V_{GS} = 0V, V_{DS} = 400V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	140	—		V_{GS} = 0V,V_{DS} = 0V to 400V ⑤
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—	100	—		

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	550	mJ
I_{AR}	Avalanche Current ①	—	6.8	A
E_{AR}	Repetitive Avalanche Energy ①	—	4.6	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.69	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	65	

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 12).

② Starting T_J = 25°C, L = 24mH, R_G = 25Ω, I_{AS} = 6.8A, (See Figure 14).

③ $I_{SD} \leq$ 6.8, di/dt ≤ 650A/μs, $V_{DD} \leq V_{(BR)DSS}$, dv/dt = 24V/ns, $T_J \leq$ 150°C.

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
C_{oss} eff.(ER) is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

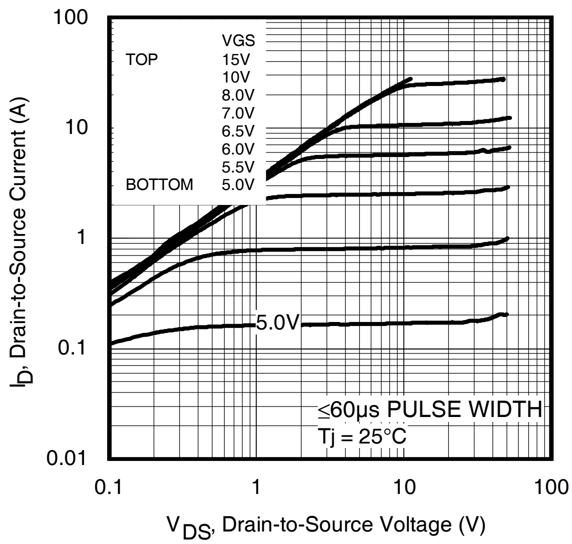


Fig 1. Typical Output Characteristics

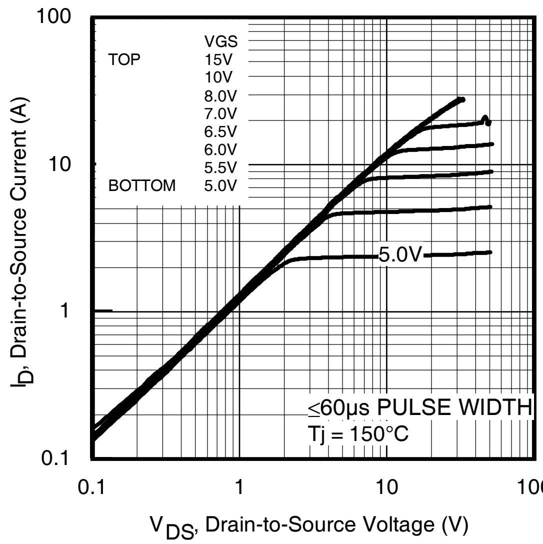


Fig 2. Typical Output Characteristics

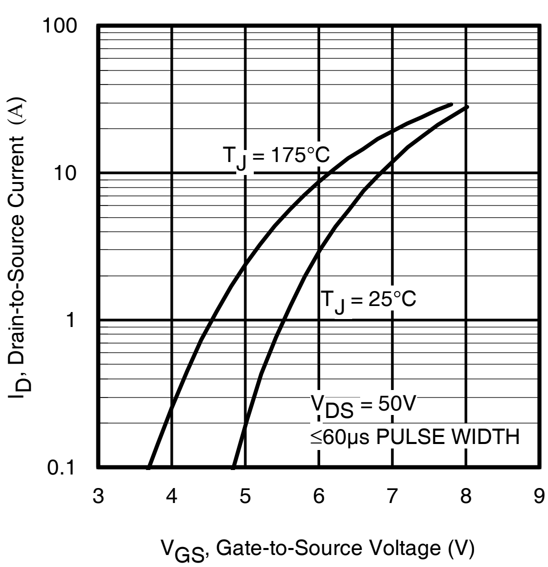


Fig 3. Typical Transfer Characteristics

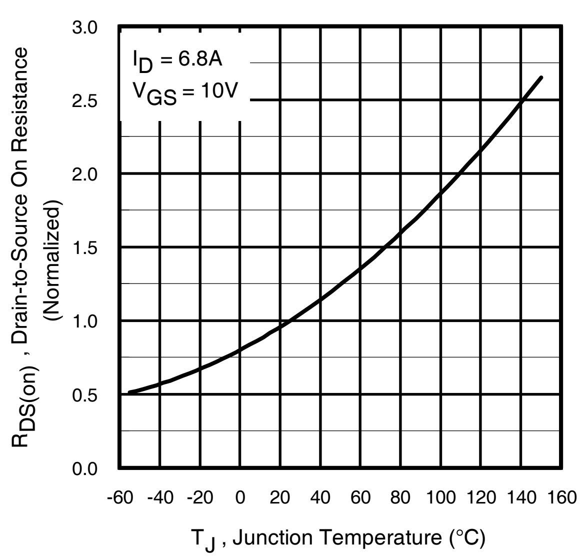


Fig 4. Normalized On-Resistance vs. Temperature

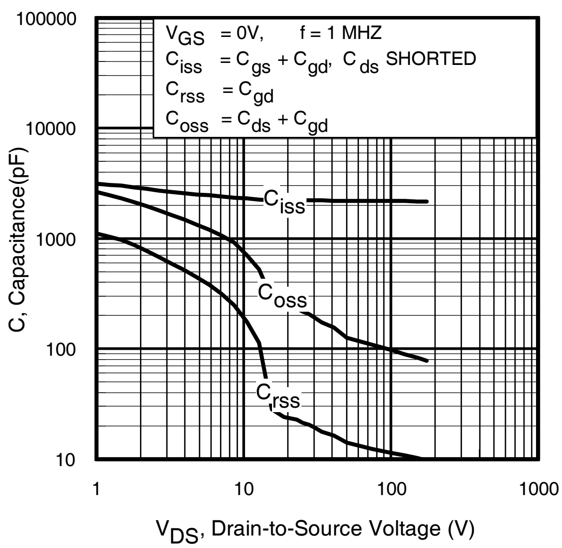


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

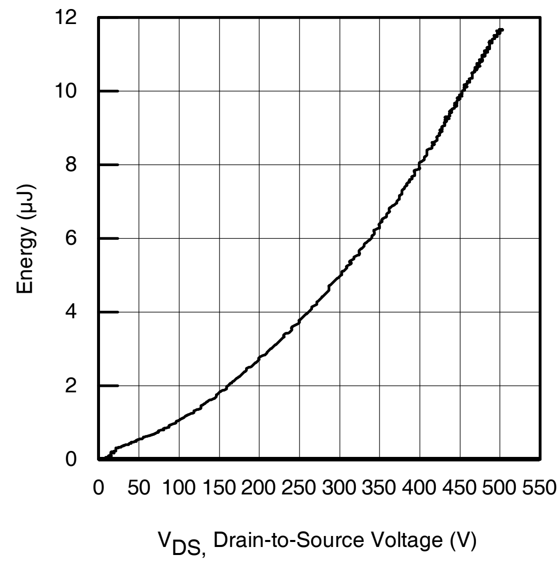


Fig 6. Typ. Output Capacitance Stored Energy vs. V_{DS}

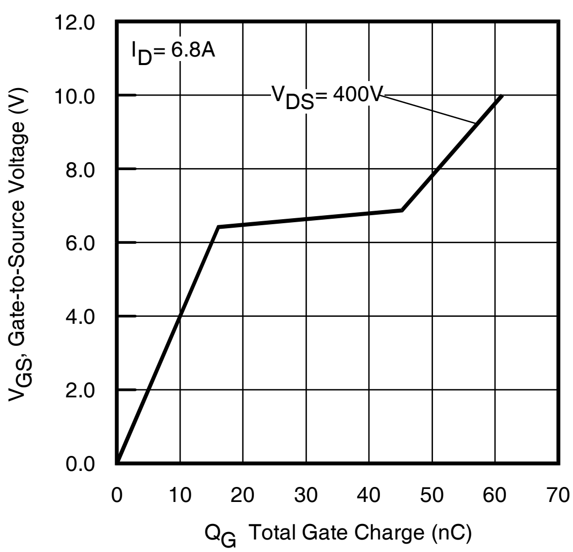


Fig 7. Typical Gate Charge vs. Gate-to-Source Voltage

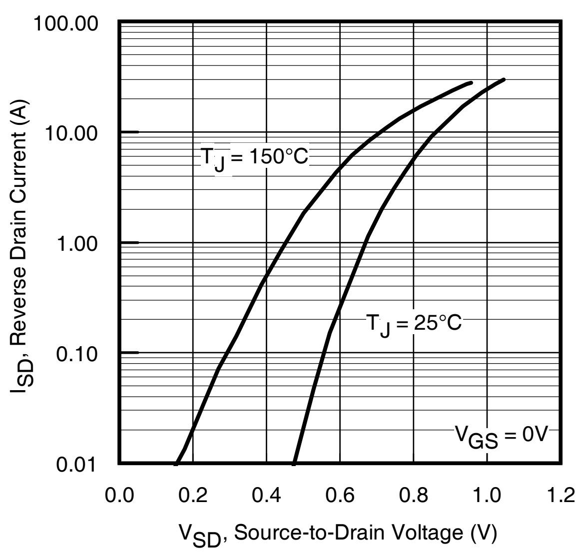


Fig 8. Typical Source-Drain Diode Forward Voltage

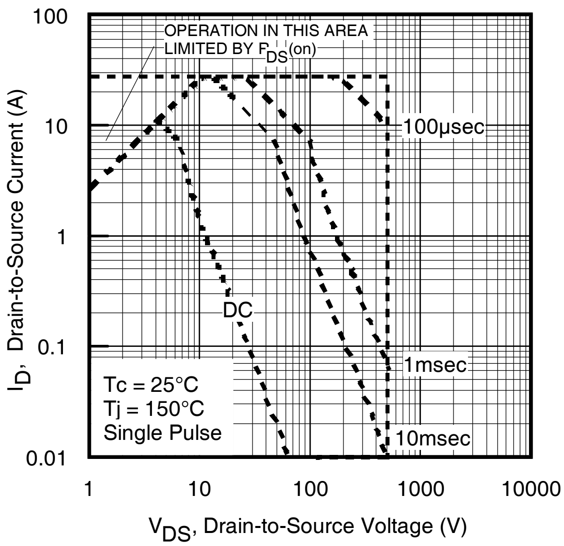


Fig 9. Maximum Safe Operating Area

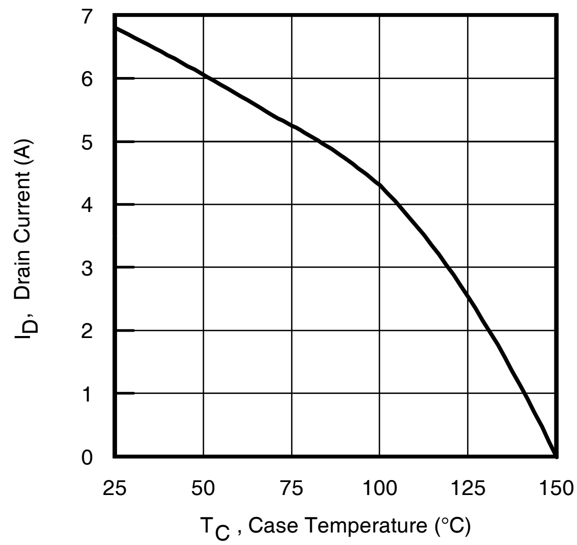


Fig 10. Maximum Drain Current vs. Case Temperature

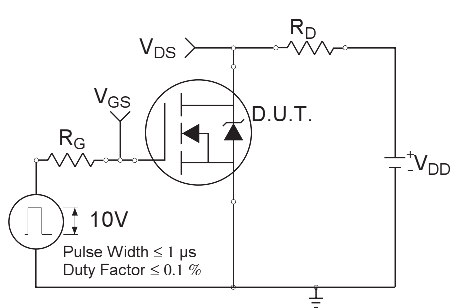


Fig 11a. Switching Time Test Circuit

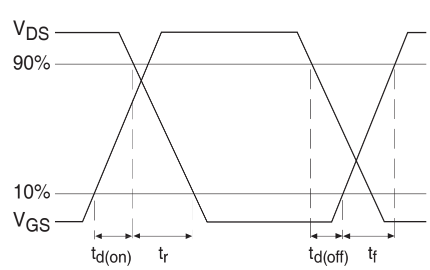


Fig 11b. Switching Time Waveforms

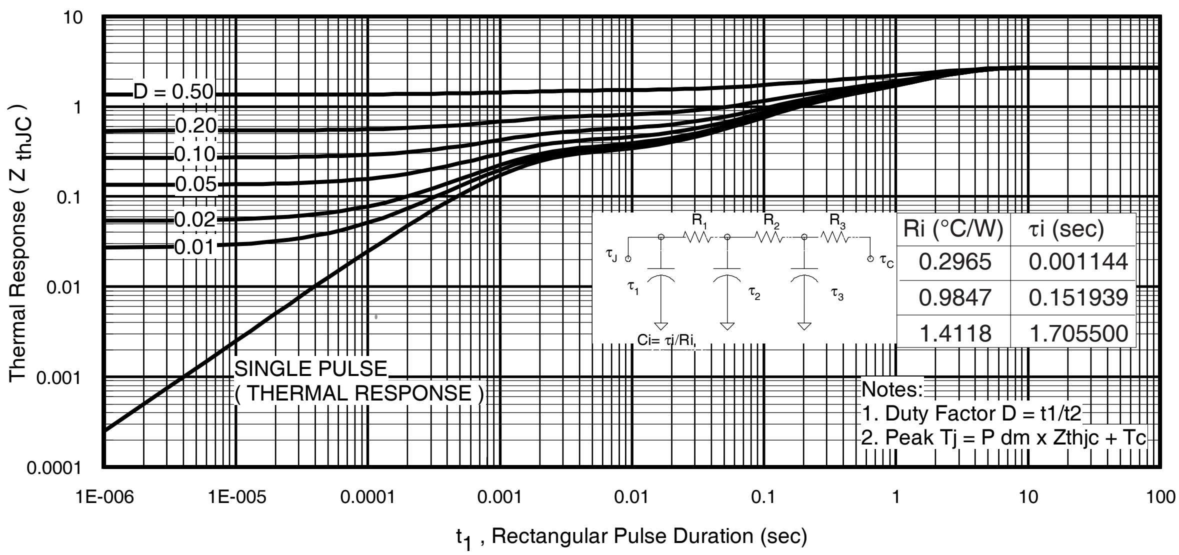


Fig 12. Maximum Effective Transient Thermal Impedance, Junction-to-Case

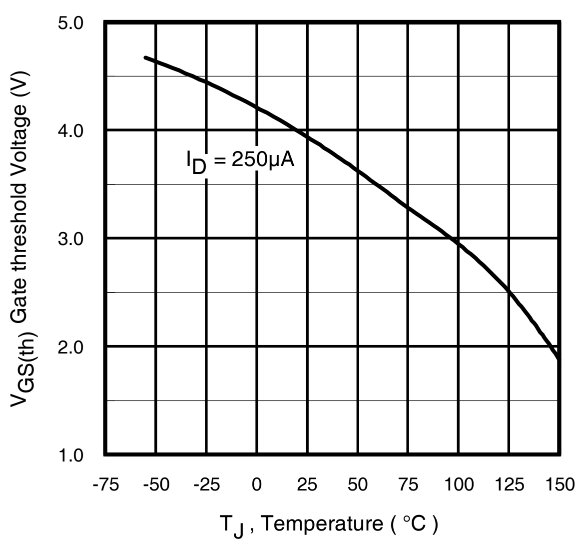


Fig 13. Threshold Voltage vs.Temperature

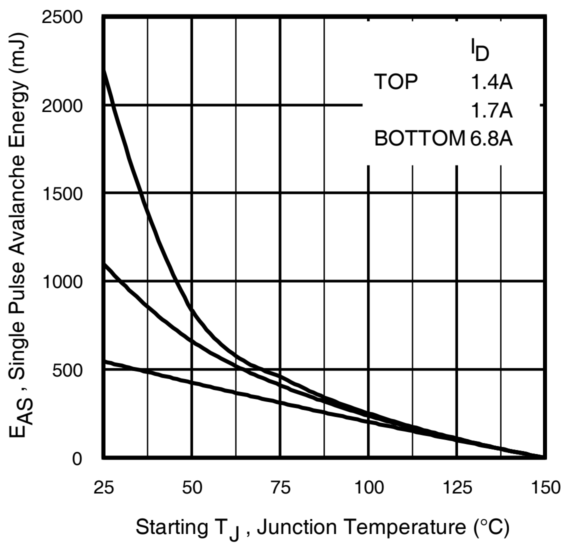


Fig 14. Maximum Avalanche Energy vs. Drain Current

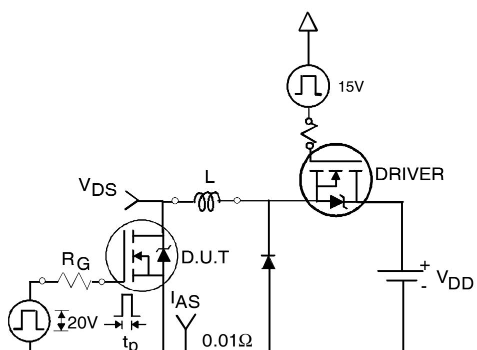


Fig 15a. Unclamped Inductive Test Circuit

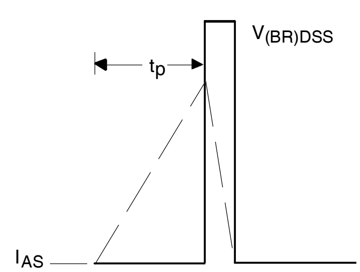


Fig 15b. Unclamped Inductive Waveforms

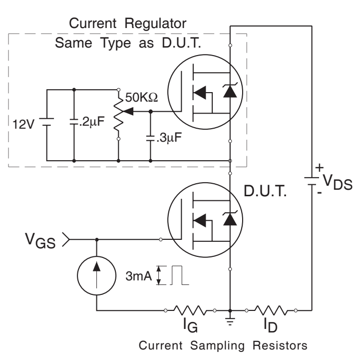


Fig 16a. Gate Charge Test Circuit

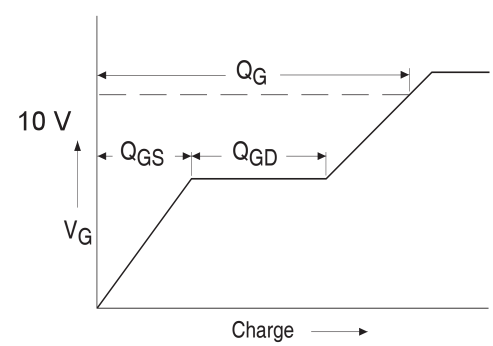
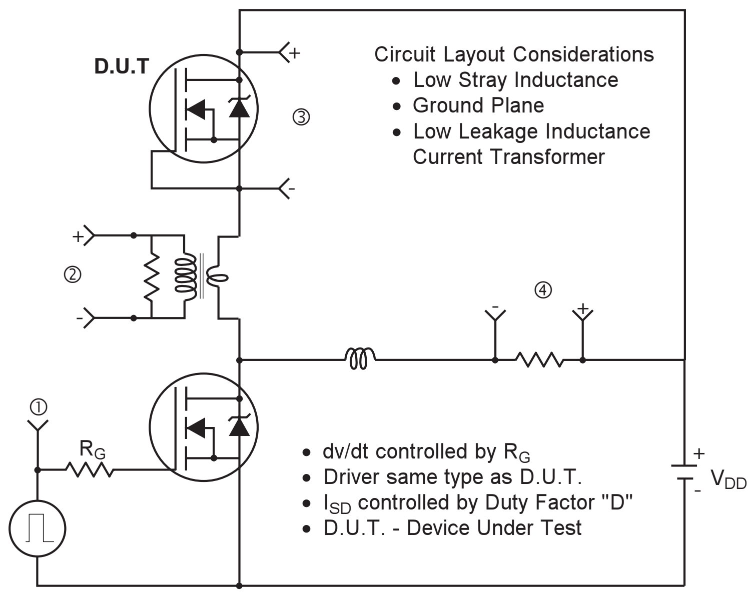
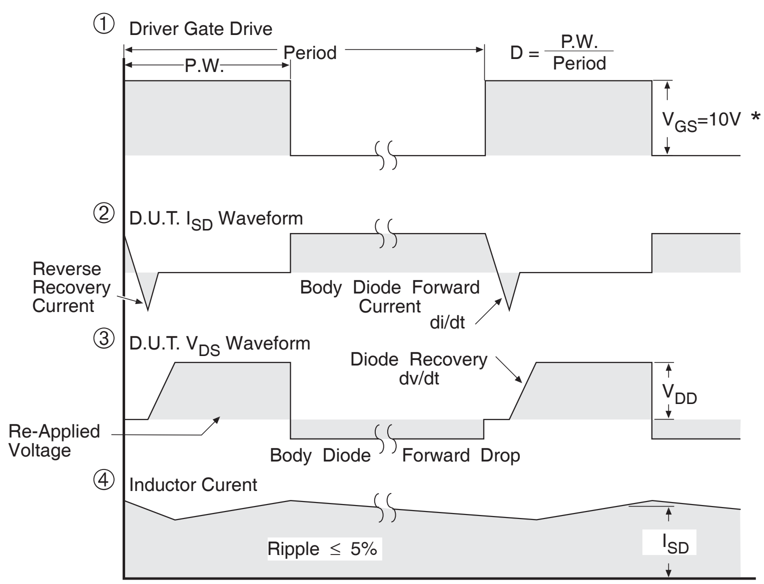


Fig 16b. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit



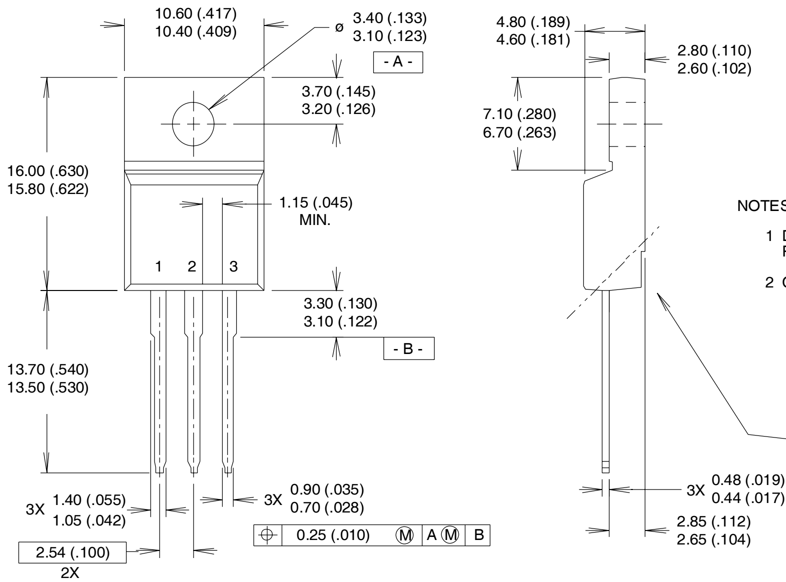


* V_{GS} = 5V for Logic Level Devices

Fig 17. For N-Channel HEXFET® Power MOSFETs

TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)

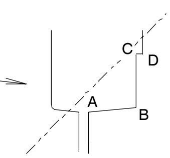


LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982

2 CONTROLLING DIMENSION: INCH.

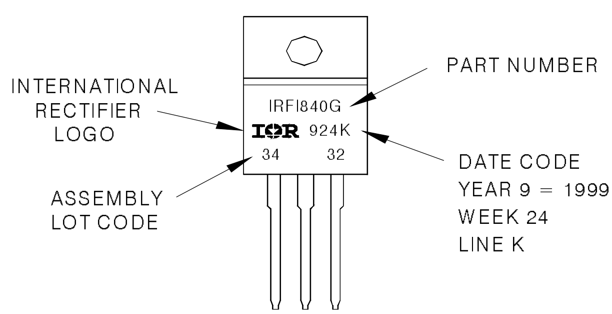


MINIMUM CREEPAGE DISTANCE BETWEEN A-B-C-D = 4.80 (.189)

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



TO-220AB FullPak package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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