QUADRUPLE DIFFERENTIAL LINE DRIVER

- **Meets or Exceeds Requirements of ANSI TIA/EIA-422-B and ITU Recommendation V.11**
- **3-State, TTL-Compatible Outputs**
- **Fast Transition Times**
- **High-Impedance Inputs**
- **Single 5-V Supply**
- **Power-Up and Power-Down Protection**

**D, N, OR NS PACKAGE
(TOP VIEW)**

1A	1	16	V_{CC}
1Y	2	15	4A
1Z	3	14	4Y
1,2EN	4	13	4Z
2Z	5	12	3,4EN
2Y	6	11	3Z
2A	7	10	3Y
GND	8	9	3A

description/ordering information

The MC3487 offers four independent differential line drivers designed to meet the specifications of ANSI TIA/EIA-422-B and ITU Recommendation V.11. Each driver has a TTL-compatible input buffered to reduce current and minimize loading.

The driver outputs utilize 3-state circuitry to provide high-impedance states at any pair of differential outputs when the appropriate output enable is at a low logic level. Internal circuitry is provided to ensure the high-impedance state at the differential outputs during power-up and power-down transition times, provided the output enable is low.

The MC3487 is designed for optimum performance when used with the MC3486 quadruple line receiver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-V supply.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	MC3487N	MC3487N
	SOIC – D	Tube	MC3487D	MC3487
		Tape and reel	MC3487DR	
	SOP – NS	Tape and reel	MC3487NSR	MC3487

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each driver)

INPUT	OUTPUT ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = TTL high level, L = TTL low level,
X = irrelevant, Z = High impedance

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TEXAS INSTRUMENTS

logic diagram (positive logic)
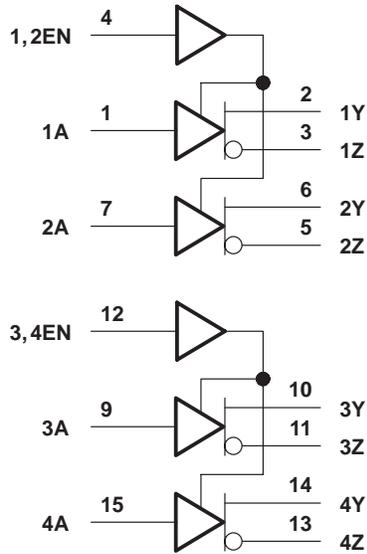
schematics of inputs and outputs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) .... 8 V
Input voltage, V_I .... 5.5 V
Output voltage, V_O .... 7 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package .... 73°C/W
                                                            N package .... 67°C/W
                                                            NS package .... 64°C/W
Operating virtual junction temperature, T_J .... 150°C
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential output voltage, V_{OD}, are with respect to the network ground terminal.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable
ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
T_A	Operating free-air temperature	0		70	°C

MC3487
QUADRUPLE DIFFERENTIAL LINE DRIVER

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				-1.5	V
V_{OH}	High-level output voltage	$V_{IL} = 0.8$ V,	$V_{IH} = 2$ V,	$I_{OH} = -20$ mA	2.5		V
V_{OL}	Low-level output voltage	$V_{IL} = 0.8$ V,	$V_{IH} = 2$ V,	$I_{OL} = 48$ mA		0.5	V
$|V_{OD}|$	Differential output voltage	$R_L = 100$ Ω,	See Figure 1		2		V
$\Delta|V_{OD}|$	Change in magnitude of differential output voltage†	$R_L = 100$ Ω,	See Figure 1			±0.4	V
V_{OC}	Common-mode output voltage‡	$R_L = 100$ Ω,	See Figure 1			3	V
$\Delta|V_{OC}|$	Change in magnitude of common-mode output voltage†	$R_L = 100$ Ω,	See Figure 1			±0.4	V
I_O	Output current with power off	$V_{CC} = 0$	$V_O = 6$ V			100	µA
			$V_O = -0.25$ V			-100	
I_{OZ}	High-impedance-state output current	Output enables at 0.8 V	$V_O = 2.7$ V			100	µA
			$V_O = 0.5$ V			-100	
I_I	Input current at maximum input voltage	$V_I = 5.5$ V				100	µA
I_{IH}	High-level input current	$V_I = 2.7$ V				50	µA
I_{IL}	Low-level input current	$V_I = 0.5$ V				-400	µA
I_{OS}	Short-circuit output current§	$V_I = 2$ V			-40	-140	mA
I_{CC}	Supply current (all drivers)	Outputs disabled				105	mA
		Outputs enabled,	No load			85	

† $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
‡ In ANSI Standard TIA/EIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
§ Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V

	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 15$ pF,	See Figure 2		20	ns
t_{PHL}	Propagation delay time, high- to low-level output				20	
t_{sk}	Skew time	$C_L = 15$ pF,	See Figure 2		6	ns
$t_{t(OD)}$	Differential-output transition time	$C_L = 15$ pF,	See Figure 3		20	ns
t_{PZH}	Output enable time to high level	$C_L = 50$ pF,	See Figure 4		30	ns
t_{PZL}	Output enable time to low level				30	
t_{PHZ}	Output disable time from high level	$C_L = 50$ pF,	See Figure 4		25	ns
t_{PLZ}	Output disable time from low level				30	

PARAMETER MEASUREMENT INFORMATION
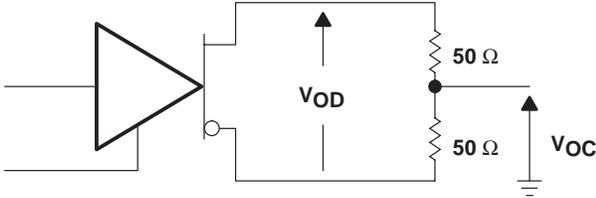
Figure 1. Differential and Common-Mode Output Voltages
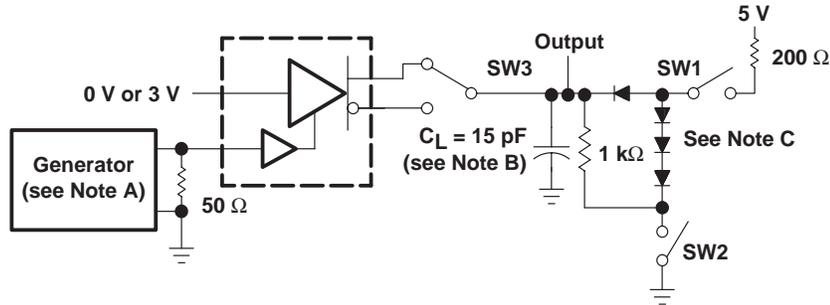
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50$ Ω.
        B. C_L includes probe and stray capacitance.
        C. All diodes are 1N916 or 1N3064.

Figure 2. Test Circuit and Voltage Waveforms
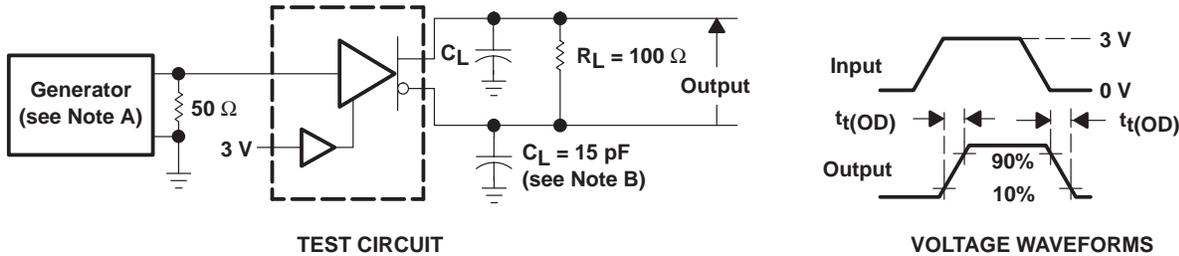
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50$ Ω.
        B. C_L includes probe and stray capacitance.
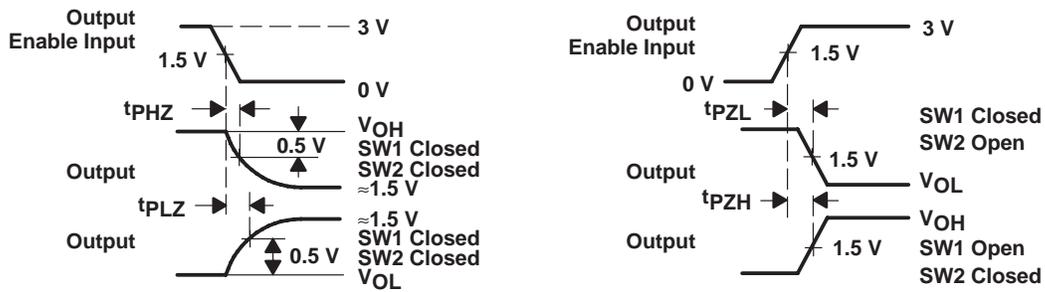
Figure 3. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

Figure 4. Driver Test Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
MC3487D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
MC3487N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC3487NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC3487NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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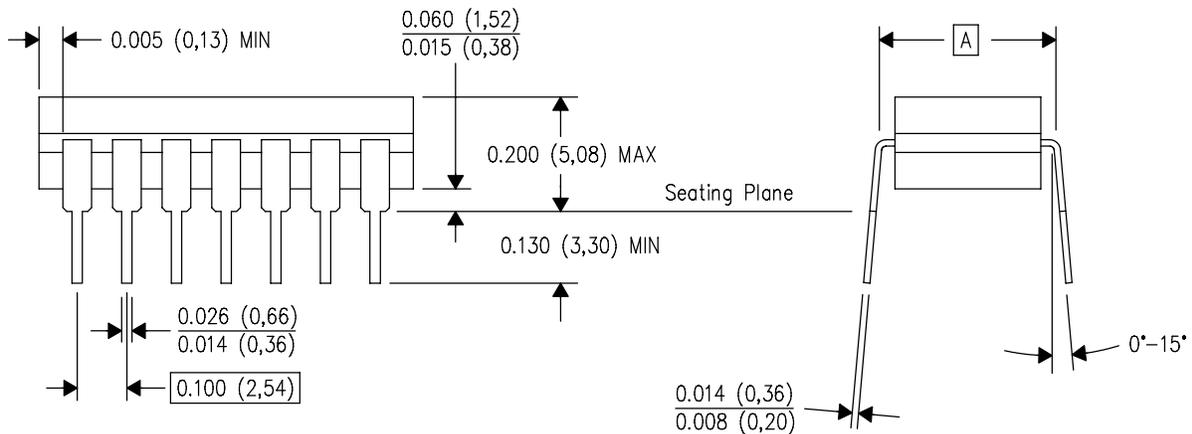
J (R-GDIP-T**)   CERAMIC DUAL IN-LINE PACKAGE
14 LEADS SHOWN
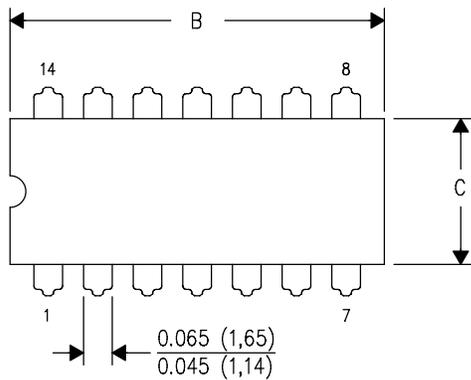
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

A

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

0°-15°

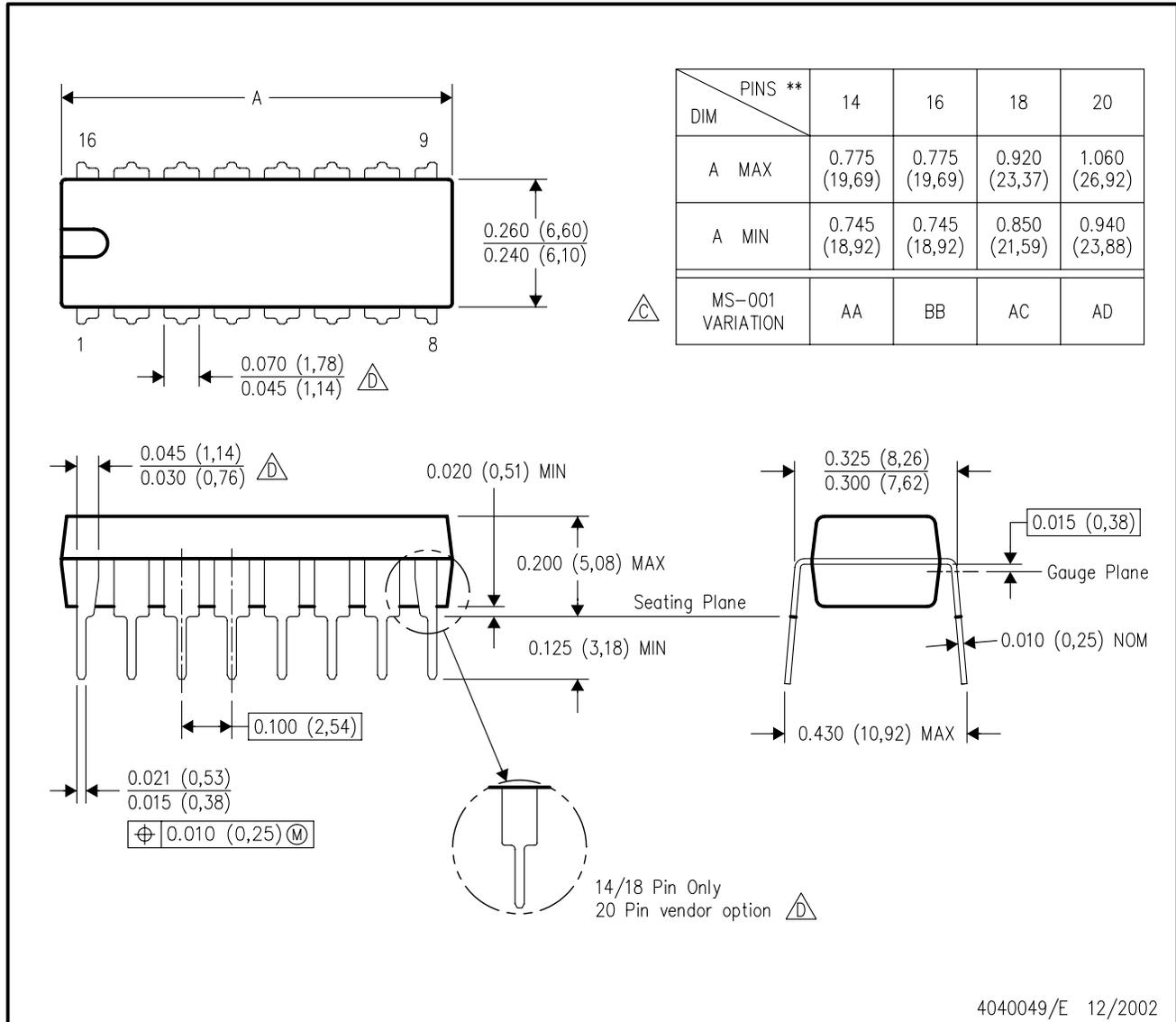0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

	PINS **	14	16	18	20
DIM					
A MAX		0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN		0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION		AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.430 (10,92) MAX

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
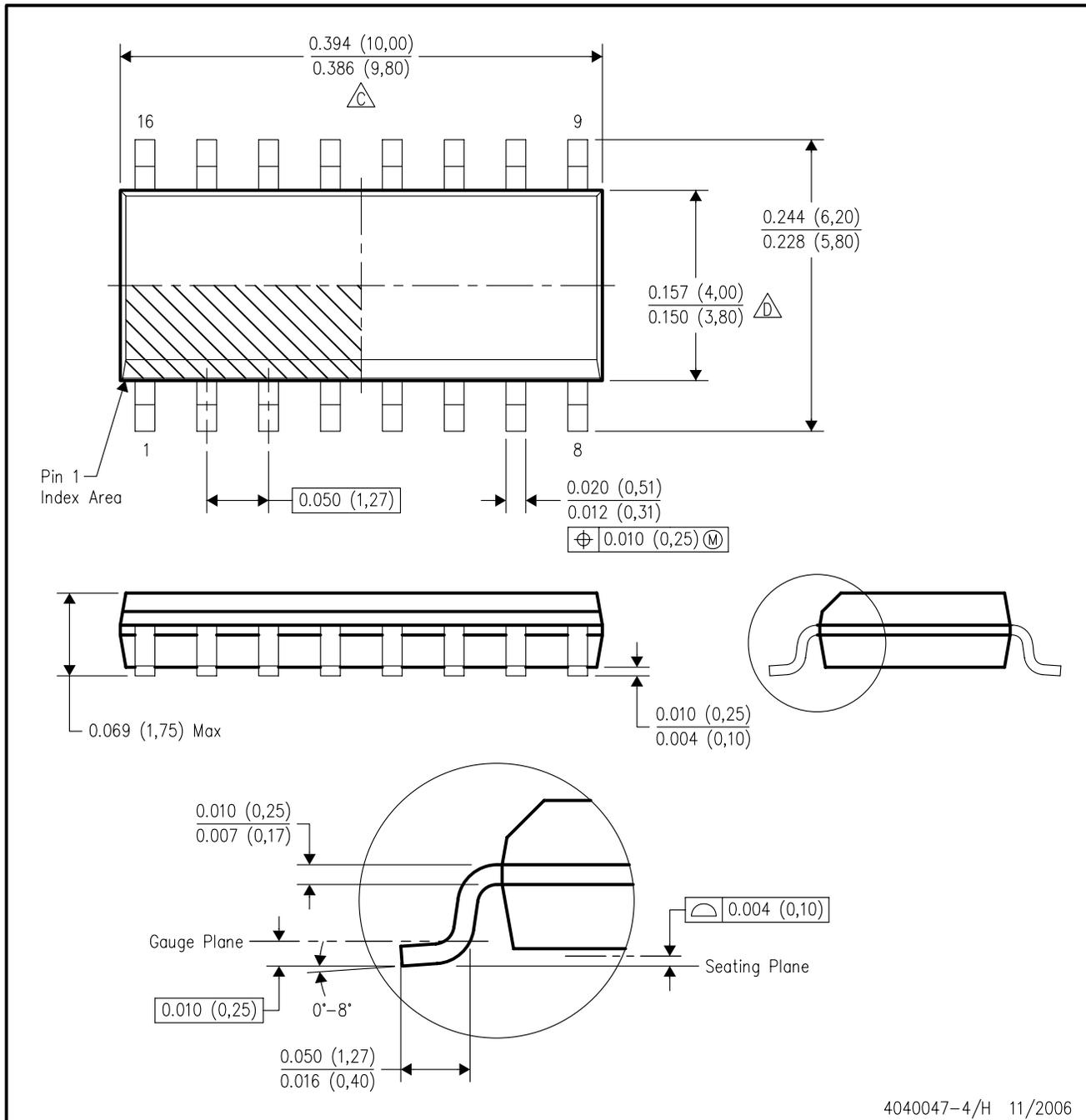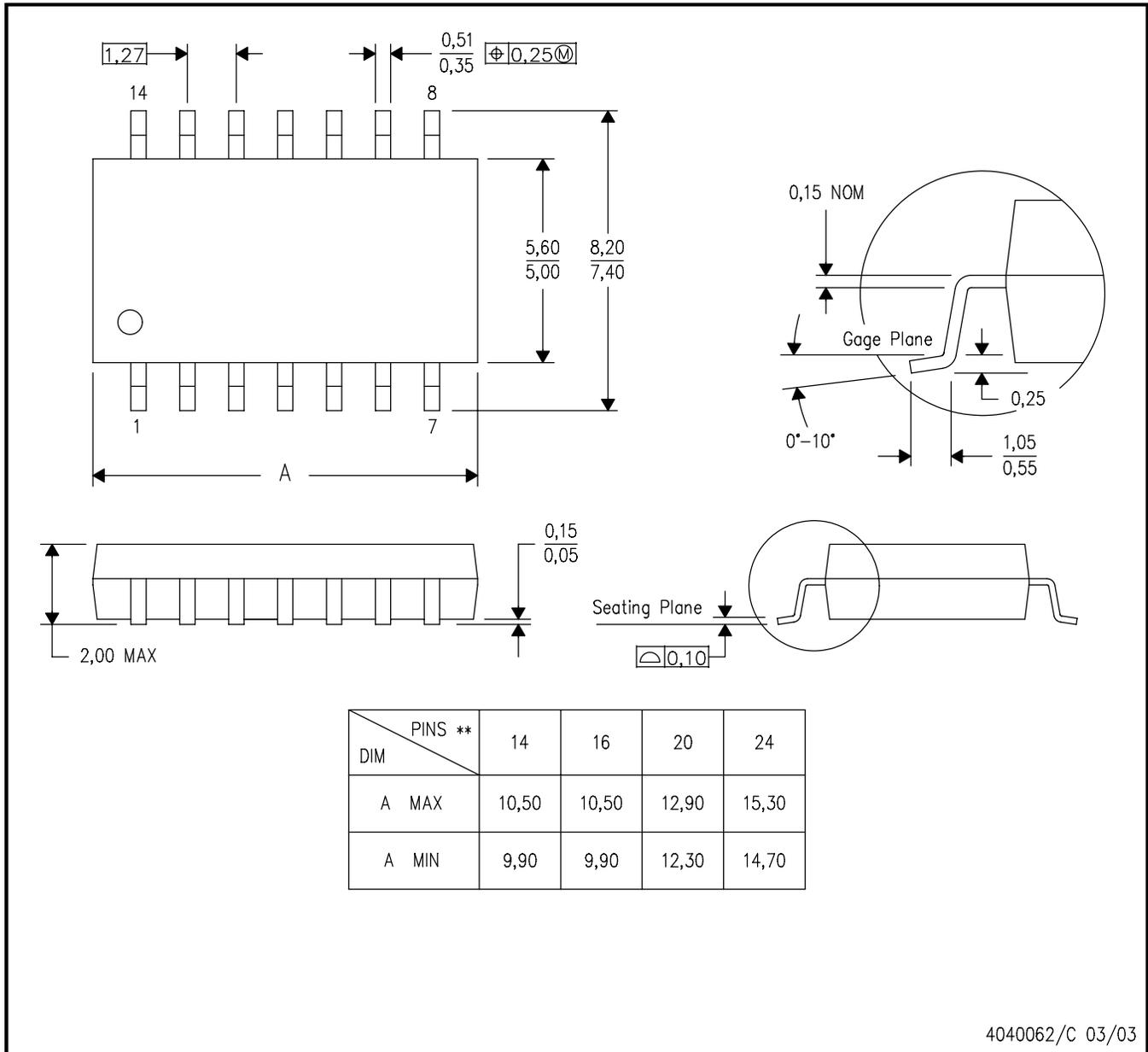20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⚠D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/H   11/2006

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
        ⚠C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed .006 (0,15) per end.
        ⚠D   Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
         E.   Reference JEDEC MS−012 variation AC.

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MECHANICAL DATA

14-PINS SHOWN

1,27 ⟶   ⟶   0,51 / 0,35   ⊕ 0,25 Ⓜ

14   8

5,60 / 5,00   8,20 / 7,40

1   7

A

0,15 NOM

Gage Plane

0,25

0°–10°   1,05 / 0,55

0,15 / 0,05

2,00 MAX

Seating Plane

⌲ 0,10

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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