

# International IOR Rectifier

PD - 94609

## HEXFET® POWER MOSFET THRU-HOLE (Low-ohmic TO-254AA)

## IRF7MS2907 75V, N-CHANNEL

### Product Summary

Part Number	BVDSS	RDS(on)	ID
IRF7MS2907	75V	0.0055Ω	45A*



Seventh Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon unit area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

These devices are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits.

### Features:

- Low RDS(on)
- Avalanche Energy Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight

### Absolute Maximum Ratings

	Parameter		Units
ID @ VGS = 10V, TC = 25°C	Continuous Drain Current	45*	A
ID @ VGS = 10V, TC = 100°C	Continuous Drain Current	45*	
IDM	Pulsed Drain Current ①	180	
PD @ TC = 25°C	Max. Power Dissipation	208	W
	Linear Derating Factor	1.67	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	760	mJ
IAR	Avalanche Current ①	45	A
EAR	Repetitive Avalanche Energy ①	20.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.2	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063in./1.6mm from case for 10s)	
	Weight	4.3 (Typical)	g

\* Current is limited by package

For footnotes refer to the last page

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**Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)**

	Parameter	Min	Typ	Max	Units	Test Conditions
B <sub>V</sub> DSS	Drain-to-Source Breakdown Voltage	75	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔB <sub>V</sub> DSS/ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	0.087	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	0.0055	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 45A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	70	—	—	S (Ω)	V <sub>DS</sub> > 15V, I <sub>DS</sub> = 45A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	20	μA	V <sub>DS</sub> = 75V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	375	nC	V <sub>GS</sub> = 10V, I <sub>D</sub> = 45A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	60		V <sub>DS</sub> = 60V
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	—	150		
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	40	ns	V <sub>DD</sub> = 38V, I <sub>D</sub> = 45A
t <sub>r</sub>	Rise Time	—	—	135		V <sub>GS</sub> = 10V, R <sub>G</sub> = 1..2Ω
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	175		
t <sub>f</sub>	Fall Time	—	—	75		
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C <sub>iss</sub>	Input Capacitance	—	12060	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V
C <sub>oss</sub>	Output Capacitance	—	2280	—		f = 1.0MHz
C <sub>rss</sub>	Reverse Transfer Capacitance	—	605	—		

**Source-Drain Diode Ratings and Characteristics**

	Parameter	Min	Typ	Max	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	45*	A	
I <sub>SM</sub>	Pulse Source Current (Body Diode) ①	—	—	180		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.0	V	T <sub>j</sub> = 25°C, I <sub>S</sub> = 45A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	175	ns	T <sub>j</sub> = 25°C, I <sub>F</sub> = 45A, di/dt ≤ 100A/μs
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	850	nC	V <sub>DD</sub> ≤ 25V ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				

\* Current is limited by package

**Thermal Resistance**

	Parameter	Min	Typ	Max	Units	Test Conditions
R <sub>thJC</sub>	Junction-to-Case	—	—	0.6	°C/W	

**Note:** Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

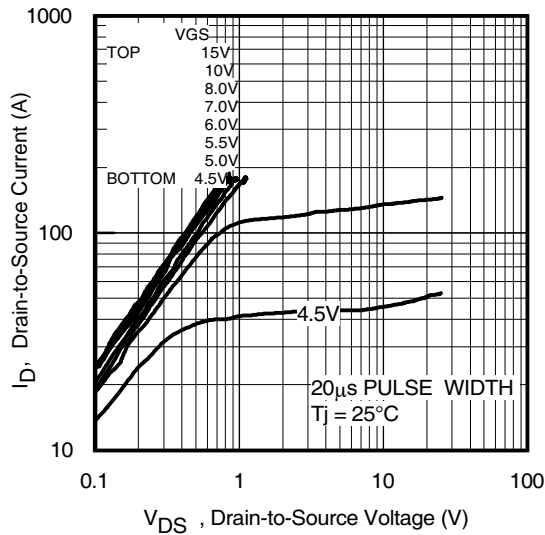


Fig 1. Typical Output Characteristics

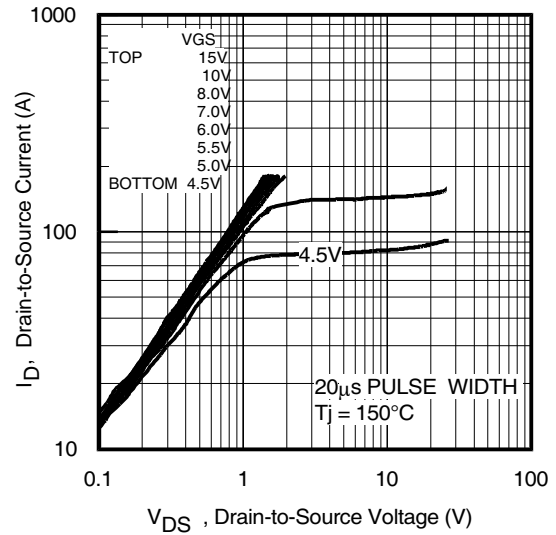


Fig 2. Typical Output Characteristics

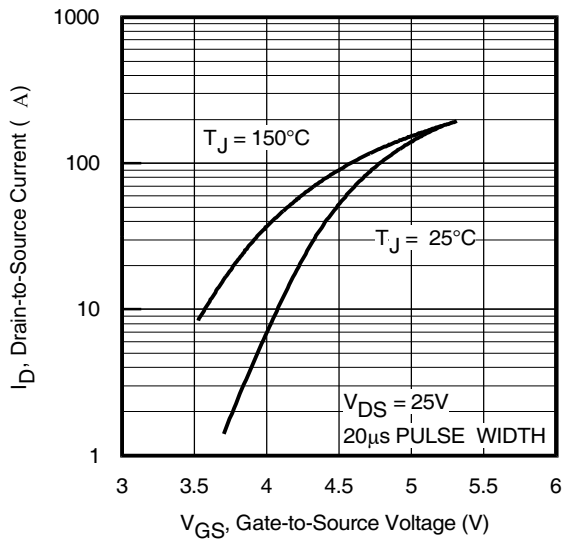


Fig 3. Typical Transfer Characteristics

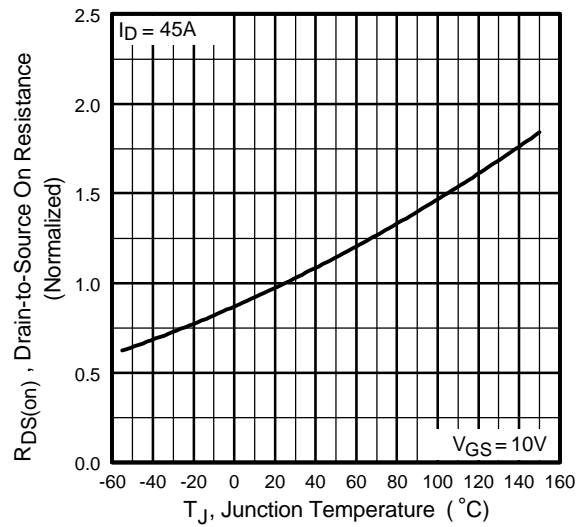
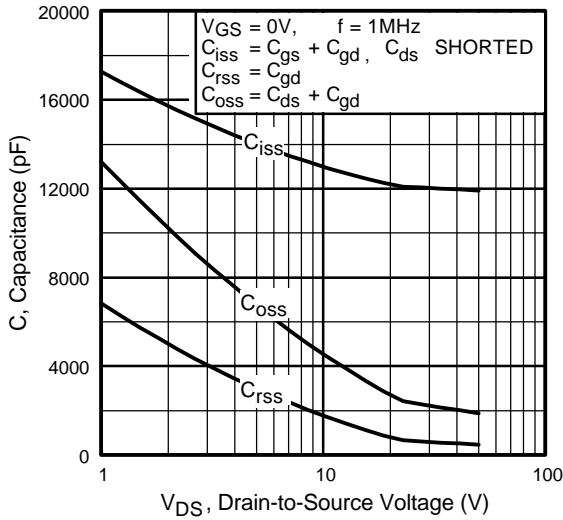
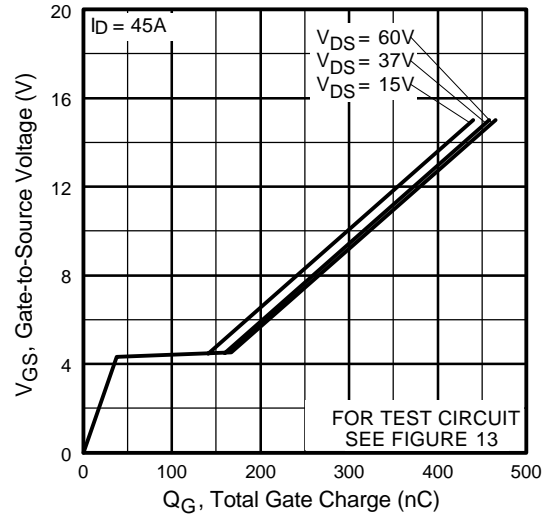


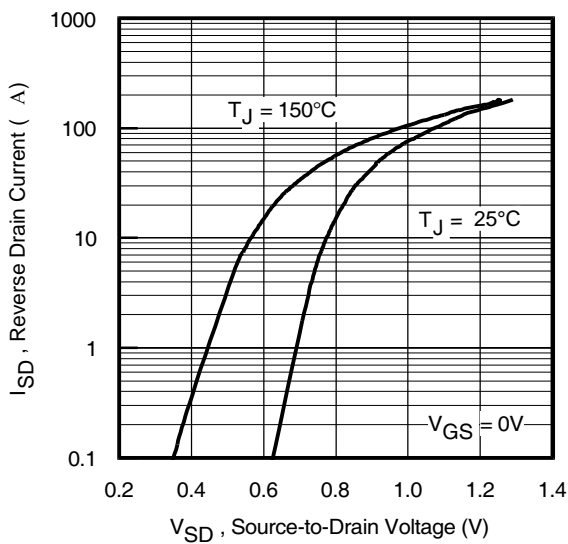
Fig 4. Normalized On-Resistance Vs. Temperature



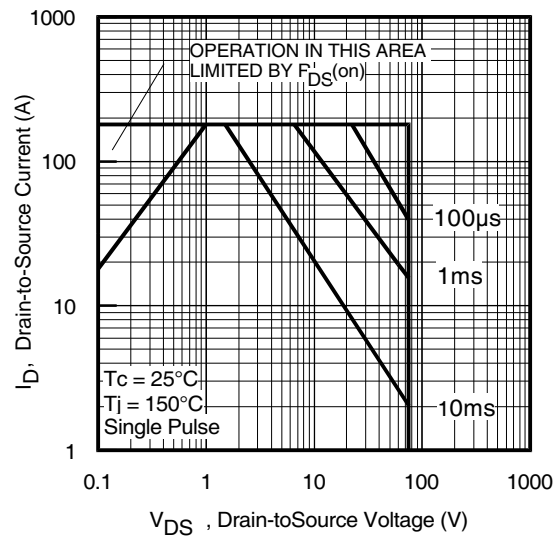
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

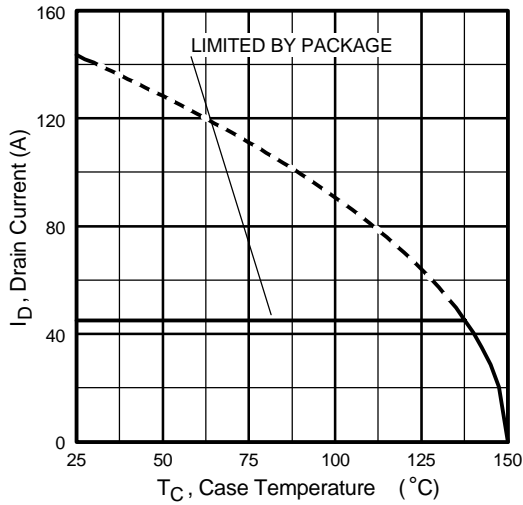


Fig 9. Maximum Drain Current Vs. Case Temperature

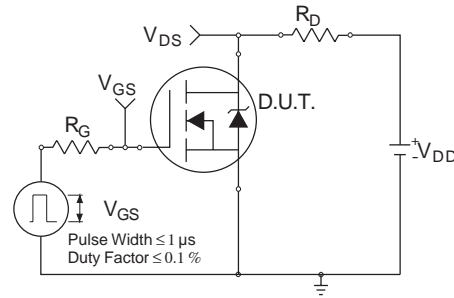


Fig 10a. Switching Time Test Circuit

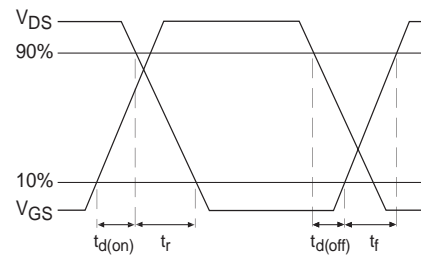


Fig 10b. Switching Time Waveforms

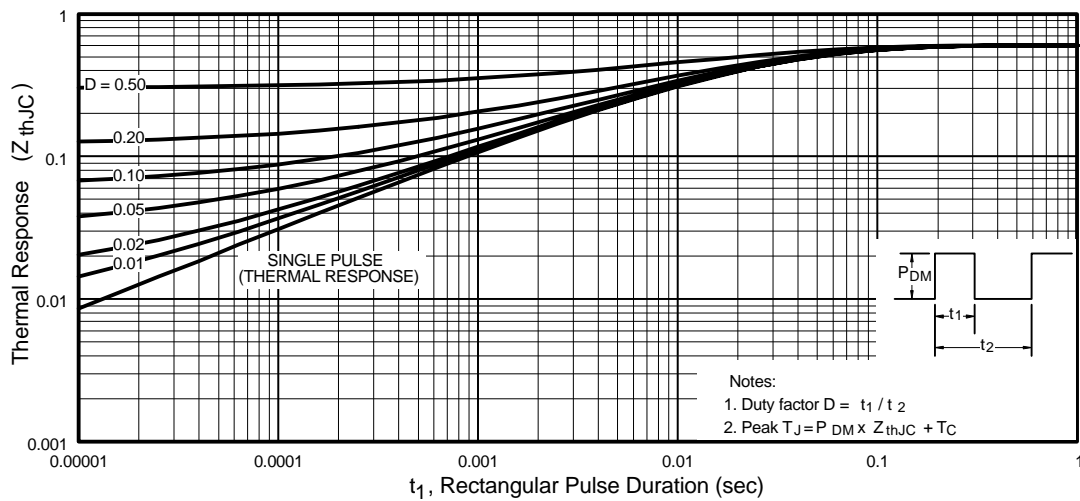


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

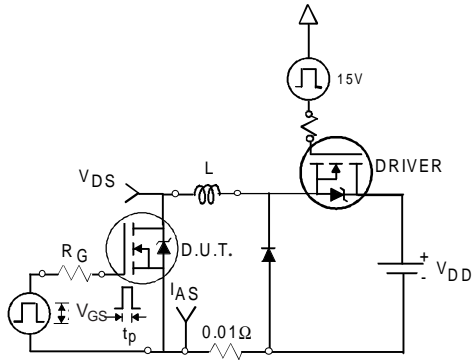


Fig 12a. Unclamped Inductive Test Circuit

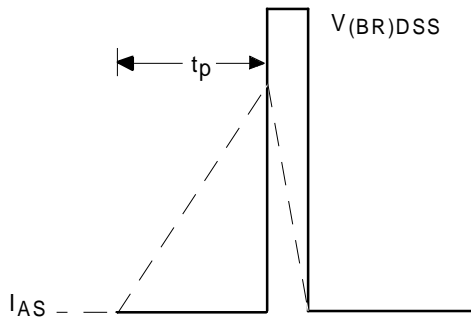


Fig 12b. Unclamped Inductive Waveforms

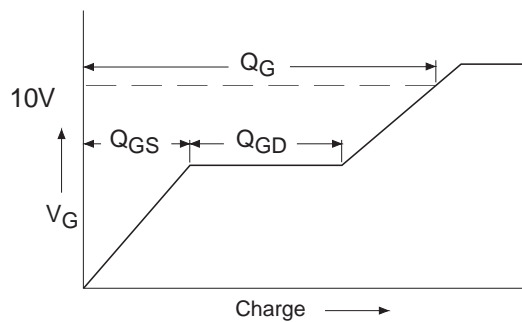


Fig 13a. Basic Gate Charge Waveform

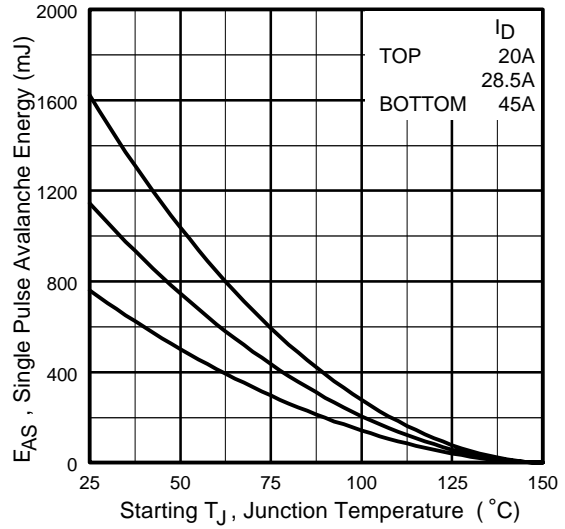


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

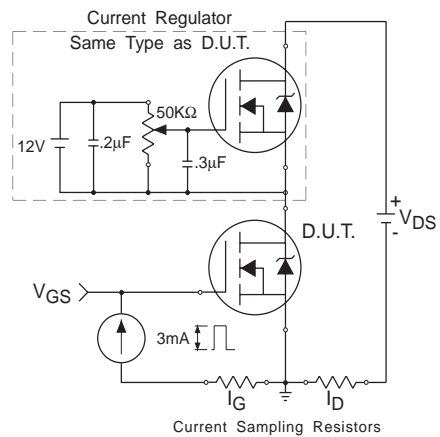
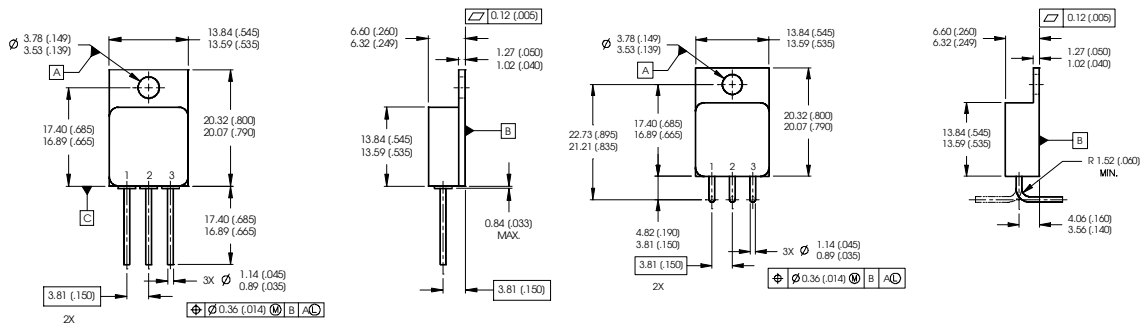


Fig 13b. Gate Charge Test Circuit

**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ②  $V_{DD} = 25\text{ V}$ , Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.75\text{mH}$   
 Peak  $I_{AS} = 45\text{A}$ ,  $V_{GS} = 10\text{V}$ ,  $R_G = 25\Omega$
- ③  $I_{SD} \leq 45\text{A}$ ,  $di/dt \leq 380\text{A}/\mu\text{s}$ ,  
 $V_{DD} \leq 75\text{V}$ ,  $T_J \leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\ \mu\text{s}$ ; Duty Cycle  $\leq 2\%$

**Case Outline and Dimensions — Low-ohmic TO-254AA**



**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

**PIN ASSIGNMENTS**

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

**CAUTION**

**BERYLLIA WARNING PER MIL-PRF-19500**

Packages containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.