



XRD87L75

Low-Voltage CMOS 8-Bit High-Speed Analog-to-Digital Converter

April 2002

FEATURES

- 8-Bit Resolution
- Up to 10MHz Sampling Rate
- Internal S/H Function
- Single Supply: 3.3V
- V_{IN} DC Range: 0V to V_{DD}
- V_{REF} DC Range: 1V to V_{DD}
- Low Power: 25mW typ. (excluding reference)
- Latch-Up Free

APPLICATIONS

- Digital Color Copiers
- Cellular Telephones
- CCD-Based Systems
- Hardware Scanners
- Video Capture Boards

GENERAL DESCRIPTION

The XRD87L75 is an 8-bit Analog-to-Digital Converter in a small 20-pin SOIC/SSOP package. Designed using an advanced 3.3V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

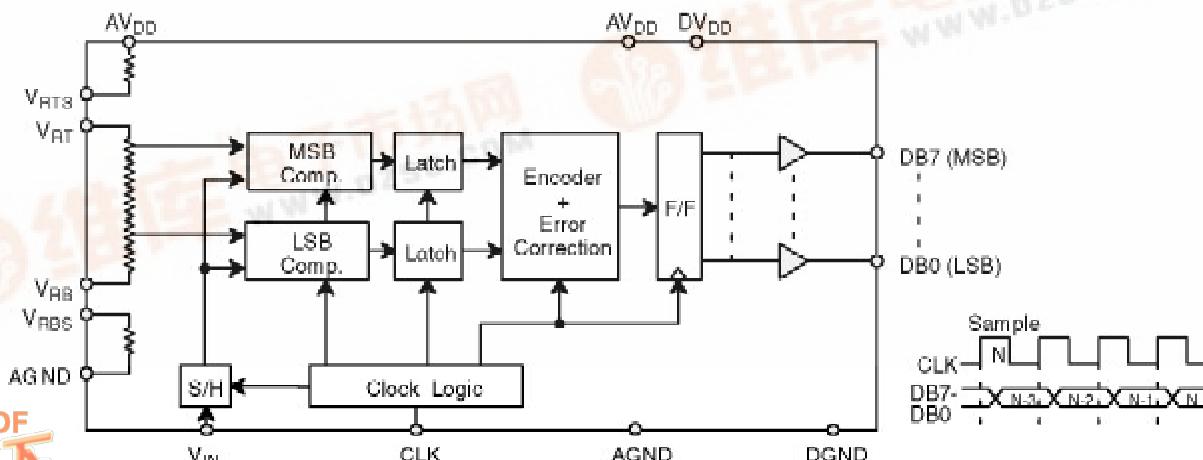
This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the XRD87L75 includes an on-chip S/H function and allows the user to digitize analog input signals between AGND and AV_{DD} . Careful design and chip layout have achieved a low analog input capacitance. This reduces "kickback" and eases the requirements of the buffer/amplifier used to drive the XRD87L75.

The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS} , or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.4V at V_{RB} and 1.72V at V_{RT} . Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD} . This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +3.3V supply. Power consumption is 25mW at $F_s = 6$ MHz.

Specified for operation over the commercial / industrial (-40 to +85°C) temperature range, the XRD87L75 is available in Surface Mount (SOIC), Shrink Small Outline (SSOP) and Plastic Dual-In-line (PDIP) Packages.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



XRD87L75

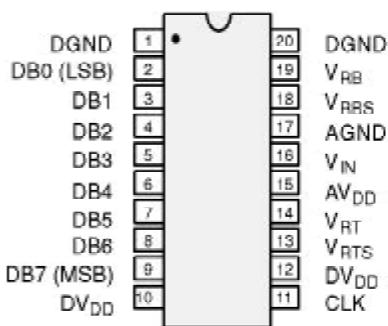
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ORDERING INFORMATION

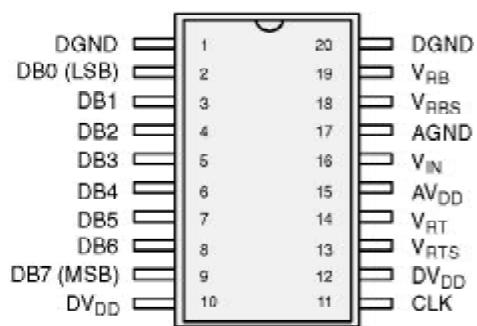
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	-40 to +85°C	XRD87L75AID	+/-0.5	+/-1.5
PDIP	-40 to +85°C	XRD87L75AIP	+/-0.5	+/-1.5
SSOP	-40 to +85°C	XRD87L75AIU	+/-0.5	+/-1.5

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20-Pin PDIP (300 MIL) - P20



20-Pin SOIC (Jedec, 300 MIL) - D20

20-Pin SSOP (5.3mm) - U20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION	PIN NO.	NAME	DESCRIPTION
1	DGND	Digital Ground	11	CLK	Sample Clock
2	DB0	Data Output Bit 0 (LSB)	12	DV _{DD}	Digital Power Supply
3	DB1	Data Output Bit 1	13	V _{RTS}	Generates 1.72V if tied to V _{RT}
4	DB2	Data Output Bit 2	14	V _{RT}	Top Reference
5	DB3	Data Output Bit 3	15	AV _{DD}	Analog Power Supply
6	DB4	Data Output Bit 4	16	V _{IN}	Analog Input
7	DB5	Data Output Bit 5	17	AGND	Analog Ground
8	DB6	Data Output Bit 6	18	V _{RBS}	Generates 0.4V if tied to V _{RB}
9	DB7	Data Output Bit 7 (MSB)	19	V _{RB}	Bottom Reference
10	DV _{DD}	Digital Power Supply	20	DGND	Digital Ground

**XRD87L75****ELECTRICAL CHARACTERISTICS TABLE**

UNLESS OTHERWISE SPECIFIED: $AV_{DD} = DV_{DD} = 3.3V$, $FS = 6MHz$ (50% DUTY CYCLE),
 $V_{RT} = 2.5V$, $V_{RB} = 0.5V$, $T_A = 25^\circ C$

Parameter	Symbol	25°C			Units	Test Conditions/Comments
		Min	Typ	Max		
KEY FEATURES						
Resolution		8			Bits	
Sampling Rate	FS	0.1	6	10	MHz	
ACCURACY						
Differential Non-Linearity	DNL		+/-0.3	+/-0.5	LSB	
Integral Non-Linearity	INL		+/-0.75	+/-1.5	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+3		LSB	
Full Scale Error	EFS		-2		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}		2.5	AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND	0.5		V	
Differential Ref. Voltage ³	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L	245	350	550	Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/ $^\circ C$	
Self Bias 1						
Short V_{RB} and V_{RBS}	V_{RB}		0.4		V	
Short V_{RT} and V_{RTS}	$V_{RT} - V_{RB}$		1.72		V	
Self Bias 2						
$V_{RB} = AGND$,	V_{RT}		1.5		V	
Short V_{RT} and V_{RTS}						
ANALOG INPUT						
Input Bandwidth (-1 dB) ^{2,4}	BW		50		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance ⁵	C_{IN}		16		pF	
Aperture Delay ²	t_{AP}		4		ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.5		0.5	V	
Logical "0" Voltage	V_{IL}				V	
DC Leakage Current ⁶	I_{IN}				μA	
CLK			5		pF	
Input Capacitance			5			
Clock Timing (See Figure 1.) ⁷						
Clock Period	1/FS	100	166		ns	
High Pulse Width	t_{PWH}	50	83		ns	
Low Pulse Width	t_{PWL}	50	83		ns	
DIGITAL OUTPUTS						
Logical "1" Voltage	V_{OH}	2.5		0.5	V	$C_{OUT} = 15 pF$
Logical "0" Voltage	V_{OL}				V	$I_{LOAD} = 1 mA$
Data Valid Delay ⁸	t_{DL}		12		ns	$I_{LOAD} = 1 mA$

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ELECTRICAL CHARACTERISTICS TABLE (CONT'D)
UNLESS OTHERWISE SPECIFIED: $AV_{DD} = DV_{DD} = 3.3V$, $FS = 6MHz$ (50% DUTY CYCLE),
 $V_{RT} = 2.5V$, $V_{RB} = 0.5V$, $T_A = 25^\circ C$

Parameter	Symbol	25°C			Units	Test Conditions/Comments
ACPARAMETERS		Min	Typ	Max		
Differential Gain Error	d_G		2		%	FS = 4 x NTSC
Differential Phase Error	d_{PH}		1		Degree	FS = 4 x NTSC
POWER SUPPLIES						
Operating Voltage (AV_{DD} , DV_{DD}) ⁹	V_{DD}	3	3.3	3.6	V	
Current (AGND + DGND)	I_{DD}		8	12	mA	Does not include ref. current

NOTES

1. The difference between the measured and the ideal code width ($V_{REP}/256$) is the DNL error (Figure 3). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (Figure 4). Accuracy is a function of the sampling rate (FS).
2. Guaranteed, not tested.
3. Specified values guarantee functionality. Refer to other parameters for accuracy.
4. -1dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
5. See V_{IN} input equivalent circuit (Figure 5). Switched capacitor analog input requires driver with low output resistance.
6. All inputs have diodes to DV_{DD} and DGND. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD} .
7. t_p , t_r should be limited to >5ns for best results.
8. Depends on the RC load connected to the output pin.
9. AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise noted)^{1, 2, 3}

V_{DD} to GND	5.5V	Storage Temperature	-65 to +150°C
V_{RT} & V_{RB}	$V_{DD} + 0.5$ to GND -0.5V	Lead Temperature (Soldering 10 seconds) ...	+300°C
V_{IN}	$V_{DD} + 0.5$ to GND -0.5V	Package Power Dissipation Rating @ 75°C	
All Inputs	$V_{DD} + 0.5$ to GND -0.5V	PDIP, SOIC, SSOP	650mW
All Outputs	$V_{DD} + 0.5$ to GND -0.5V	Derates above 75°C	9mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100ms.
3. V_{DD} refers to AV_{DD} and DV_{DD} . GND refers to AGND and DGND.

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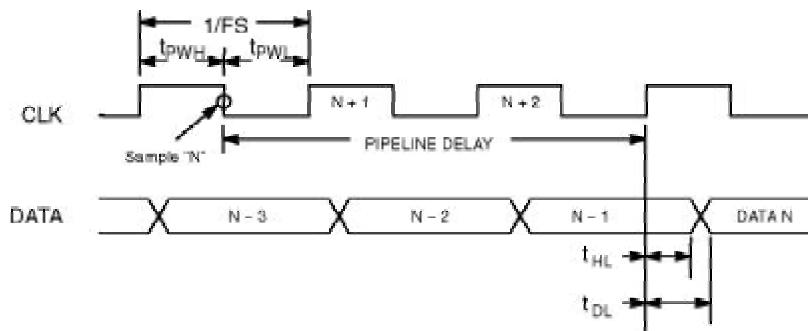


Figure 1. XRD87L75 Timing Diagram

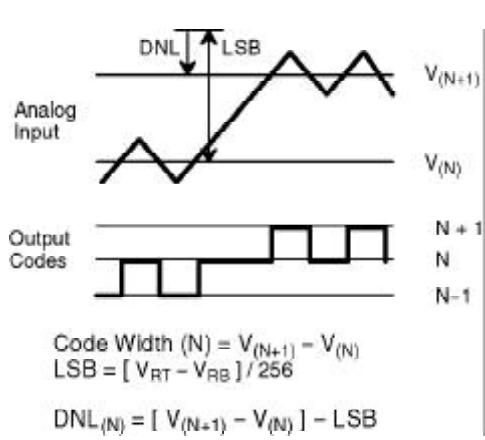


Figure 2. DNL Measurement

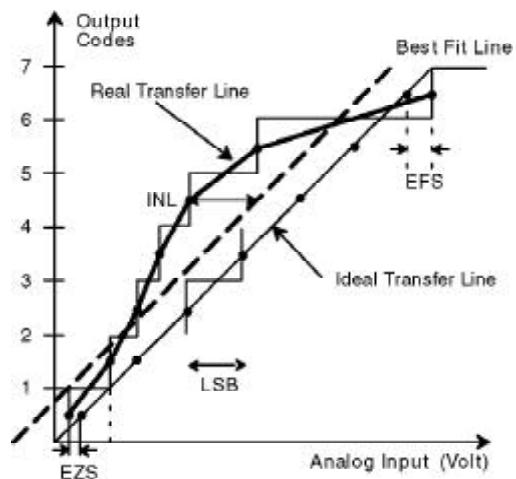


Figure 3. INL Error Calculation

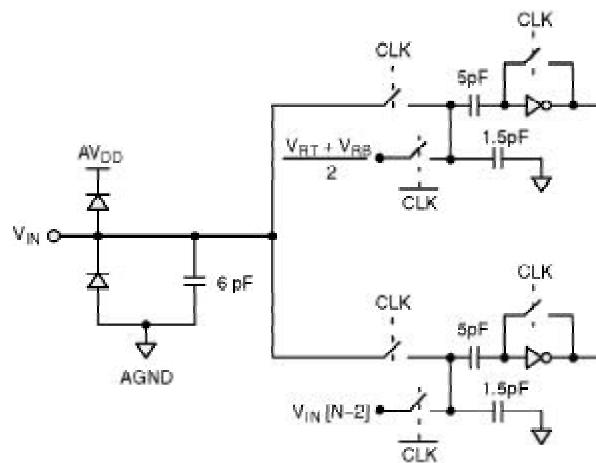


Figure 4. Equivalent Input Circuit

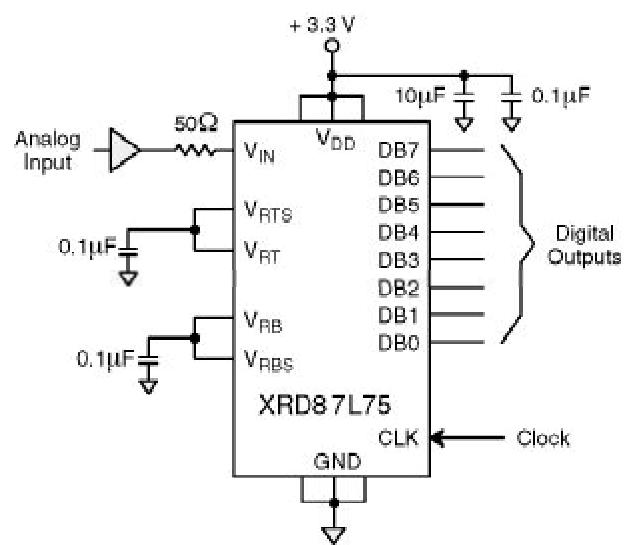


Figure 5. Typical Circuit Connections

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APPLICATION NOTES

Signals should not exceed $AV_{DD} + 0.5V$ or go below $AGND - 0.5V$ or $DV_{DD} + 0.5V$ or $DGND - 0.5V$. All pins have internal protection diodes that will protect them from short transients ($<100\mu s$) outside the supply range.

AGND and DGND pins are connected internally through the P-substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

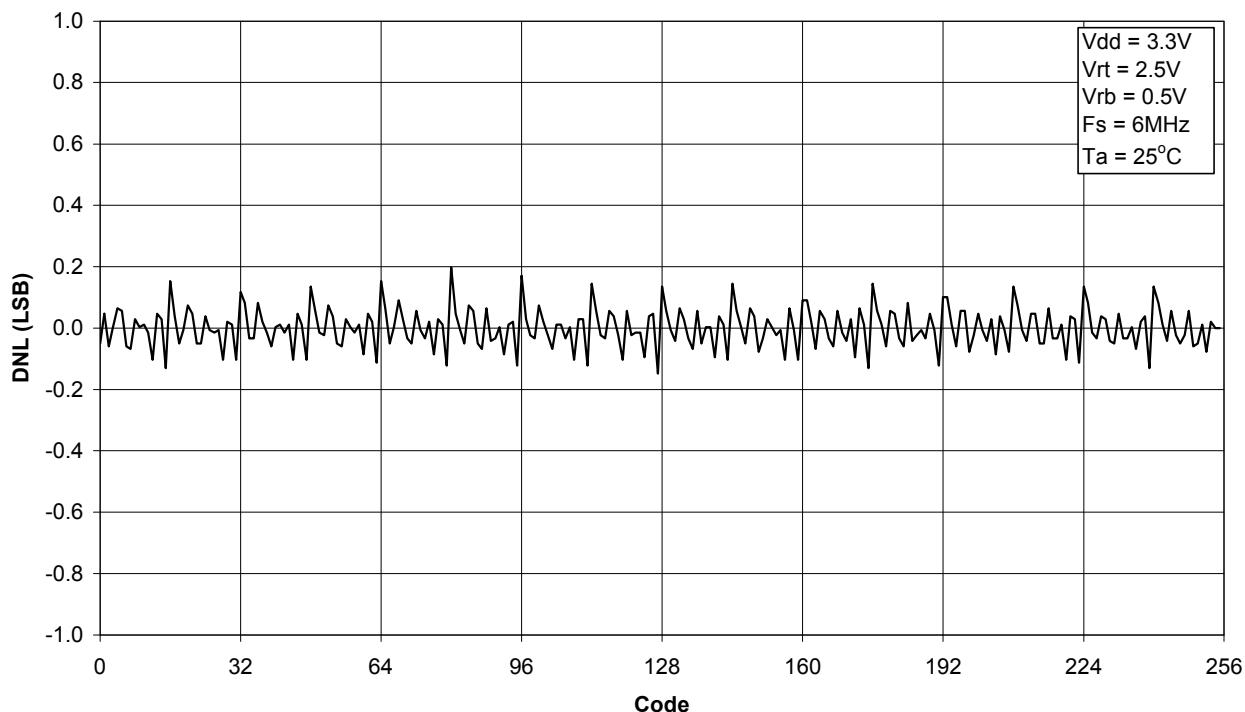
The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with $0.1\mu F$ and $10\mu F$ capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

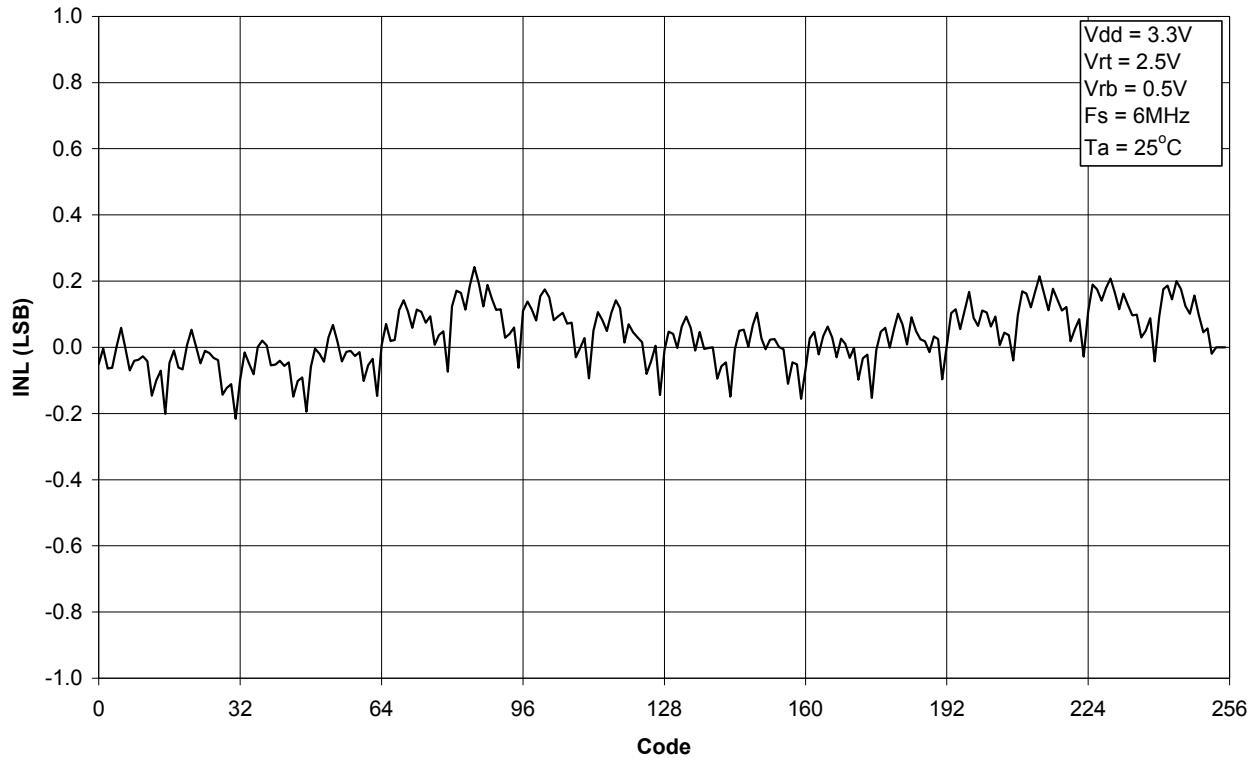
To avoid timing errors, use the rising edge of the sample clock (CLK) to latch data from the XRD87L75 to other parts of the system.

The reference can be biased internally by shorting V_{RT} to V_{RTS} and V_{RB} to V_{RBS} . This will generate $0.4V$ at V_{RB} and $1.72V$ at V_{RT} (see *Figure 5*).

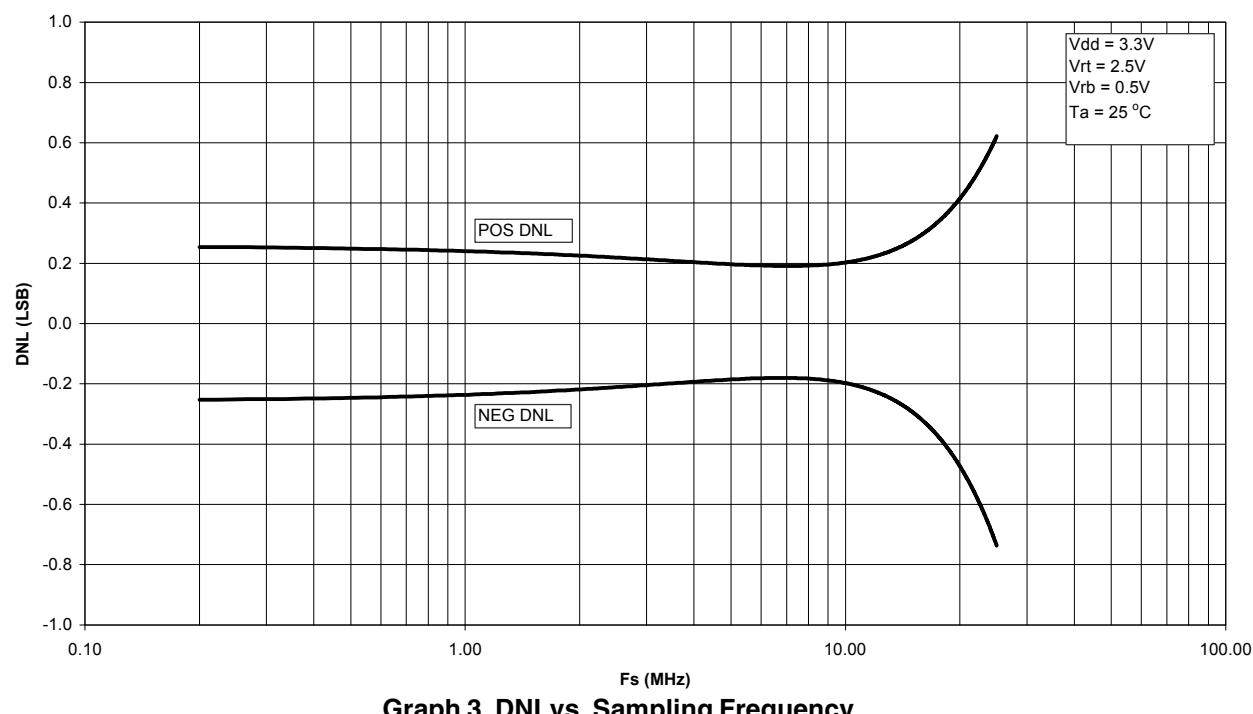
If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.



Graph 1. DNL vs. Code



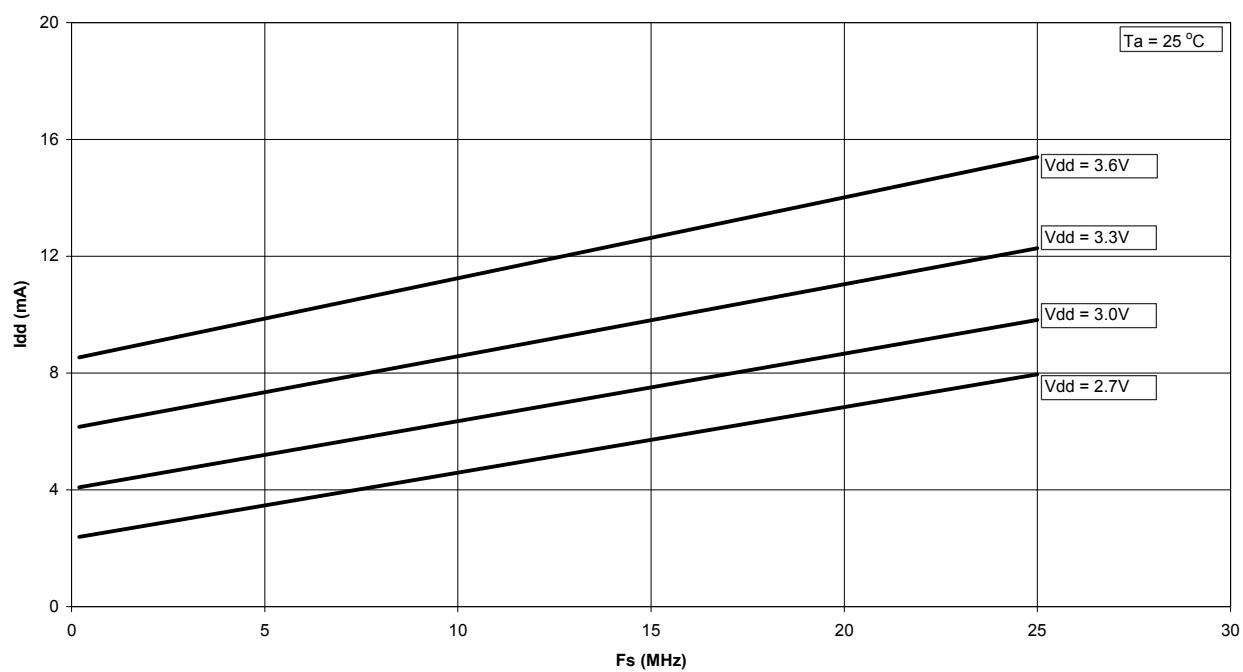
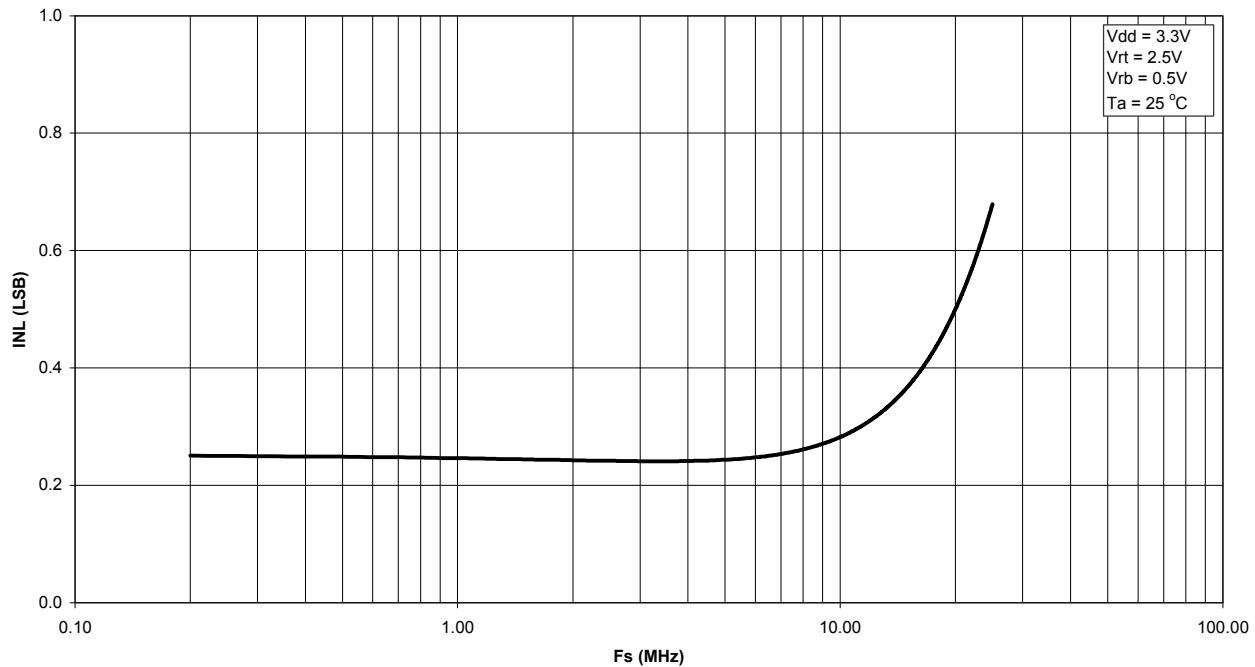
Graph 2. INL vs. Code



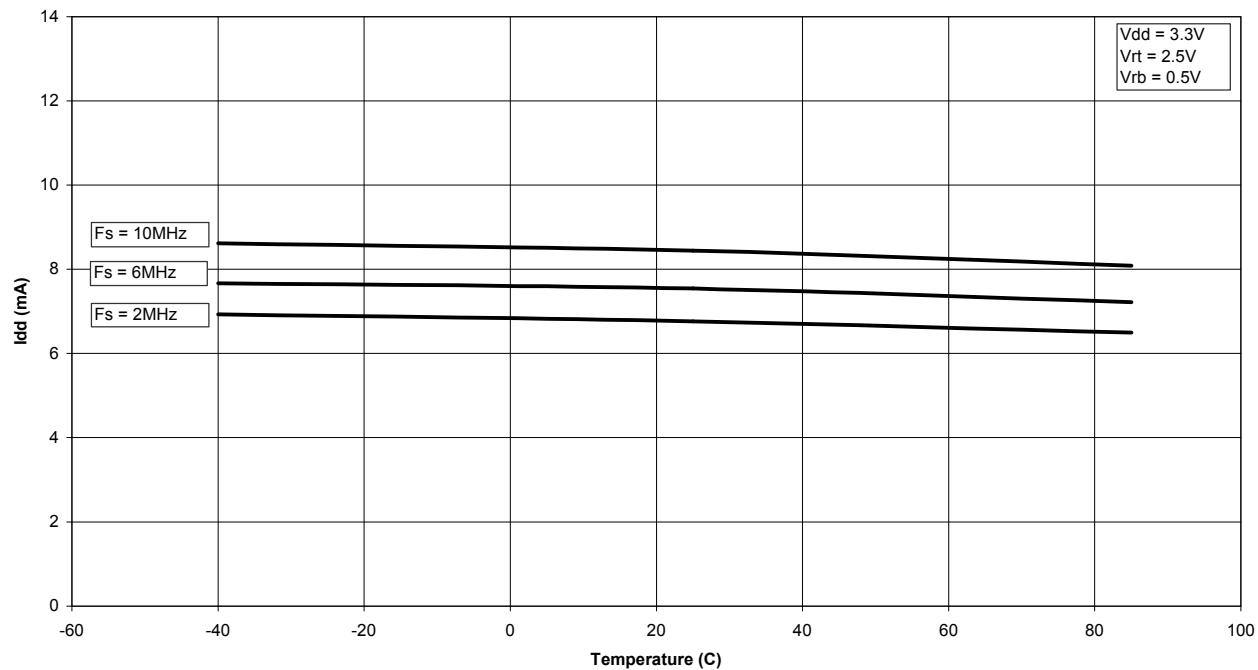
Graph 3. DNLvs. Sampling Frequency

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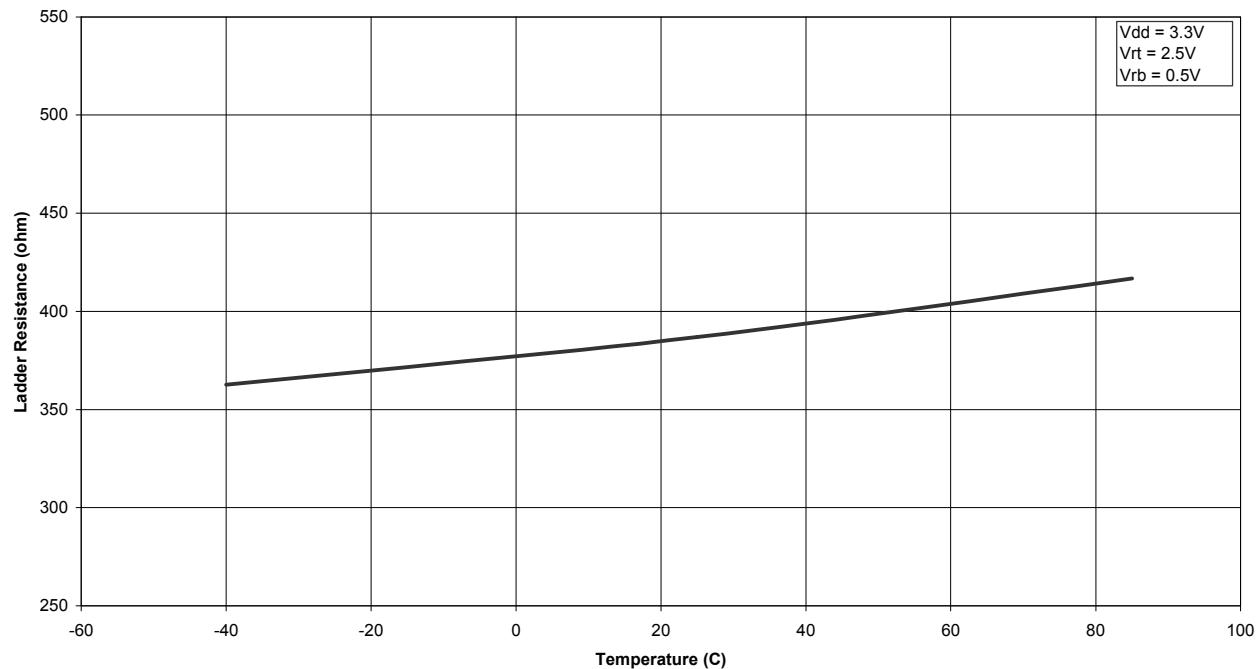
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Graph 5. IDD vs. Sampling Frequency



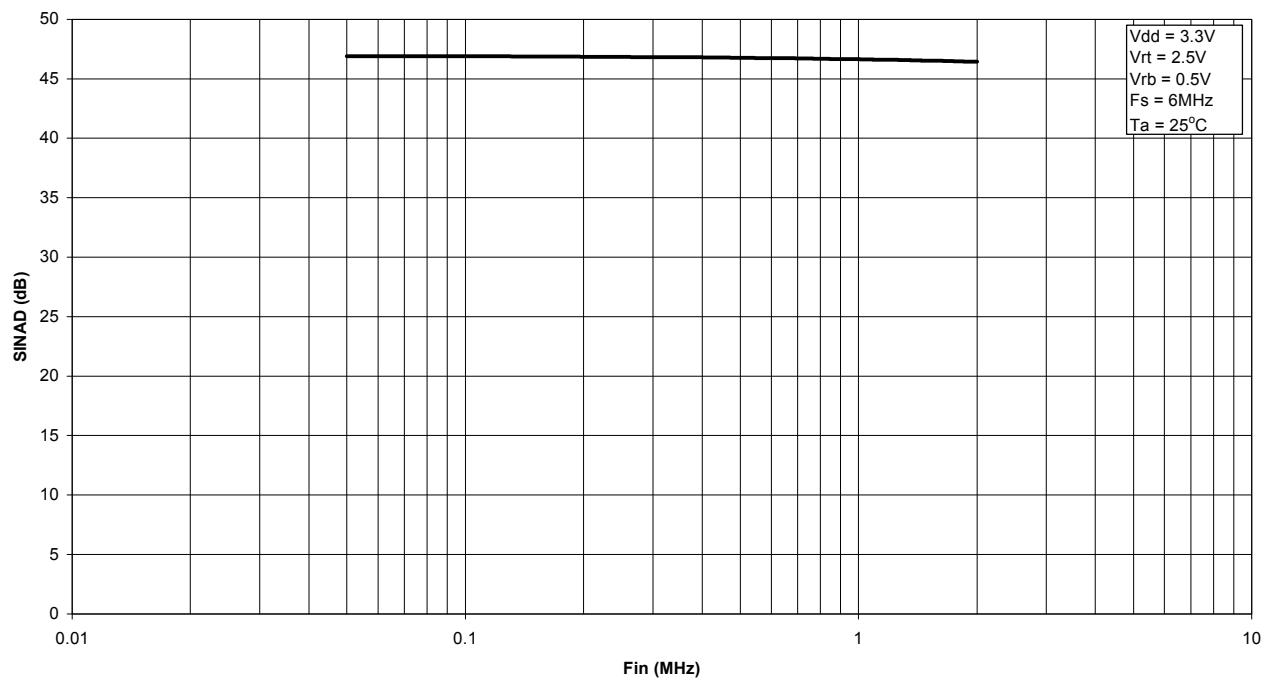
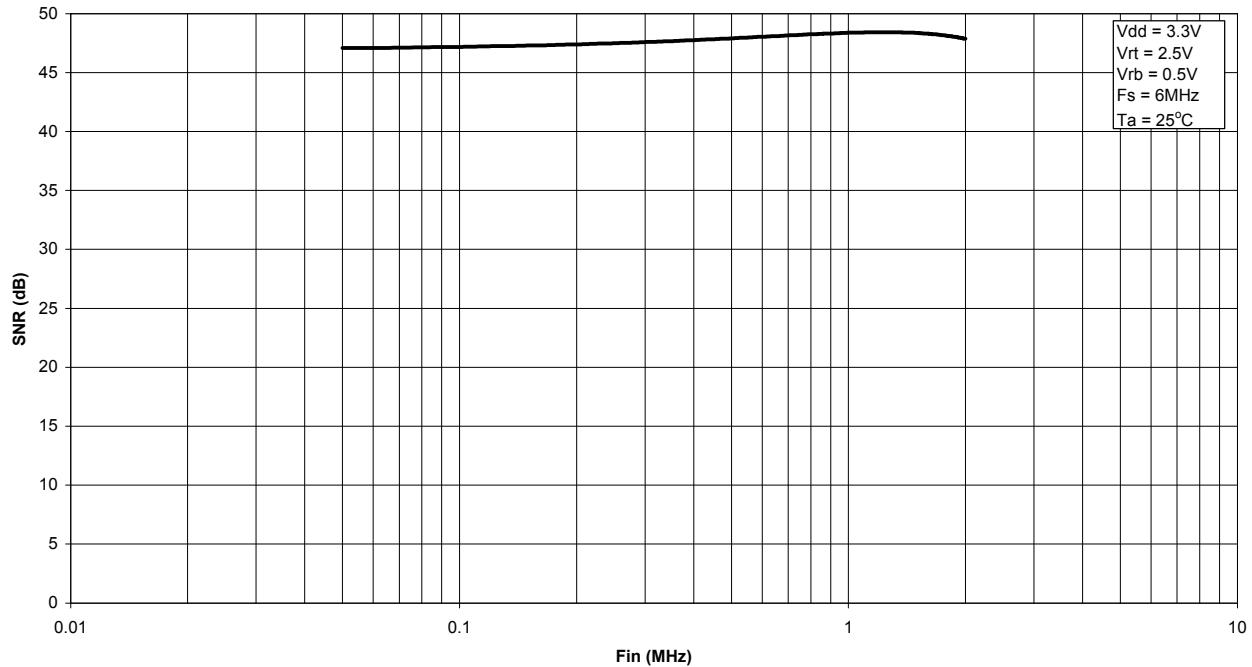
Graph 6. Supply Current vs. Temperature



Graph 7. Ladder Resistance vs. Temperature

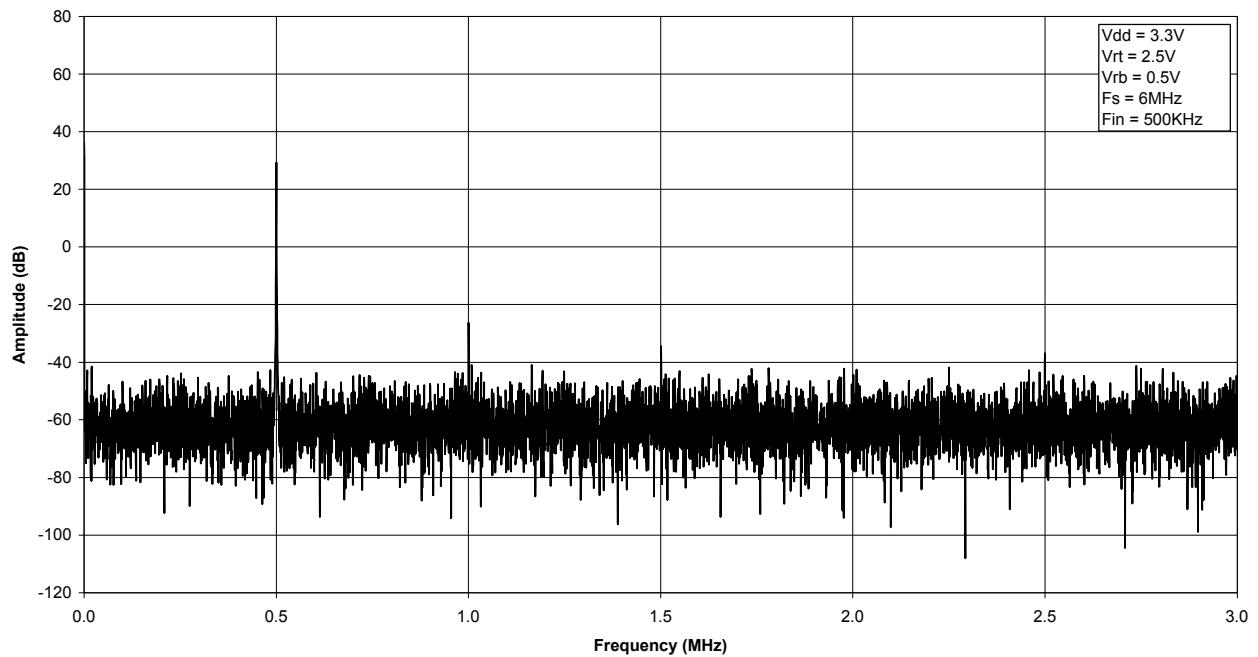
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Graph 10. FFT Plot

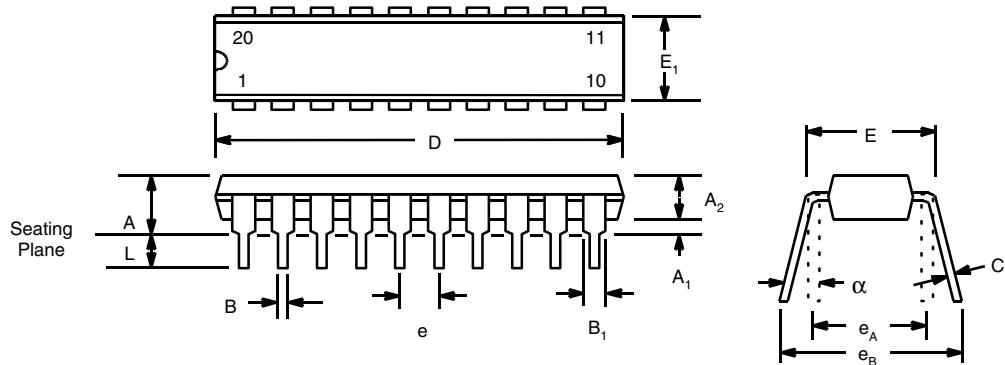


Graph 10. FFT Plot

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20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
REV. 1.00

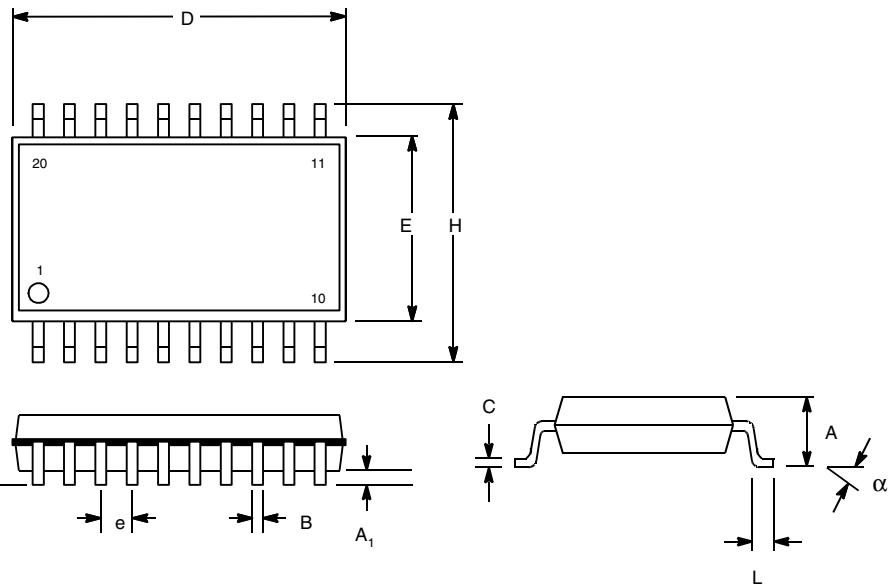


Note: The control dimension is the inch column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A1	0.015	0.070	0.38	1.78
A2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.925	1.060	23.50	26.92
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eA	0.300 BSC		7.62 BSC	
eB	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
a	0°	15°	0°	15°

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**20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)**
REV. 1.00



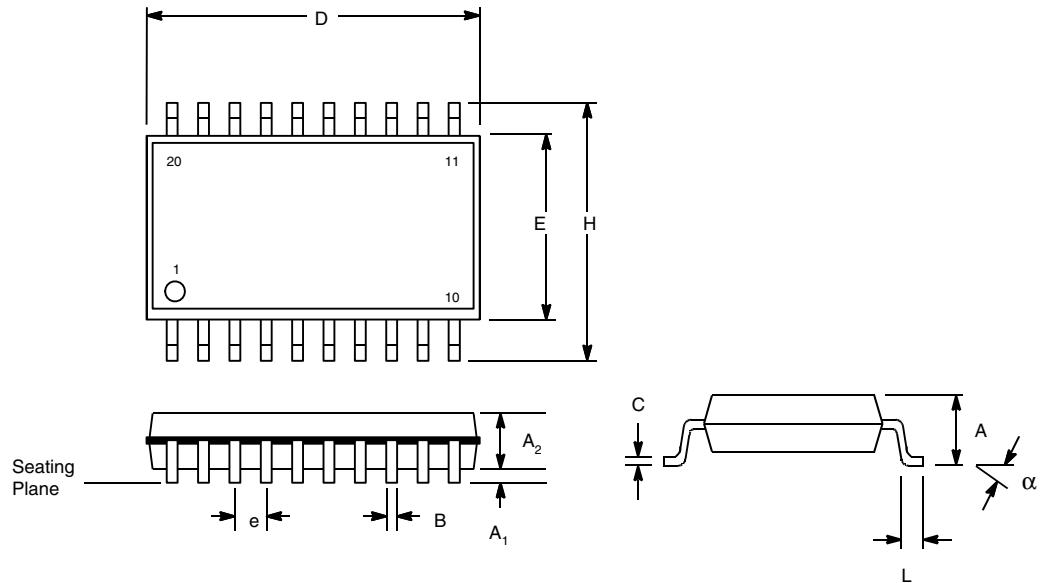
NOTE: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.496	0.512	12.60	13.00
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
a	0°		8°	

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**20 LEAD SHRINK SMALL OUTLINE PACKAGE
(5.3 mm SSOP)**
REV. 2.00



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.067	0.079	1.70	2.00
A1	0.002	0.006	0.05	0.15
A2	0.065	0.073	1.65	1.85
B	0.009	0.015	0.22	0.38
C	0.004	0.010	0.09	0.25
D	0.272	0.296	6.90	7.50
E	0.197	0.221	5.00	5.60
e	0.0256 BSC		0.65 BSC	
H	0.292	0.323	7.40	8.20
L	0.022	0.037	0.55	0.95
a	0°		8°	



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