3.3V 500MHz DUAL 1:10 HSTL FANOUT BUFFER/TRANSLATOR WITH 2:1 MUX INPUT

Precision Edge® SY89827L

FEATURES

- Dual LVPECL or HSTL input, 10 differential 1.5V HSTL compatible outputs
- Configurable as dual-channel 10 output or a single-channel 20 output clock driver
- Guaranteed AC parameters over temperature and voltage:
  - > 500MHz f_{MAX}
  - < 50ps within device skew
  - < 1.5ns propagation delay
  - < 700ps t_r / t_f time
- Low jitter design
  - < 1ps$_{RMS}$ cycle-to-cycle jitter
  - < 10ps$_{PP}$ total jitter
- 3.3V core supply, 1.8V output supply
- Output enable function
- Available in a 64-Pin EPAD-TQFP

APPLICATIONS

- High-performance PCs
- Workstations
- Parallel processor-based systems
- Other high-performance computing
- Communications

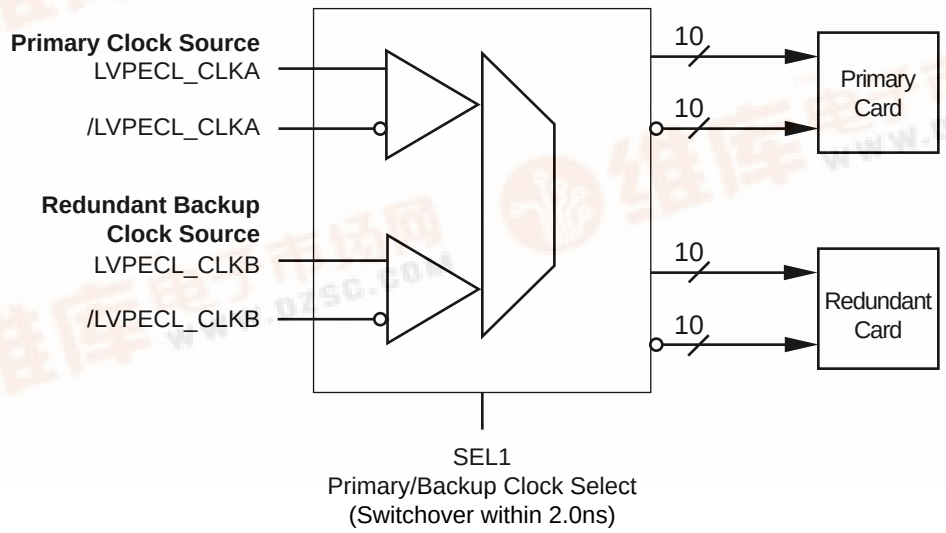
Precision Edge®

DESCRIPTION

The SY89827L is a High Performance Bus Clock Driver with dual 1:10 or single 1:20 HSTL (High Speed Transceiver Logic) output pairs. The part is designed for use in low voltage (3.3V/1.8V) applications which require a large number of outputs to drive precisely aligned, ultra low skew signals to their destination. The input is multiplexed from either HSTL or LVPECL (Low Voltage Positive Emitter Coupled Logic) by the CLK_SEL pin. The Output Enables (OE1 & OE2) are synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control.

The SY89827L features extremely low skew performance of <50ps over temperature and voltage – performance previously unachievable in a standard product having such a high number of outputs. The SY89827L is available in a single space saving package, enabling a lower overall cost solution. For applications that require greater HSTL fanout capability, consider the SY89824L.

TYPICAL APPLICATION CIRCUIT



System using SY89827L as a switchover circuit from a Primary Clock to a Redundant Backup Clock in a failsafe application. LVPECL inputs only, shown in this application.

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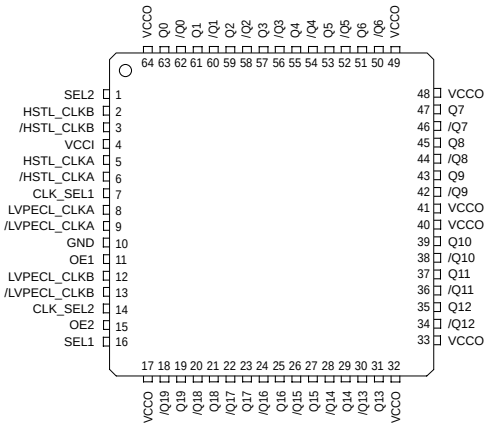
PACKAGE/ORDERING INFORMATION



64-Pin TQFP (H64-1)

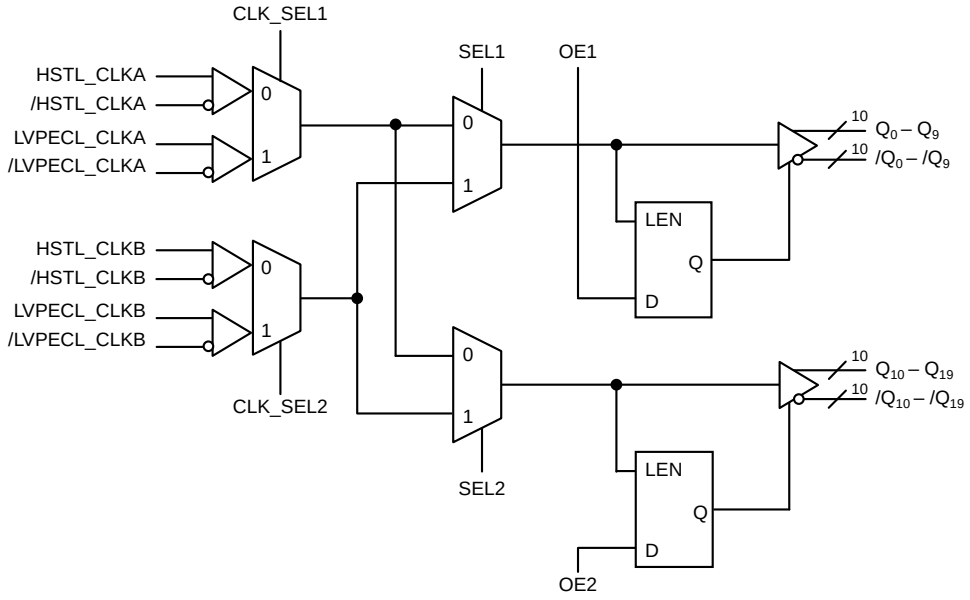
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89827LHI	H64-1	Industrial	SY89827LHI	Sn-Pb
SY89827LHITR[2]	H64-1	Industrial	SY89827LHI	Sn-Pb
SY89827LHY[3]	H64-1	Industrial	SY89827LHY with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89827LHYTR[2, 3]	H64-1	Industrial	SY89827LHY with Pb-Free bar-line indicator	Pb-Free Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

OE1[1]	OE2[1]	SEL1[1]	SEL2[1]	CLK_SEL1[1]	CLK_SEL2[1]	Q0 – Q9	/Q0 – /Q9	Q10 – Q19	/Q10 – /Q19
1	1	0	0	0	X	HSTL_CLKA	/HSTL_CLKA	HSTL_CLKA	/HSTL_CLKA
1	1	0	0	1	X	LVPECL_CLKA	/LVPECL_CLKA	LVPECL_CLKA	/LVPECL_CLKA
1	1	0	1	0	0	HSTL_CLKA	/HSTL_CLKA	HSTL_CLKB	/HSTL_CLKB
1	1	0	1	0	1	HSTL_CLKA	/HSTL_CLKA	LVPECL_CLKB	/LVPECL_CLKB
1	1	0	1	1	0	LVPECL_CLKA	/LVPECL_CLKA	HSTL_CLKB	/HSTL_CLKB
1	1	0	1	1	1	LVPECL_CLKA	/LVPECL_CLKA	LVPECL_CLKB	/LVPECL_CLKB
1	1	1	0	0	0	HSTL_CLKB	/HSTL_CLKB	HSTL_CLKA	/HSTL_CLKA
1	1	1	0	0	1	LVPECL_CLKB	/LVPECL_CLKB	HSTL_CLKA	/HSTL_CLKA
1	1	1	0	1	0	HSTL_CLKB	/HSTL_CLKB	LVPECL_CLKA	/LVPECL_CLKA
1	1	1	0	1	1	LVPECL_CLKB	/LVPECL_CLKB	LVPECL_CLKA	/LVPECL_CLKA
1	1	1	1	X	0	HSTL_CLKB	/HSTL_CLKB	HSTL_CLKB	/HSTL_CLKB
1	1	1	1	X	1	LVPECL_CLKB	/LVPECL_CLKB	LVPECL_CLKB	/LVPECL_CLKB
0	1	X	0	0	X	LOW	HIGH	HSTL_CLKA	/HSTL_CLKA
0	1	X	0	1	X	LOW	HIGH	LVPECL_CLKA	/LVPECL_CLKA
0	1	X	1	X	0	LOW	HIGH	HSTL_CLKB	/HSTL_CLKB
0	1	X	1	X	1	LOW	HIGH	LVPECL_CLKB	/LVPECL_CLKB
1	0	0	X	0	X	HSTL_CLKA	/HSTL_CLKA	LOW	HIGH
1	0	0	X	1	X	LVPECL_CLKA	/LVPECL_CLKA	LOW	HIGH
1	0	1	X	X	0	HSTL_CLKB	/HSTL_CLKB	LOW	HIGH
1	0	1	X	X	1	LVPECL_CLKB	/LVPECL_CLKB	LOW	HIGH
0	0	X	X	X	X	LOW	HIGH	LOW	HIGH

Note 1. Input has internal pull-up Floating input = 1.

PIN DESCRIPTIONS

Pin Number	Pin Name	I/O	Type	Internal P/U	Pin Function
5, 6	HSTL_CLKA /HSTL_CLKA	Input	HSTL		Differential clock input selected by CLK_SEL1, SEL1 and SEL2. Can be left floating if not selected. Floating input, if selected produces an indeterminate output. HSTL input signal requires external termination 50Ω-to-GND.
2, 3	HSTL_CLKB /HSTL_CLKB	Input	HSTL		Differential clock input selected by CLK_SEL1, SEL1 and SEL2. Can be left floating if not selected. Floating input, if selected produces an indeterminate output. HSTL input signal requires external termination 50Ω-to-GND.
8, 9	LVPECL_CLKA /LVPECL_CLKA	Input	LVPECL	75kΩ pull-down	Differential clock input selected by CLK_SEL1, SEL1 and SEL2. Can be left floating. Floating input, if selected produces a LOW at output. Requires external termination. See Figure 1.
12, 13	LVPECL_CLKB /LVPECL_CLKB	Input	LVPECL	75kΩ pull-down	Differential clock input selected by CLK_SEL2, SEL1 and SEL2. Requires external termination. See Figure 1.
7	CLK_SEL1	Input	LVTTL/ CMOS	11kΩ Pull-up	Selects HSTL_CLKA input when LOW and LVPECL_CLKA input when HIGH.
14	CLK_SEL2	Input	LVTTL/ CMOS	11kΩ Pull-up	Selects HSTL_CLKB input when LOW and LVPECL_CLKB input when HIGH.
16	SEL1	Input	LVTTL/ CMOS	11kΩ Pull-up	Selects input source CLKA when LOW and CLKB when HIGH for outputs Q0 – Q9 and /Q0 – /Q9.
1	SEL2	Input	LVTTL/ CMOS	11kΩ Pull-up	Selects input source CLKA when LOW and CLKB when HIGH for outputs Q10 – Q19 and /Q10 – /Q19.
11	OE1	Input	LVTTL/ CMOS	11kΩ Pull-up	Enable input synchronized internally to prevent glitching of the Q0 – Q9 and /Q0 – /Q9 outputs.
15	OE2	Input	LVTTL/ CMOS	11kΩ Pull-up	Enable input synchronized internally to prevent glitching of the Q10 – Q19 and /Q10 – /Q19 outputs.
4	VCCI	Power			Core VCC connected to 3.3V supply. Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to VCC pins as possible.
17, 32, 33, 40, 41, 48, 49, 64	VCCO	Power			Output buffer VCC connected to 1.8V nominal supply. All VCCO pins should be connected together on the PCB. Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to VCCO pins as possible.
10	GND	Power			Ground.
63, 61, 59, 57, 55 53, 51, 47, 45, 43	Q0 – Q9	Output	HSTL		Differential clock outputs from CLKA when SEL1 = LOW and from CLKB when SEL1 = HIGH. HSTL outputs (Q and /Q) must be terminated with 50Ω-to-GND. Q outputs are static when OE1 = LOW. Unused output pairs may be left floating.
62, 60, 58, 56, 54 52, 50, 46, 44, 42	/Q0 – /Q9	Output	HSTL		Differential clock outputs (complement) from CLKA when SEL1 = LOW and from CLKB when SEL1 = HIGH. HSTL outputs (Q and /Q) must be terminated with 50Ω-to-GND. /Q outputs are static HIGH when OE1 = LOW. Unused output pairs may be left floating.
39, 37, 35, 31, 29	Q10 – Q19 27, 25, 23, 21, 19	Output	HSTL		Differential outputs from CLKA when SEL2 = LOW and from CLKB when SEL2 = HIGH. HSTL outputs (Q and /Q) must be terminated with 50Ω-to-GND. Q outputs are static LOW when OE2 = LOW. Unused output pairs may be left floating.
38, 36, 34, 30, 28	/Q10 – /Q19 26, 24, 22, 20, 18	Output	HSTL		Differential outputs (complement) from CLKA when SEL2 = LOW and from CLKB when SEL2 = HIGH. HSTL outputs (Q and /Q) must be terminated with 50Ω-to-GND. /Q outputs are static HIGH when OE2 = LOW. Unused output pairs may be left floating.

Absolute Maximum Ratings(Note 1)

Power Supply Voltage (V_{CCI}, V_{CCO}) ..... –0.5 to +4.0V
Input Voltage (V_{IN}) ..... –0.5 to V_{CCI}
Output Current (I_{OUT}) ..... –50mA
Lead Temperature (T_{LEAD}, Soldering, 20sec.) ..... 260°C
Storage Temperature (T_S) ..... –65 to +150°C
ESD Rating, **Note 3** ..... >1kV

Operating Ratings(Note 2)

Supply Voltage
(V_{CCI}) ..... +3.3V to +3.47V
(V_{CCO}) ..... +1.6V to +2.0V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
TQFP (θ_{JA})
Exposed pad soldered to GND, **Note 4**
Still-Air (multi-layer PCB) ..... 23°C/W
–200lfpm (multi-layer PCB) ..... 18°C/W
–500lfpm (multi-layer PCB) ..... 15°C/W
Exposed pad NOT soldered to GND (not recommended)
Still-Air (multi-layer PCB) ..... 44°C/W
–200lfpm (multi-layer PCB) ..... 36°C/W
–500lfpm (multi-layer PCB) ..... 30°C/W
TQFP (θ_{JC}) ..... 4.4°C/W

DC ELECTRICAL CHARACTERISTICS

Power Supply: T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CCI}	V_{CC} Core		3.13	3.3	3.47	V
V_{CCO}	V_{CC} Output		1.6	1.8	2.0	V
I_{CCI}	I_{CC} Core	No Load		140	170	mA

HSTL Input/Output: V_{CCI} = 3.3V ±5%, V_{CCO} = 1.8V ±10%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	**Note 5**	1.0		1.2	V
V_{OL}	Output LOW Voltage	**Note 5**	0.2		0.4	V
V_{IH}	Input HIGH Voltage		V_X +0.1		1.6	V
V_{IL}	Input LOW Voltage		–0.3		V_X –0.1	V
V_X	Input Crossover Voltage		0.68		0.9	V
I_{IH}	Input HIGH Current		+20		–350	µA
I_{IL}	Input LOW Current				–500	µA

Note 1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Devices are ESD sensitive. Handling precautions recommended.

Note 4. It is highly recommended to solder the exposed pad of the EPAD-TQFP package to a ground plane on the PCB for maximum thermal efficiency.

Note 5. Outputs loaded with 50Ω-to-ground.

DC ELECTRICAL CHARACTERISTICS

LVPECL Input: V_{CCI} = 3.3V ±5%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage (Single-Ended)		V_{CCI} –1.165		V_{CCI} –0.880	V
V_{IL}	Input LOW Voltage		V_{CCI} –1.945		V_{CCI} –1.625	V
V_{PP}	Minimum Input Swing (LVPECL_CLK)	**Note 6**	300			mV
V_{CMR}	Common Mode Range (LVPECL_CLK)	**Note 7**	GNDI +1.8		V_{CCI} –0.4	V
I_{IH}	Input HIGH Current				150	µA
I_{IL}	Input LOW Current		0.5			µA

Note 6. The V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay.

Note 7. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The numbers in the table are referenced to V_{CCI}. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.). V_{CMR} range varies 1:1 with V_{CCI}. V_{CMR} (min) is fixed at GNDI +1.8V

CMOS/LVTTL Inputs: V_{CCI} = 3.3V ±5%, V_{CCO} = 1.8V ±10%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		+20		–250	µA
I_{IL}	Input LOW Current				–600	µA

AC ELECTRICAL CHARACTERISTICS(NOTE 1)

V_{CCI} = 3.3V ±5%, V_{CCO} = 1.8V ±10%, T_A = –40°C to +85°C, all outputs loaded, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Toggle Frequency	**Note 2**	500			MHz
t_{PD}	Differential Propagation Delay	**Note 3**	1.0	1.3	1.5	ns
V_{PP}	Minimum Input Swing, **Note 4**	HSTL PECL	200 150			mV mV
t_{SW}	Switchover Time	CLK_SEL-to-Q SEL-to-Q		1.6 1.4	2.0 1.75	ns ns
t_{JITTER}	Cycle-to-Cycle	**Note 8**			<1	ps_{RMS}
	Total Jitter	**Note 9**			<10	ps_{PP}
$t_{S(OE)}$	Output Enable Set-Up Time	**Note 5**	1.0			ns
$t_{H(OE)}$	Output Enable Hold Time	**Note 5**	0.5			ns
t_{skew}	Within Device Skew	**Note 6** 0°C to +85°C –40°C		25 35	50 75	ps ps
	Part-to-Part Skew	**Note 7**			400	ps
t_r, t_f	Output Rise/Fall Times (20% to 80%)			450	700	ps

Note 1. Outputs loaded with 50Ω-t- ground.

Note 2. f_{MAX} is defined as the maximum toggle frequency, measured with a 750mV LVPECL/HSTL input. HSTL output swing is > 400mV.

Note 3. Differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.

Note 4. The V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay.

Note 5. OE set-up time is defined with respect to the rising edge of the clock. OE HIGH-to-LOW transition ensures outputs remain disabled during the next clock cycle. OE LOW-to-HIGH transition enables normal operation of the next input clock.

Note 6. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature. This parameters includes within bank skew and bank-to-bank skew.

Note 7. The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature.

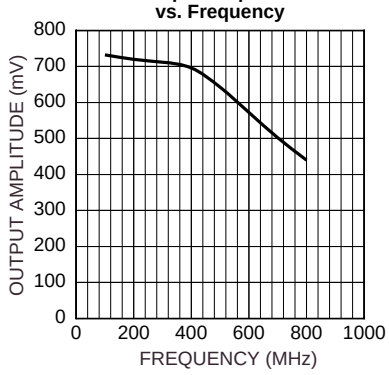
Note 8. Cycle-to-cycle jitter definition: The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n - T_{n+1}$ where T is the time between rising edges of the output signal.

Note 9. Total jitter definition: with an ideal clock input, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

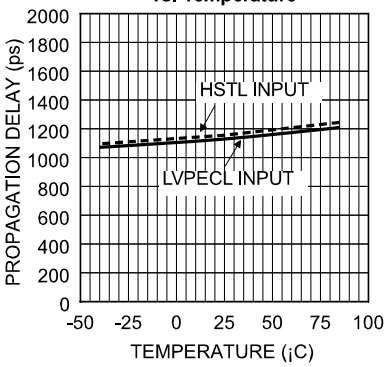
TYPICAL OPERATING CHARACTERISTICS

V_{CCI} = 3.3V, V_{CCO} = 1.8V, T_A = 25°C, unless otherwise stated.

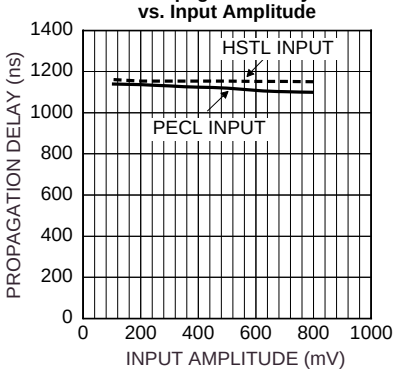
Output Amplitude vs. Frequency



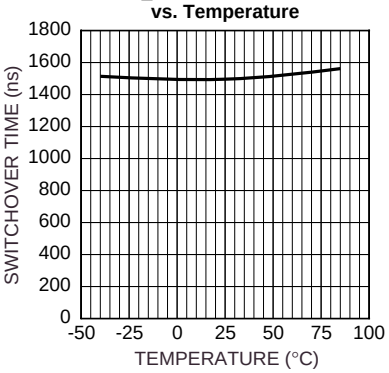
Propagation Delay vs. Temperature



Propagation Delay vs. Input Amplitude



CLK_SEL Switchover Time vs. Temperature



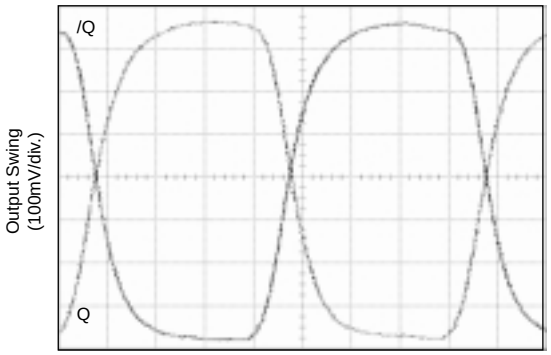
FUNCTIONAL CHARACTERISTICS

V_{CCI} = 3.3V, V_{CCO} = 1.8V, T_A = 25°C, unless otherwise stated.

100MHz Output

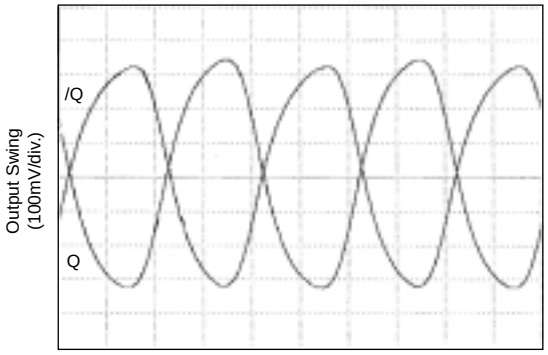
TIME (2ns/div.)

250MHz Output



TIME (500ps/div.)

500MHz Output



TIME (500ps/div.)

LVPECL/HSTL INPUTS

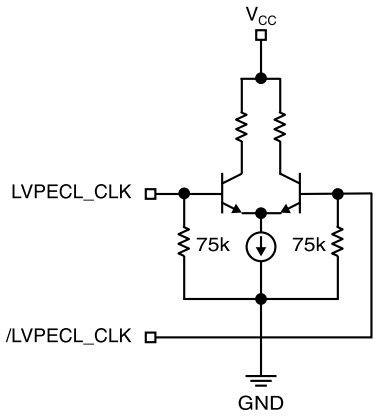


Figure 1. Simplified LVPECL Input Stage

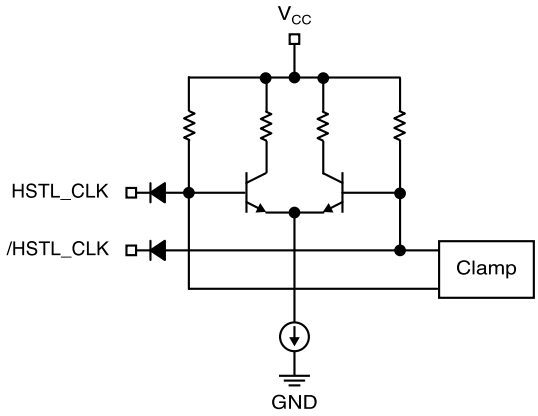


Figure 2. Simplified HSTL Input Stage

HSTL OUTPUTS

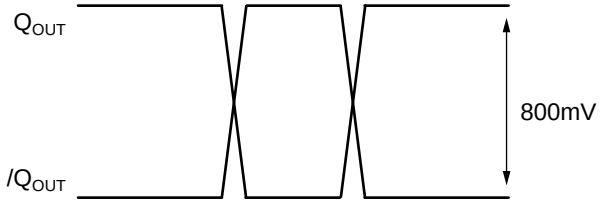


Figure 3. Output Driver Signal Levels (Single-Ended)

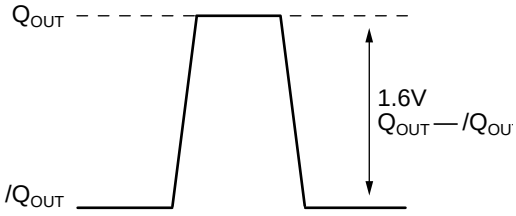
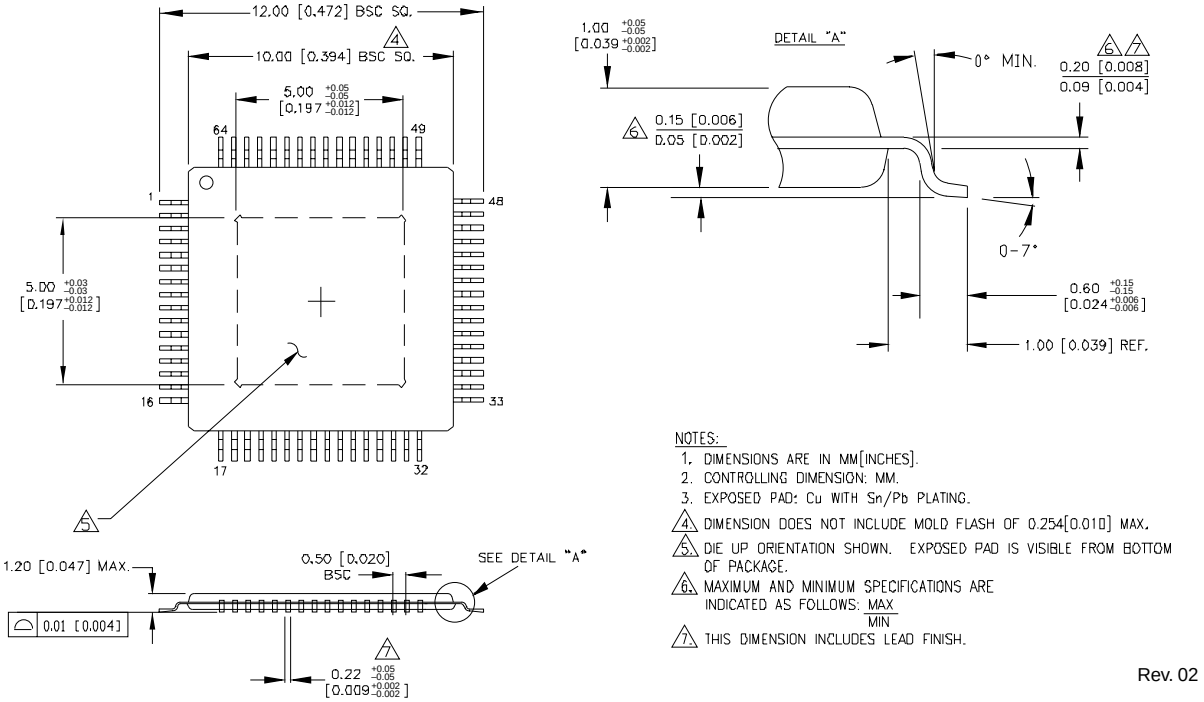


Figure 4. Output Driver Signal Levels (Differential)

RELATED PRODUCT AND SUPPORT DOCUMENTATION

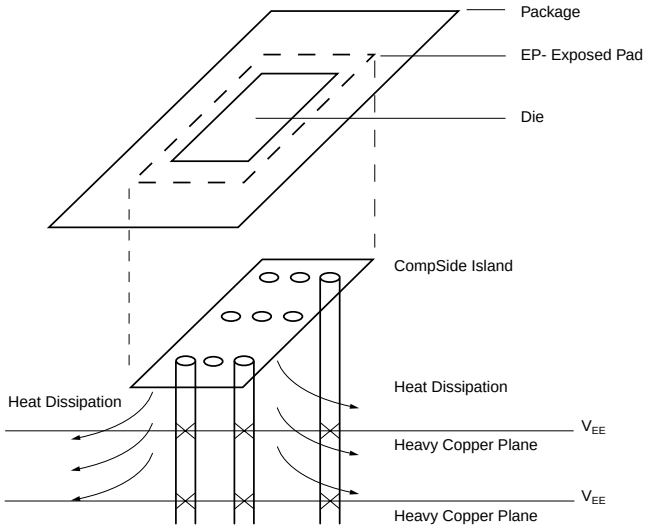
Part Number	Function	Data Sheet Link
SY89809L	3.3V 1:9 High-Performance, Low-Voltage Bus Clock Driver	www.micrel.com/product-info/products/sy89809l.shtml
SY89824L	3.3V 1:22 High-Performance, Low-Voltage Bus Clock Driver	www.micrel.com/product-info/products/sy89824l.html
	Exposed Pad Application Note	www.amkor.com/products/notes_papers/epad.pdf
M-0317	HBW Solutions	www.micrel.com/product-info/products/solutions.shtml
MIC3775	750mA µCap Low-Voltage Low-Dropout Regulator	www.micrel.com/product-info/products/mic3775.shtml

64-PIN EPAD-TQFP (DIE UP) (H64-1)



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. EXPOSED PAD: Cu WITH Sn/Pb PLATING.
4. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
5. DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.
6. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN
7. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 02



PCB Thermal Consideration for 64-Pin EPAD-TQFP Package
(Always solder, or equivalent, the exposed pad to the PCB)

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