Data Sheet December 22, 2006 FN6141.0

6-Pin Voltage Supervisors with Pin-Selectable Voltage Trip Points

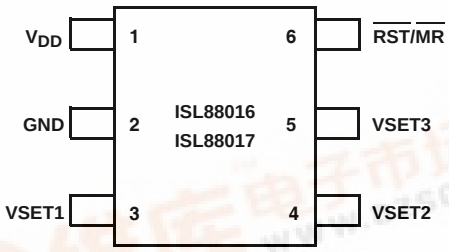
The ISL88016, ISL88017 supervisors offer pin-selectable voltage trip points along with popular functions such as Power-on Reset control, Supply Voltage Supervision, and Manual Reset assertion in a small 6 Ld TSOT-23 package.

By connecting the three VSET pins to V_{DD}, GND or floating, users can program the voltage trip point from 1.60V to 2.85V in 50mV increments on the ISL88016 and from 2.15V to 4.65V in 100mV increments on the ISL88017. These user-selectable reset threshold voltages are accurate to ±2% over temperature and the reset signal is valid down to 1V.

Intersil's proprietary TwinPin™ combines the active low reset out with the manual reset input into one pin. This provides device adjustability without sacrificing functionality. These parts are specifically designed for low power consumption and high threshold accuracy.

Pinout

ISL88016, ISL88017
(6 LD TSOT-23)
TOP VIEW



Features

- Pin-Selectable Single Voltage Monitoring Supervisors
- User Pin-Selectable Voltage Trip Points
  - **ISL88016**: 1.60V to 2.85V in 50mV Steps
  - **ISL88017**: 2.15V to 4.65V in 100mV Steps
- Reduce Inventory on Fixed Voltage Trip Point Options
- Manual Reset Capability
- Proprietary TwinPin™ Combines Active-Low Reset Output and Manual Reset Input Functions into One Pin
- Reset Signal Valid Down to V_{DD} = 0.8V
- Voltage Threshold ±2% Accuracy Over Temp
- No External Components Necessary
- Immune to Power-Supply Transients
- Ultra Low 3µA Supply Current
- Small 6 Ld TSOT-23 Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

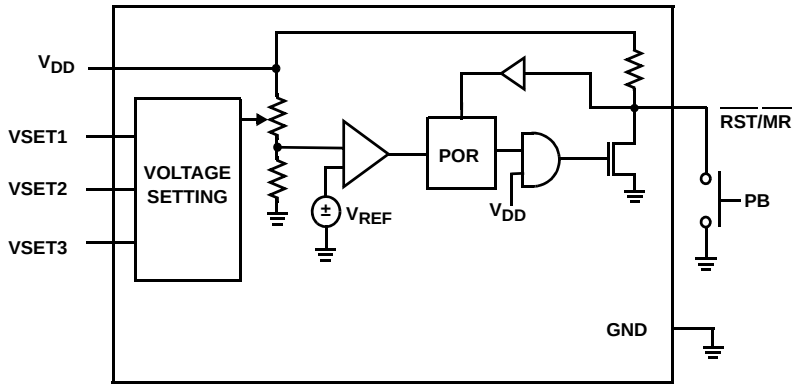
- Process Control Systems
- Intelligent Instruments
- Embedded Control Systems
- Computer Systems
- Portable/Battery-Powered Equipment
- PDA and Hand-Held PC Devices

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL88016IHTZ-T	016Z	3k pcs	6 Ld TSOT-23 Tape & Reel	MDP0049
ISL88017IHTZ-T	017Z	3k pcs	6 Ld TSOT-23 Tape & Reel	MDP0049
ISL88016IHTZ-TK	016Z	1k pcs	6 Ld TSOT-23 Tape & Reel	MDP0049
ISL88017IHTZ-TK	017Z	1k pcs	6 Ld TSOT-23 Tape & Reel	MDP0049
ISL88016/17EVAL1Z	Evaluation Platform			

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Functional Block Diagrams



ISL88016
ISL88017

Product Features Table

FUNCTION	ISL88016	ISL88017
Active-Low Reset ($\overline{RST}$)	x	x
Manual Reset Input ($\overline{MR}$)	x	x
1.60V to 2.85V (50mV Increments) Pin-Selectable Voltage Trip Range	x	
2.15V to 4.65V (100mV Increments) Pin-Selectable Voltage Trip Range		x
Pb-Free Package Option Available	x	x

Pin Descriptions

PIN	NAME	FUNCTION
1	V_{DD}	Supply Voltage and Monitored Input. The V_{DD} pin is the IC power supply terminal and also the monitored input. The voltage at this pin is compared against the programmed voltage trip point, V_{TP}. A reset is first asserted when the device is initially powered up to ensure that the power supply has stabilized. Thereafter, reset is again asserted whenever V_{DD} falls below V_{TH}. The device is designed with hysteresis to help prevent chattering due to noise and is immune to brief power-supply transients.
2	GND	Ground.
3	VSET1	Voltage Trip Point Select Pins 1, 2 and 3. These inputs are either tied either to GND or V_{DD} or left floating in various combinations to program the falling voltage trip point. See Voltage Trip Point Setting Table on following page for programming configurations.
4	VSET2	
5	VSET3	
6	$\overline{RST}$/$\overline{MR}$	Proprietary TwinPin™ technology combines Active-Low Reset Output and Manual Reset Input Functions into one pin. This dual function pin functions as both the reset output and a manual reset input. The $\overline{RST}$ output pin has an integrated 100k pull-up resistor to V_{DD} that is pulled to GND (LOW) when reset is asserted, V_{DD} < programmed voltage trip point. The $\overline{MR}$ input is an active-low debounced input to which a user can connect a push-button to add manual reset capability.

Power-On Reset Voltage Setting

V_{TH}		VSET1	VSET2	VSET3
ISL88016	ISL88017			
1.60	2.15	GND	GND	GND
1.65	2.25	FLOAT	GND	GND
1.70	2.35	V_{DD}	GND	GND
1.75	2.45	GND	FLOAT	GND
1.80	2.55	FLOAT	FLOAT	GND
1.85	2.65	V_{DD}	FLOAT	GND
1.90	2.75	GND	V_{DD}	GND
1.95	2.85	FLOAT	V_{DD}	GND
2.00	2.95	V_{DD}	V_{DD}	GND
2.05	3.05	GND	GND	FLOAT
2.10	3.15	FLOAT	GND	FLOAT
2.15	3.25	V_{DD}	GND	FLOAT
2.20	3.35	GND	FLOAT	FLOAT
2.25	3.45	FLOAT	FLOAT	FLOAT
2.30	3.55	V_{DD}	FLOAT	FLOAT
2.35	3.65	GND	V_{DD}	FLOAT
2.40	3.75	FLOAT	V_{DD}	FLOAT
2.45	3.85	V_{DD}	V_{DD}	FLOAT
2.50	3.95	GND	GND	V_{DD}
2.55	4.05	FLOAT	GND	V_{DD}
2.60	4.15	V_{DD}	GND	V_{DD}
2.65	4.25	GND	FLOAT	V_{DD}
2.70	4.35	FLOAT	FLOAT	V_{DD}
2.75	4.45	V_{DD}	FLOAT	V_{DD}
2.80	4.55	GND	V_{DD}	V_{DD}
2.85	4.65	FLOAT	V_{DD}	V_{DD}
Reserved	Reserved	V_{DD}	V_{DD}	V_{DD}

Absolute Maximum Ratings

Temperature Under Bias . . . . . .-40°C to +125°C
Storage Temperature . . . . . .-65°C to +150°C
Voltage on Any Pin with Respect to GND . . . . . .-1.0V to +7V
D.C. Output Current. 5mA
Lead Temperature (Soldering, 10s) . . . . . .+300°C

Recommended Operating Conditions

Temperature Range (Industrial) . . . . . .-40°C to +85°C

CAUTION: Absolute Maximum Ratings indicate limits beyond which permanent damage to the device and impaired reliability may occur. These are stress ratings provided for information only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied.

For guaranteed specifications and test conditions, see Electrical Specifications. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS						
V_{DD}	Supply Voltage Range		1.6		5.5	V
I_{DD}	ISL88016 Supply Current $V_{DD} > V_{TH}$	V_{DD} = 5.0V		4.3	6	µA
		V_{DD} = 3.3V		3.1	4.9	µA
		V_{DD} = 2.5V		3.1	4.5	µA
		V_{DD} = 1.8V		2.5	4.4	µA
	ISL88017 Supply Current $V_{DD} > V_{TH}$	V_{DD} = 5.0V		4.0	8.5	µA
		V_{DD} = 3.3V		3.2	8.5	µA
		V_{DD} = 2.5V		3.2	6.5	µA
		V_{DD} = 2.25V		3.0	5.4	µA
VOLTAGE THRESHOLD						
V_{TH}	V_{DD} Voltage Trip Point	See Power-On Reset Voltage Setting Table on page 3	-2		+2	%
V_{THHYST}	Hysteresis at VTH Input Temperature = +25°C			1		%
RESET						
V_{OL}	ISL88016 Reset Output Voltage Low	$V_{DD} < V_{TH,}$ Sinking 0.225mA		0.20	0.5	V
	ISL88017 Reset Output Voltage Low	$V_{DD} < V_{TH,}$ Sinking 0.225mA		0.20	0.5	V
V_{OH}	Reset Output Voltage High	$V_{DD} > V_{TH}$		V_{DD}		V
t_{POR}	POR Time-Out Delay		140	200	280	ms
t_{RST}	V_{TH} Low to Reset Asserted Delay	V_{DD} Open		0.01		µs
C_{LOAD}	Load Capacitance on Reset Pin			5		pF
MANUAL RESET						
V_{MR}	$\overline{MR}$ Input Voltage				100	mV
t_{MR}	$\overline{MR}$ Minimum Pulse Width		10			µs
R_{PU}	Integrated $\overline{RST}$/$\overline{MR}$ Pull-Up Resistor			100		kΩ
VSET						
I_{VSET}	VSET Current				1	µA
V_{VSET}	VSET Open Pin Voltage	VSET = Open		$0.5V_{DD}$		V
V_{IL}	VSET Input Voltage Low				$0.1V_{DD}$	V
V_{IH}	VSET Input Voltage High		0.9 x V_{DD}			V

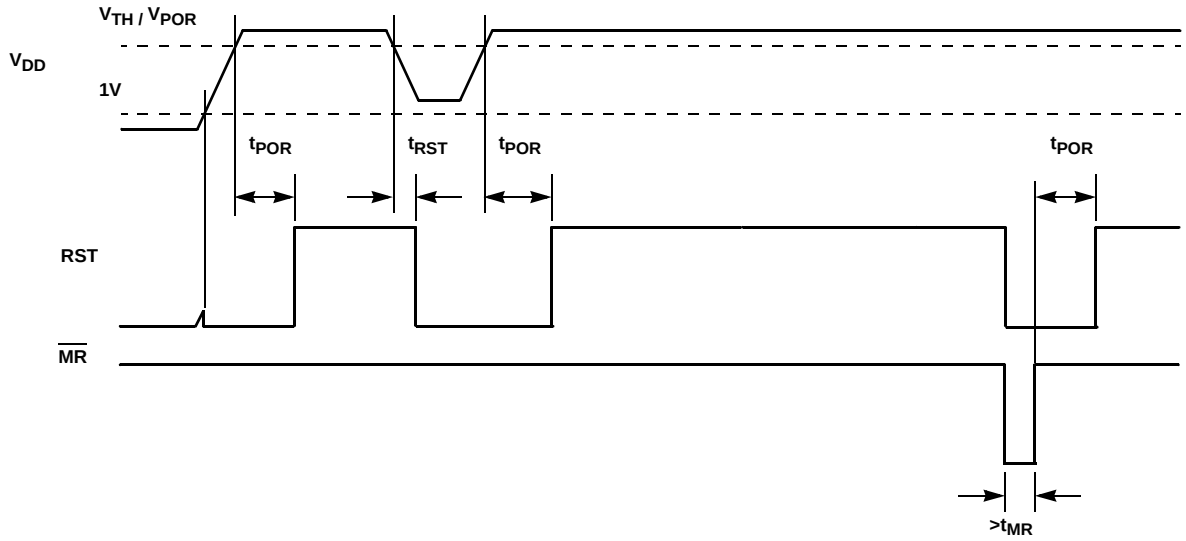


FIGURE 1. VOLTAGE MONITORING TIMING DIAGRAM

Principles of Operation

The ISL88016 and ISL88017 devices provides a low cost solution for those voltage monitoring applications needing supply voltage supervision with power reset control, and manual reset assertion. By integrating these common features along with three pins of Vth programming into a small 6 Ld TSOT-23 package and using only 1µA of supply current, the ISL88016 and ISL88017 devices can lower system cost, reduce board space requirements, and increase the reliability of a system while reducing inventory overhead costs.

Low Voltage Monitoring

During normal operation, the ISL88016 and ISL88017 monitor the voltage level of V_{DD}. The device asserts a reset ($\overline{RST}$ = LOW) if this voltage is less than the programmed voltage trip point. The reset signal prevents system operation during a power failure or brownout condition. This reset signal remains asserted until V_{DD} exceeds the voltage threshold setting for the reset time delay period t_{POR}. (See Figure 1).

The ISL88016 and ISL88017 allow users to customize the Power-On Reset voltage threshold level, which is the voltage at which the reset is deasserted. The three VSET inputs are either tied to V_{DD}, GND or left open to program V_{TH}. See the Power-On Reset Voltage Setting table on page 3 for specific voltage configuration. Also see Figure 2 for a schematic representation of the VSET pins being programmed, noting the minimum necessary components for IC operation. Do not attempt to reprogram a V_{TH} while the IC is biased.

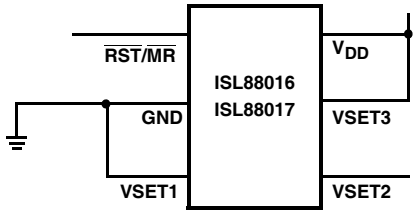


FIGURE 2. SETTING V_{POR} USING VSET INPUTS

Power-On Reset (POR)

Applying power to the ISL88016 and ISL88017 activates a POR circuit which asserts reset once V_{DD} = 1 V. (i.e., $\overline{RST}$ goes LOW). This provides several benefits:

- It prevents the system microprocessor from starting to operate with insufficient voltage.
- It prevents the processor from operating prior to stabilization of the oscillator.
- It ensures that the monitored device is held out of operation until internal registers are properly loaded.
- It allows time for an FPGA to download its configuration prior to initialization of the circuit.

The reset signal remains asserted until V_{DD} rises above the minimum voltage sense level for time period t_{POR}. This ensures that the V_{DD} voltage has stabilized.

Optional V_{DD} de-coupling capacitance can be added to filter transients if needed.

Manual Reset

The manual reset input ($\overline{MR}$) allows the user to trigger a reset by using a push-button switch. The $\overline{MR}$ input is an active low debounced input. By connecting a push-button directly from $\overline{MR}$ to ground, the designer adds manual system reset capability (see Figure 3). Reset is asserted if the $\overline{MR}$ pin is pulled low to less than 100mV for 10µs or longer while the push-button is closed. After $\overline{MR}$ is released, the reset outputs remain asserted for t_{POR} (200ms) and then released.

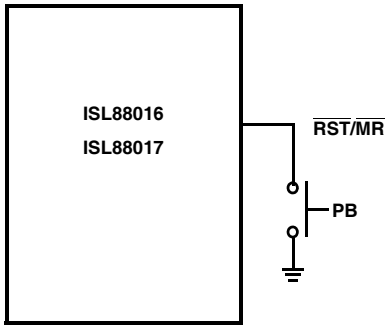


FIGURE 3. CONNECTING A MANUAL RESET PUSH-BUTTON

Using the ISL88016/17EVAL1Z Platform

The ISL88016/17EVAL1Z platform is provided with both an ISL88016 in the top and an ISL88017 in the bottom positions. Each IC is default programmed to VSET1, VSET2 and VSET3 = FLOAT but provided with jumpers to change the Vth level by individually connecting the three VSET pins to either V_{DD} (1) or GND (0). To the left of the circuits is a VSET programming table for easy reference. Provide adequate bias to V_{DD} to deassert $\overline{RESET}$ signal. See Figure 4 for the ISL88016/17EVAL1Z schematic and Figure 5 for its photograph.

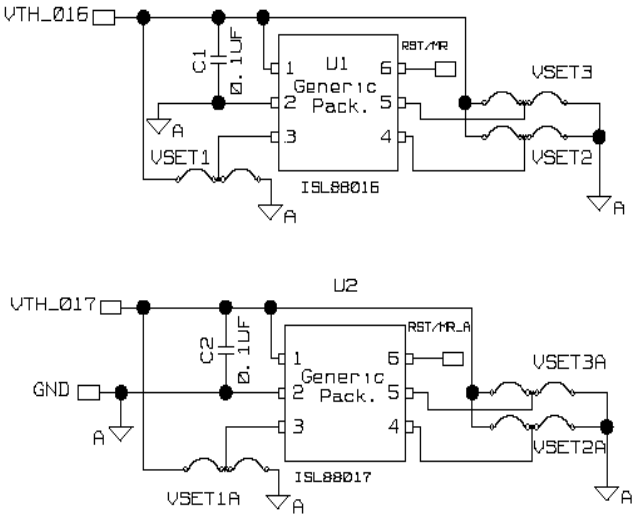


FIGURE 4. ISL88016/17EVAL1Z SCHEMATIC

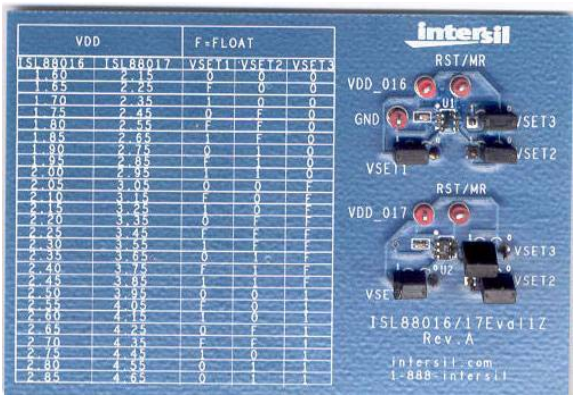


FIGURE 5. ISL88016/17EVAL1Z PHOTOGRAPH

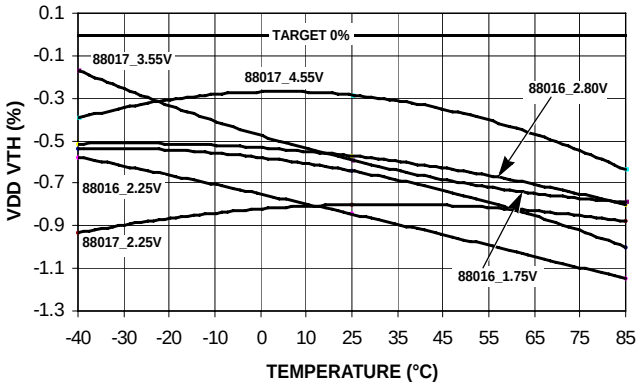


FIGURE 6. SAMPLED V_{TH}% TO TARGET OVER TEMP

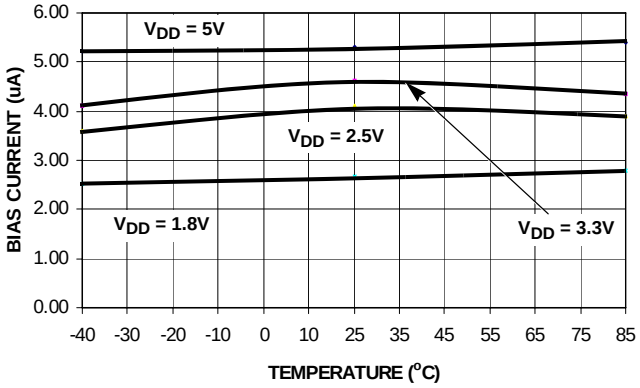


FIGURE 7. I_{DD} OVER TEMP

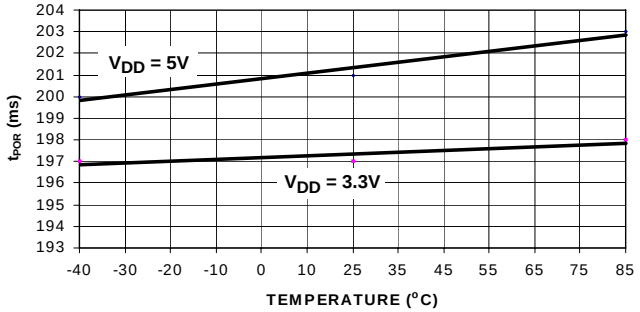
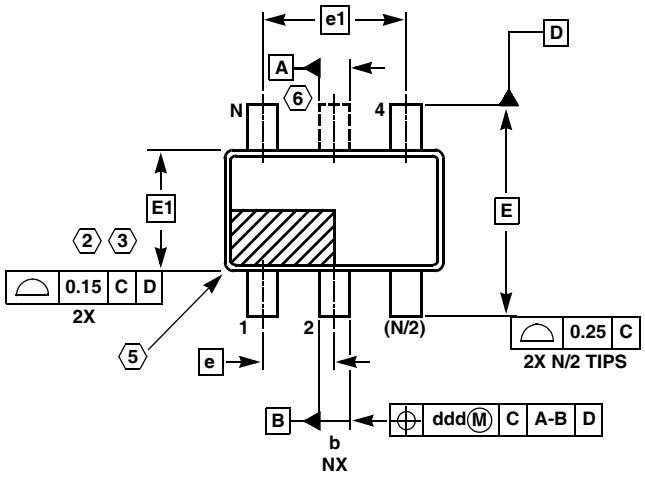
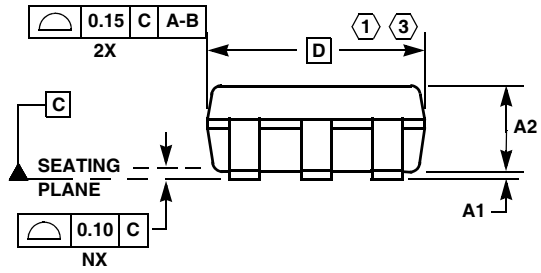
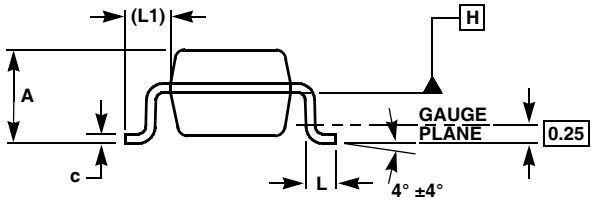


FIGURE 8. t_{POR} OVER TEMP

TSOT Package Family







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TSOT PACKAGE FAMILY

SYMBOL	TSOT5	TSOT6	TSOT8	TOLERANCE
A	1.00	1.00	1.00	Max
A1	0.05	0.05	0.05	±0.05
A2	0.87	0.87	0.87	±0.03
b	0.38	0.38	0.29	±0.07
c	0.127	0.127	0.127	+0.07/-0.007
D	2.90	2.90	2.90	Basic
E	2.80	2.80	2.80	Basic
E1	1.60	1.60	1.60	Basic
e	0.95	0.95	0.65	Basic
e1	1.90	1.90	1.95	Basic
L	0.40	0.40	0.40	±0.10
L1	0.60	0.60	0.60	Reference
ddd	0.20	0.20	0.13	-
N	5	6	8	Reference

Rev. A 12/02

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.15mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (TSOT6 AND TSOT8 only).
6. TSOT5 version has no center lead (shown as a dashed line).