



SPDT SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

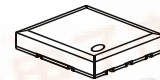
The NJG1647HD3 is a GaAs SPDT switch IC suited for the application of GSM, CDMA and UMTS handsets.

This switch features low distortion, high power handling and low insertion loss.

This device can operate a single bit control signal from +1.3V. This device has the low current consumption mode.

The ultra-small & ultra-thin USB6-D3 package is adopted.

■ PACKAGE OUTLINE



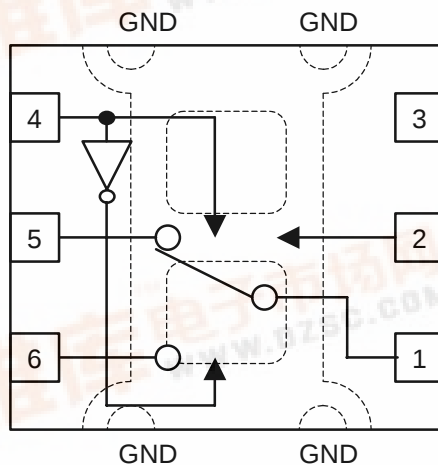
NJG1647HD3

■ FEATURES

- Low control voltage 1.3V min.
- Low operation voltage 2.5~+3.6V
- Low distortion IIP3=+70dBm typ. @ $P_{IN}=24\text{dBm}$, 2 tone, $V_{DD}=2.7\text{V}$
2nd harmonics=-70dBc max. @ $P_{IN}=35\text{dBm}$, $f=0.9\text{GHz}$
3rd harmonics=-70dBc max. @ $P_{IN}=35\text{dBm}$, $f=0.9\text{GHz}$
- Low insertion loss 0.25dB typ. @ $f=0.9\text{GHz}$, $P_{IN}=35\text{dBm}$, $V_{DD}=2.7\text{V}$
0.30dB typ. @ $f=1.9\text{GHz}$, $P_{IN}=33\text{dBm}$, $V_{DD}=2.7\text{V}$
- Ultra-small & ultra-thin package USB6-D3 (Package size: 2.0x1.8x0.8mm)

■ PIN CONFIGURATION

USB6-D3 Type (Top View)



Pin connection

1. PC
2. CTL2 (Option)
3. VDD
4. CTL1
5. P1
6. P2

■ TRUTH TABLE

"H"= $V_{CTL(H)}$, "L"= $V_{CTL(L)}$

CTL1	Path
H	P1-PC
L	P2-PC

Option: CTL2 is the mode switching port. Supplying "L" voltage, this device is operated the low current consumption mode.

NOTE: Please note that any information on this datasheet will be subject to change.

NJG1647HD3

■ ABSOLUTE MAXIMUM RATINGS

($T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	$V_{DD}=2.7\text{V}$, $CTL2=V_{CTL(H)}$	36	dBm
		$V_{DD}=2.7\text{V}$, $CTL2=V_{CTL(L)}$	32	
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	CTL1, CTL2 terminal	5.0	V
Power Dissipation	P_D	on PCB board	270	mW
Operating Temp.	T_{opr}		-40~+85	$^{\circ}\text{C}$
Storage Temp.	T_{stg}		-55~+150	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS 1

(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		2.5	2.7	3.6	V
Operating Current1	I_{DD1}	No RF input, $CTL2=V_{CTL(H)}$	-	300	500	μA
Operating Current2	I_{DD2}	No RF input, $CTL2=V_{CTL(L)}$	-	15	50	μA
Control Voltage (LOW)	$V_{CTL(L)}$	CTL1, CTL2 Terminal	0	-	0.4	V
Control Voltage (HIGH)	$V_{CTL(H)}$	CTL1, CTL2 Terminal	1.3	-	5.0	V
Control Current	I_{CTL}		-	5	10	μA

■ ELECTRICAL CHARACTERISTICS 2

(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss 1	LOSS1	$f=0.9\text{GHz}$, $P_{IN}=35\text{dBm}$	-	0.25	0.45	dB
Insertion Loss 2	LOSS2	$f=1.9\text{GHz}$, $P_{IN}=33\text{dBm}$	-	0.30	0.50	dB
Isolation 1	ISL1	$f=0.9\text{GHz}$, $P_{IN}=35\text{dBm}$	22	25	-	dB
Isolation 2	ISL2	$f=1.9\text{GHz}$, $P_{IN}=33\text{dBm}$	17	20	-	dB
Pin at 0.2dB Compression Point1	$P_{-0.2\text{dB}}(1)$	$f=1.9\text{GHz}$	34	-	-	dBm
2 nd harmonics1	$2f_0(1)$	$f=0.9\text{GHz}$, $P_{IN}=35\text{dBm}$	-	-75	-70	dBc
2 nd harmonics2	$2f_0(2)$	$f=1.9\text{GHz}$, $P_{IN}=33\text{dBm}$	-	-75	-70	dBc
3 rd harmonics1	$3f_0(1)$	$f=0.9\text{GHz}$, $P_{IN}=35\text{dBm}$	-	-75	-70	dBc
3 rd harmonics2	$3f_0(2)$	$f=1.9\text{GHz}$, $P_{IN}=33\text{dBm}$	-	-75	-70	dBc
Input 3 rd order intercept point1	IIP3(1)	$f=829+849\text{MHz}$, $P_{IN}=24\text{dBm}$ each tone *1	+65	+70	-	dBm
Input 3 rd order intercept point2	IIP3(2)	$f=1870+1910\text{MHz}$, $P_{IN}=24\text{dBm}$ each tone *1	+65	+70	-	dBm
VSWR	VSWR	on-state ports, $f=1.9\text{GHz}$	-	1.2	1.4	
Switching time	T_{SW}		-	1	5	μs

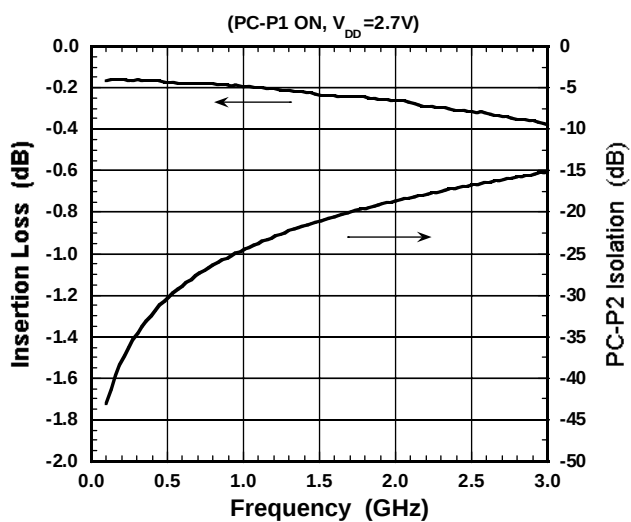
*1: IIP is defined by the following equation: $IIP3=(3 \times P_{out-IM3})/2+LOSS$

■ TERMINAL INFORMATION

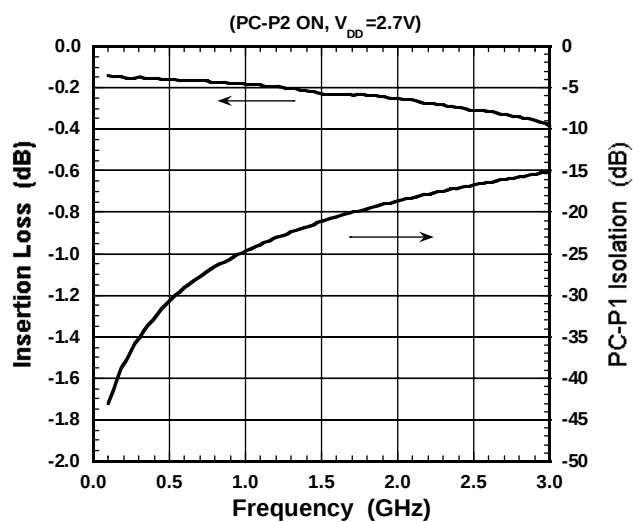
No.	SYMBOL	DESCRIPTION
1	PC	Common RF port. This PC port is connected to P1 or P2 by logical control voltage of CTL1. In order to block DC bias voltage of internal circuit, an external capacitor is required.
2	CTL2	Control port 2. This terminal is set to +1.3~5.0V of logical high level as usual, and set to +0.0~0.4V of logical low level for the low current consumption mode.
3	VDD	Supply voltage terminal (+2.5~3.6V). Please place an inductor close to this terminal, and a bypass capacitor between VDD and GND for avoiding RF characteristic degradation.
4	CTL1	Control port 1. This terminal is set to +1.3~5.0V of logical high level for ON state between PC and P1 ports, and set to +0.0~0.4V of logical low level for ON state between PC and P2 RF ports.
5	P1	This port is connected with PC port by control voltage of +1.3~5.0V($V_{CTL(H)}$) to 4th pin. An external capacitor is required to block the DC bias voltage of internal circuit.
6	P2	This port is connected to PC port by control voltage of +0.0~0.4V($V_{CTL(L)}$) to 4th pin. An external capacitor is required to block the DC bias voltage of internal circuit.
GND	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.

■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

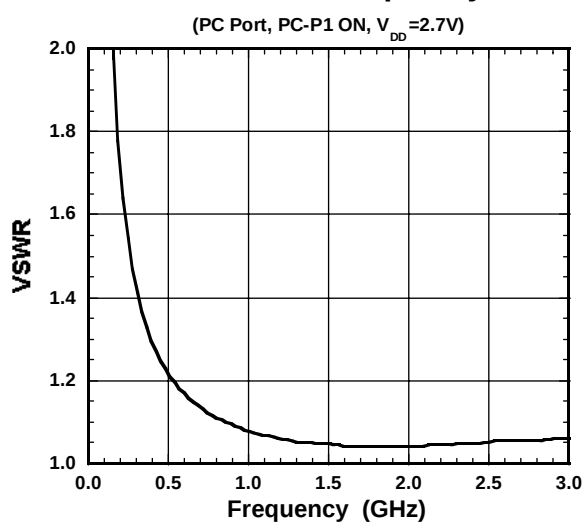
Loss, ISL vs Frequency



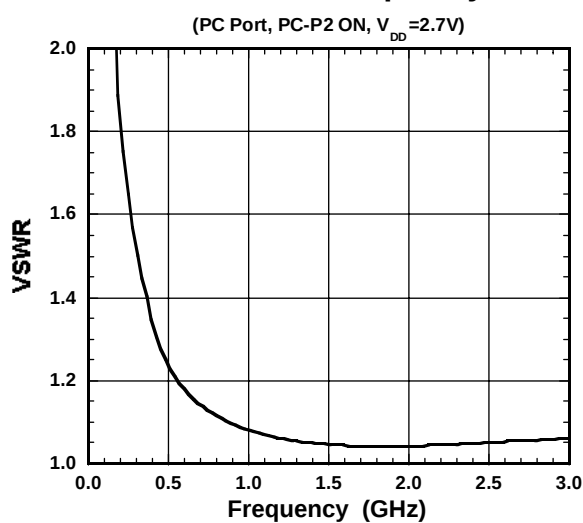
Loss, ISL vs Frequency



VSWR vs Frequency

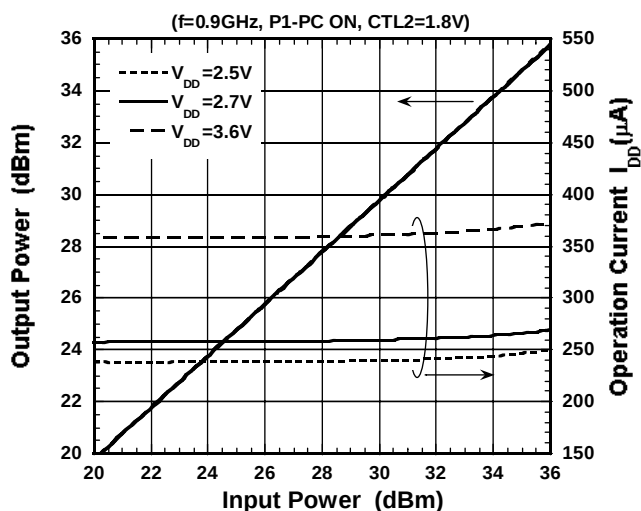


VSWR vs Frequency

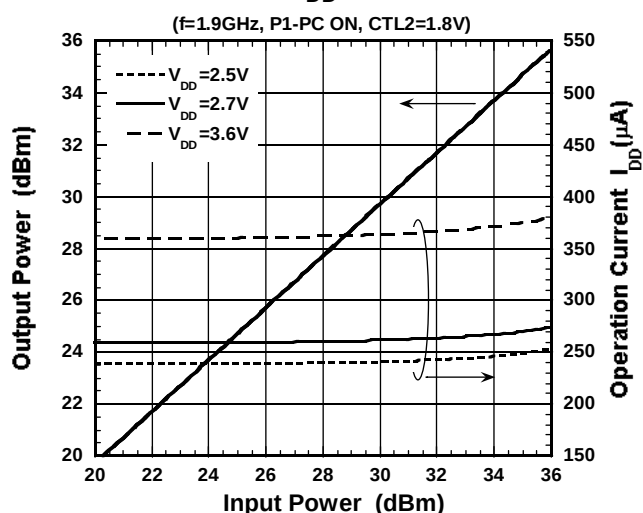


■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

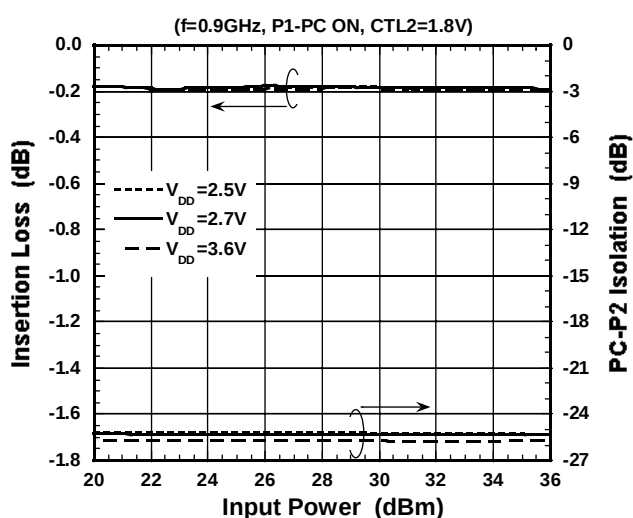
Output Power, I_{DD} vs Input Power



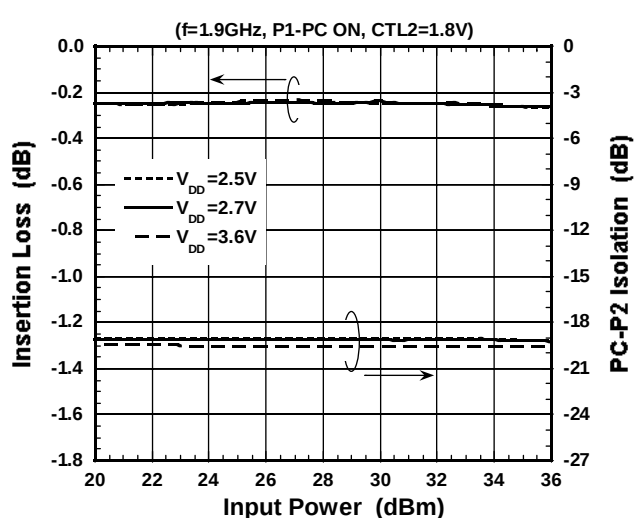
Output Power, I_{DD} vs Input Power



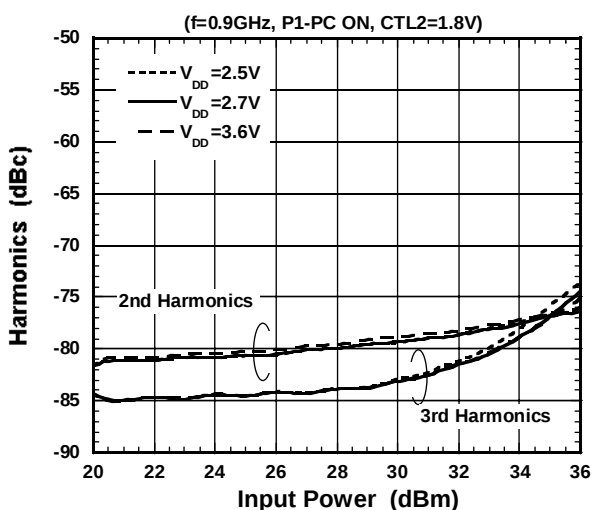
Loss, ISL vs Input Power



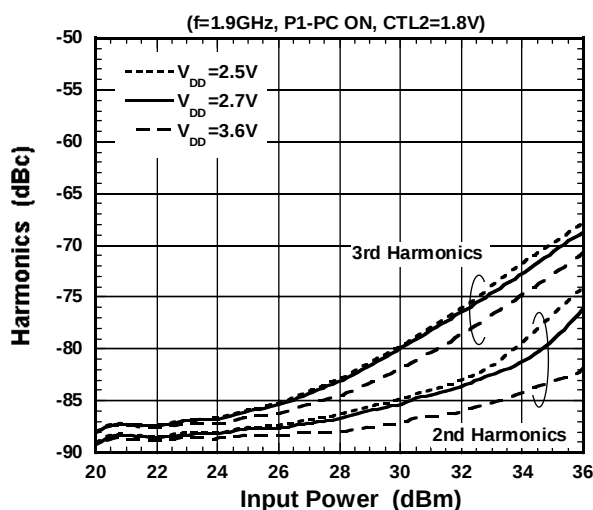
Loss, ISL vs Input Power



Harmonics vs Input Power



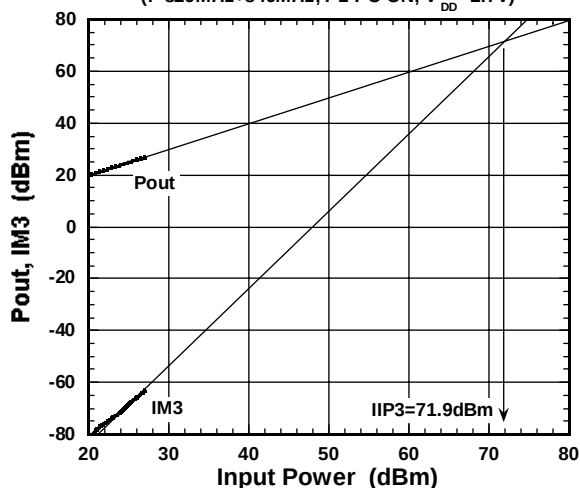
Harmonics vs Input Power



■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

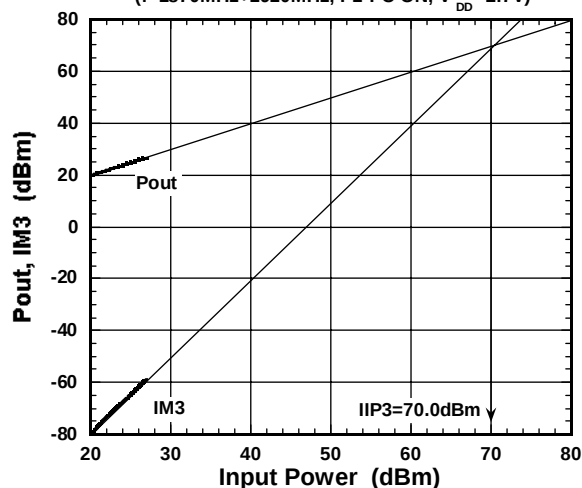
Output Power, IM3 vs Input Power

(f=829MHz+849MHz, P1-PC ON, $V_{DD}=2.7V$)



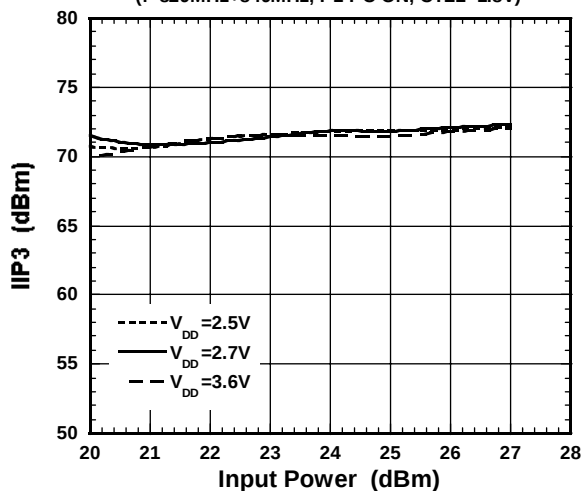
Output Power, IM3 vs Input Power

(f=1870MHz+1910MHz, P1-PC ON, $V_{DD}=2.7V$)



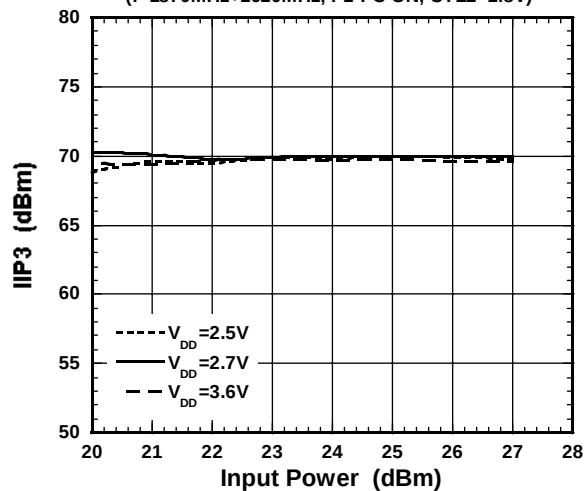
IIP3 vs Input Power

(f=829MHz+849MHz, P1-PC ON, CTL2=1.8V)



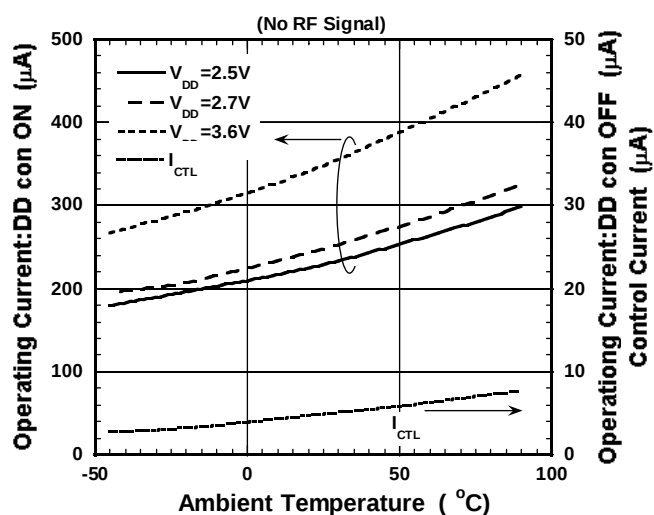
IIP3 vs Input Power

(f=1870MHz+1910MHz, P1-PC ON, CTL2=1.8V)

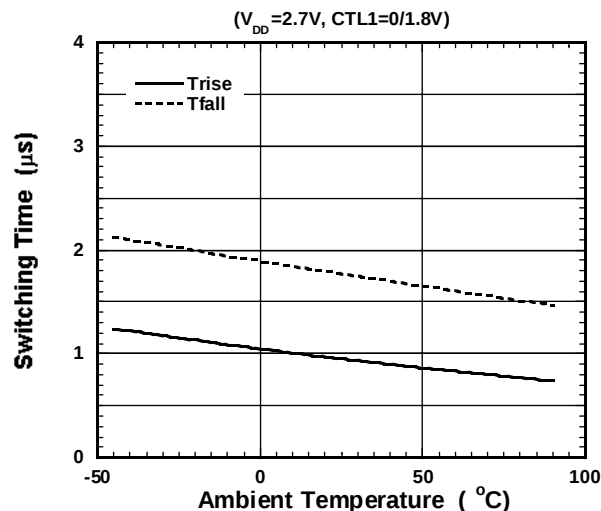


■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

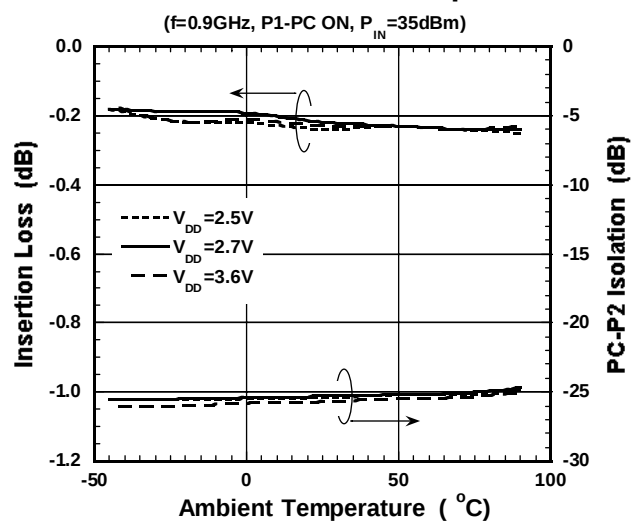
DC Current vs Ambient Temperature



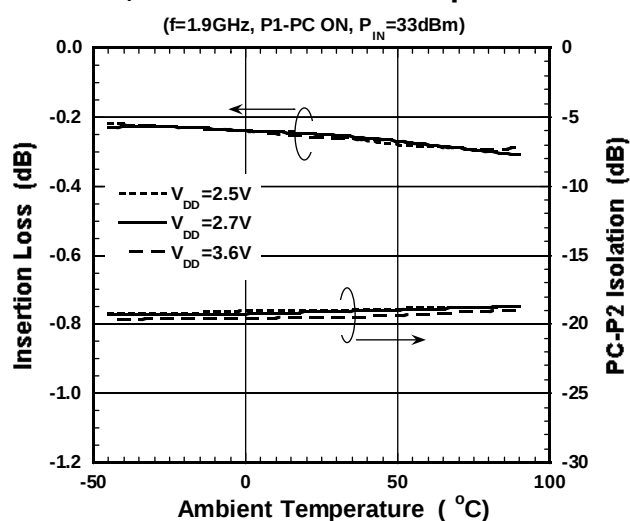
Switching Time vs Ambient Temperature



Loss, ISL vs Ambient Temperature

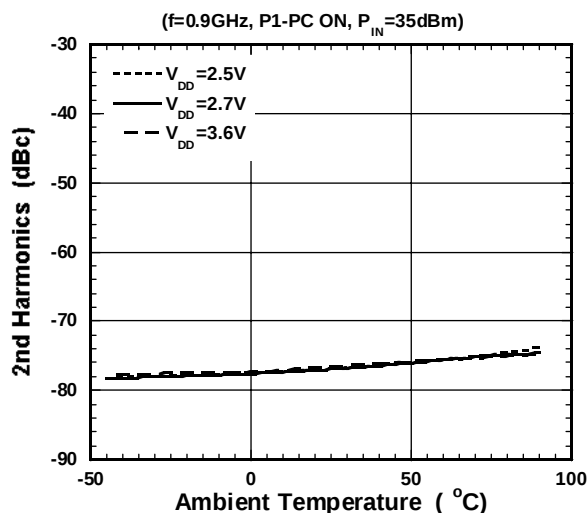


Loss, ISL vs Ambient Temperature

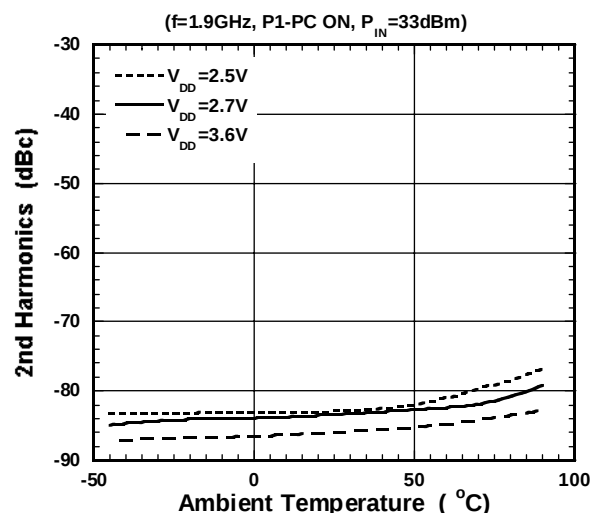


■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

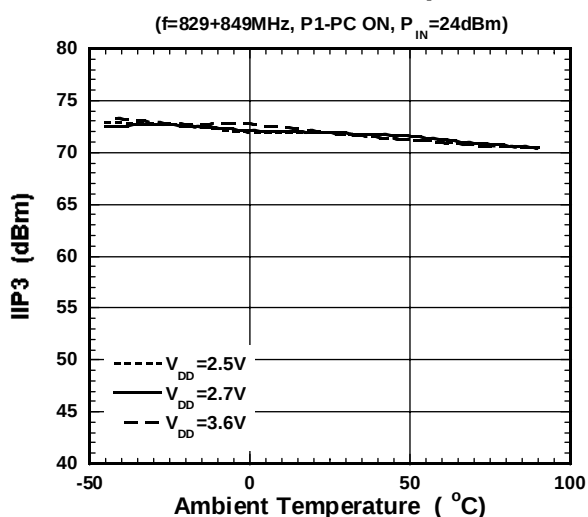
2nd Harmonics vs Ambient Temperature



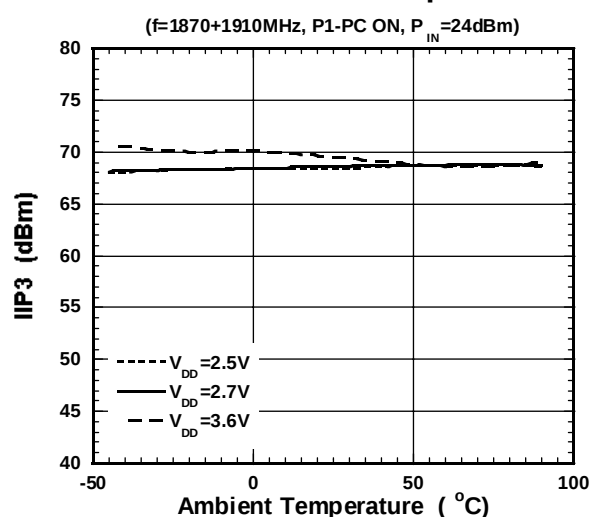
2nd Harmonics vs Ambient Temperature



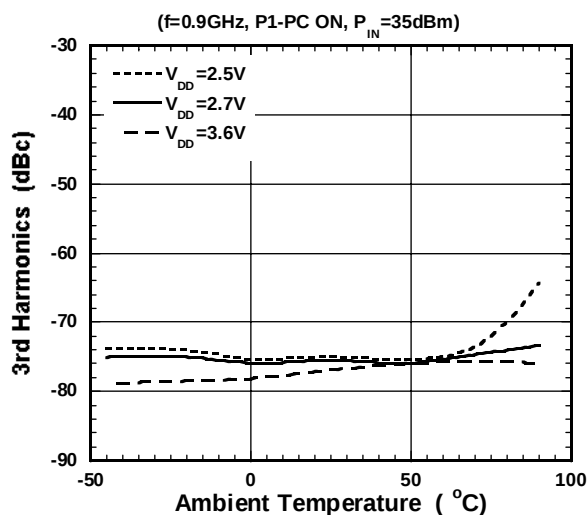
IIP3 vs Ambient Temperature



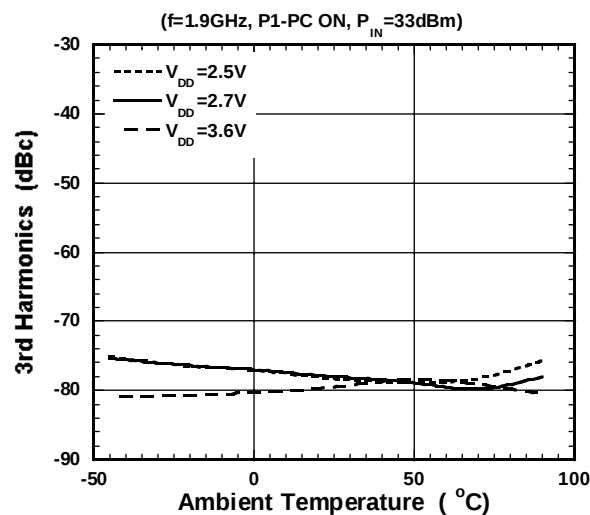
IIP3 vs Ambient Temperature



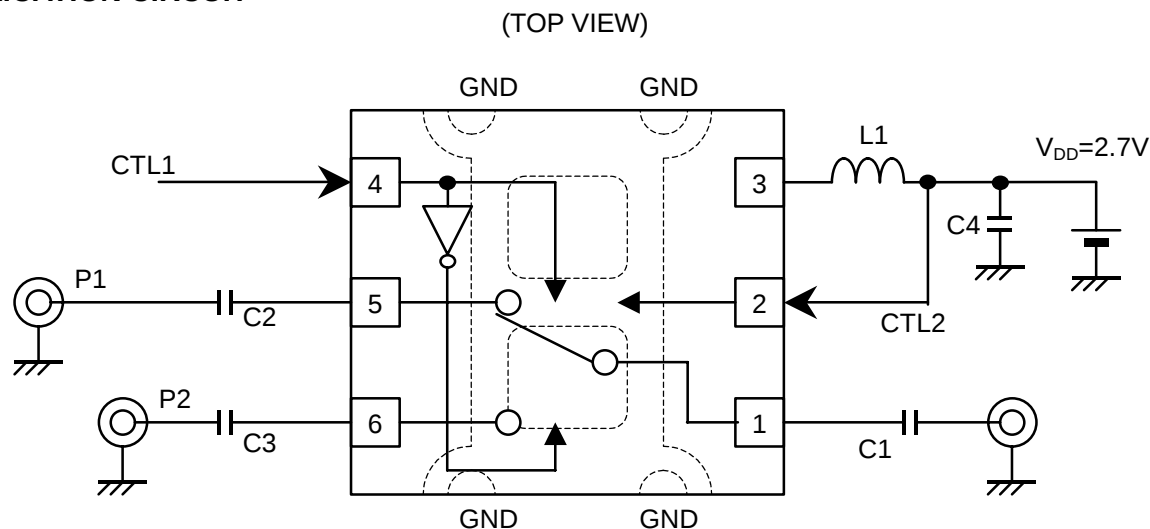
3rd Harmonics vs Ambient Temperature



3rd Harmonics vs Ambient Temperature



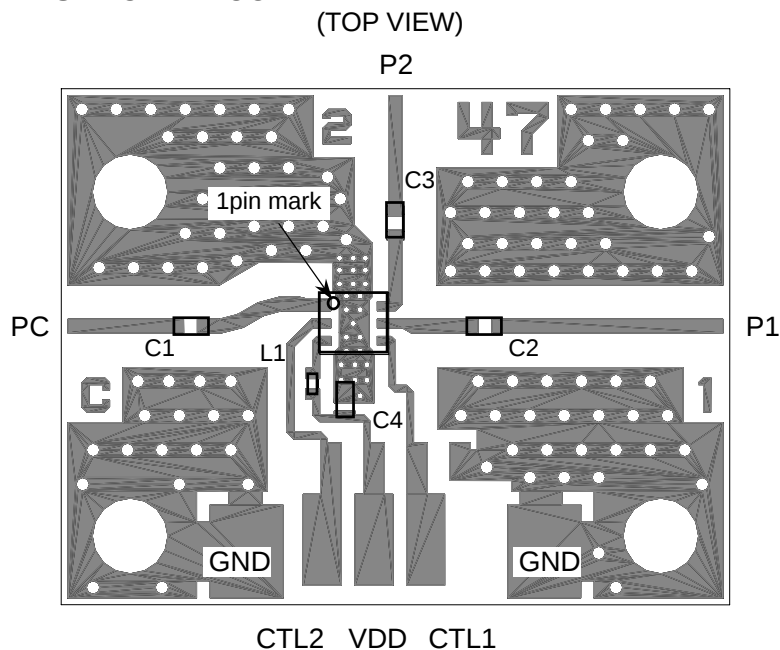
APPLICATION CIRCUIT



PARTS LIST

No.	Parameters	Note
C1~C3	56pF	Murata MFG (GRM15)
C4	1000pF	
L1	82nH	TDK (MLG0603)

TEST PCB LAYOUT



PCB SIZE=19.4x15.0mm
 PCB: FR-4, t=0.2mm
 CAPACITOR: size 1005
 INDUCTOR: size 0603
 Strip Line Width=0.4mm($Z_0=50\Omega$)

Losses of PCB

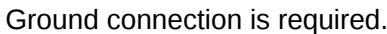
(Connector and DC blocking Capacitor losses are included)

Frequency (GHz)	Loss (dB)	
	PC-P1	PC-P2
0.9	0.23	0.21
1.9	0.33	0.30

PRECAUTIONS

- [1] The DC blocking capacitors have to be placed at RF terminal of PC, P1 and P2.
- [2] To control the influence on the RF performance, the terminal of VDD should be connected with ground through the inductor L1 and the bypass capacitor C4.
- [3] For good RF performance, the ground terminals must be placed possibly close to ground plane of substrate, and through holes for GND should be placed near by the pin connection.

■ PACKAGE OUTLINE (USB6-D3)



- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

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