

19-1780; Rev 0; 7/00

EVALUATION KIT
AVAILABLE

MAXIM

Complete Dual-Band Quadrature Transmitters

General Description

Features

The MAX2366 dual-band, triple-mode complete transmitter for cellular phones represents the most integrated and architecturally advanced solution to date for this application. The device takes a differential I/Q baseband input and mixes it up to IF through a quadrature modulator and IF variable-gain amplifier (VGA). The signal is then routed to an external bandpass filter and upconverted to RF through an SSB mixer and RF VGA. The signal is further amplified with an on-board PA driver. Dual IF synthesizers, dual RF synthesizers, a local oscillator (LO) buffer, and a 3-wire programmable bus complete the basic functional blocks of this IC. The MAX2367 supports single-band, single-mode (PCS) operation. The MAX2368 supports single-band cellular dual-mode operation.

- ◆ Dual-Band, Triple-Mode Operation
- ◆ +7dBm Output Power with -54dBc ACPR
- ◆ 100dB Power Control Range
- ◆ Supply Current Drops as Output Power Is Reduced
- ◆ Dual Synthesizer for IF and RF LO
- ◆ Dual On-Chip IF VCO
- ◆ QSPI/SPI/MICROWIRE-Compatible 3-Wire Bus
- ◆ Digitally Controlled Operational Modes
- ◆ +2.7V to +5.5V Operation
- ◆ Single Sideband Upconverter Eliminates SAW Filters

The MAX2366 enables architectural flexibility because its two IF voltage-controlled oscillators (VCOs), two IF ports, two RF LO input ports, and three PA driver output ports allow the use of a single receive IF frequency and split-band PCS filters for optimum out-of-band noise performance. The PA drivers allow up to three RF SAW filters to be eliminated. Select a mode of operation by loading data on the SPI™/QSPI™/MICROWIRE™-compatible 3-wire serial bus. Charge-pump current, sideband rejection, IF/RF gain balancing, standby, and shutdown are also controlled with the serial interface.

Ordering Information

The MAX2366/MAX2367/MAX2368 come in a 48-pin QFN-EP package and are specified for the extended (-40°C to +85°C) temperature range.

| PART | TEMP. RANGE | PIN-PACKAGE |
|------------|----------------|-------------|
| MAX2366EGM | -40°C to +85°C | 48 QFN-EP* |
| MAX2367EGM | -40°C to +85°C | 48 QFN-EP* |
| MAX2368EGM | -40°C to +85°C | 48 QFN-EP* |

*Exposed paddle

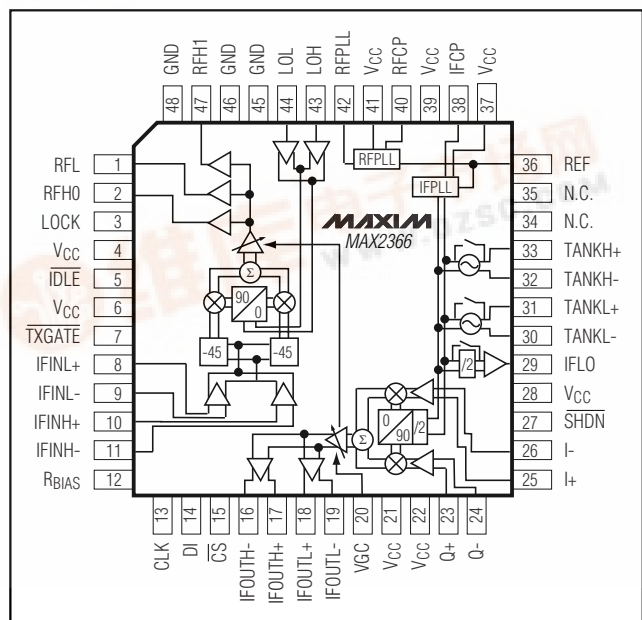
Applications

Functional Diagram

- Triple-Mode, Dual-Mode, or Single-Mode Mobile Phones
- Satellite Phones
- Wireless Data Links (WAN/LAN)
- Wireless Local Area Networks (LANs)
- High-Speed Data Modems
- High-Speed Digital Cordless Phones
- Wireless Local Loop (WLL)

Pin Configurations appear at end of data sheet.

Selector Guide appears at end of data sheet.



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MICROWIRE is a trademark of National Semiconductor Corp.

MAX2366/MAX2367/MAX2368

Complete Dual-Band Quadrature Transmitters

ABSOLUTE MAXIMUM RATINGS

| | |
|--|-----------------------------------|
| V _{CC} to GND | -0.3V to +3.6V |
| RFL, RFH0, RFH1 | +5.5V |
| DI, CLK, CS, VGC, SHDN, TXGATE, IDLE, LOCK | -0.3V to (V _{CC} + 0.3V) |
| AC Input Pins (IFINL, IFINH, Q, I, TANKL, TANKH, REF, RFPLL, LOL, LOH) | 1.0V peak |
| Digital Input Current (SHDN, TXGATE, IDLE, CLK, DI, CS) | ±10mA |

| | | |
|---|--|-----------------|
| Continuous Power Dissipation (T _A = +70°C) | 48-Pin QFN-EP (derate 27mW/°C above +70°C) | 2.5W |
| Operating Temperature Range | | -40°C to +85°C |
| Junction Temperature | | +150°C |
| Storage Temperature Range | | -65°C to +160°C |
| Lead Temperature (soldering, 10s) | | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX2366/7/8 test fixture: V_{CC} = V_{BATT} = +2.75V, SHDN = IDLE = TXGATE = +2.0V, VGC = +2.5V, R_{BIAS} = 16kΩ, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, and operating modes are defined in Table 6.)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--------------------------------------|---------------------------|--------------------------|-----------------------|-----|-----|-------|
| Operating Supply Voltage | | | 2.7 | | 3.0 | V |
| Operating Supply Current | (Note 1) | PCS mode | VGC = 0.5V | 92 | 118 | mA |
| | | | VGC = 2.0V | 97 | 123 | |
| | | | VGC = 2.5V | 132 | 161 | |
| | | Cellular digital mode | VGC = 0.5V | 91 | 110 | |
| | | | VGC = 2.0V | 95 | 122 | |
| | | | VGC = 2.5V | 132 | 164 | |
| | | FM mode | VGC = 0.5V | 85 | 110 | |
| | | | VGC = 2.0V | 89 | 114 | |
| | | | VGC = 2.5V | 114 | 142 | |
| | | Addition for IFLO buffer | | | 6.5 | |
| IDLE = 0.6V, cell idle | | | 15 | 20 | | |
| TXGATE = 0.6V | | | 26 | 34 | | |
| | | RFPLL off | 11 | | | |
| SHDN = 0.6V, sleep mode | | | 0.5 | 20 | μA | |
| Logic High | (Note 7) | | 2.0 | | | V |
| Logic Low | (Note 7) | | | | 0.6 | V |
| Logic Input Current | (Note 7) | | -5 | | +5 | μA |
| VGC Input Current | (Note 7) | | -10 | | +10 | μA |
| VGC Input Resistance During Shutdown | SHDN = 0.6V (Note 7) | | 225 | 280 | | kΩ |
| Lock Indicator High | 50kΩ pullup load (Note 7) | | V _{CC} - 0.4 | | | V |
| Lock Indicator Low | 50kΩ pullup load (Note 7) | | | | 0.4 | V |

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MAX2366/MAX2367/MAX2368

ELECTRICAL CHARACTERISTICS

(MAX2366/67/68 evaluation kit: 50Ω system, operating modes as defined in Table 6, input voltage at I and Q = 200mV_{RMS} differential, common mode = V_{CC}/2, 300kHz quadrature CW tones, RF and IF synthesizers locked with passive lead-lag second-order loop filter, REF = 200mVp-p at 19.68MHz, V_{CC} = SHDN = IDLE = CS = TXGATE = +2.75V, V_{BAT} = +2.75V, IF output load = 400Ω, LOH, LOL input power = -7dBm, f_{LOL} = 966MHz, f_{LOH} = 1750MHz, IFINH = 125mV_{RMS} at 130MHz, IS-95 CDMA modulation f_{RFH0} = f_{RFH1} = 1880MHz, f_{RFL} = 836MHz, T_A = +25°C, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---------------|--------------------|------------------------|-------|
| MODULATOR, QUADRATURE MODES (CDMA, PCS, FM_IQ) | | | | | |
| IF Frequency Range | IF_BAND = 0 | 120–235 | | | MHz |
| | IF_BAND = 1 | 120–300 | | | |
| I/Q Common-Mode Input Voltage | V _{CC} = 2.7V to 3.0V (Notes 2, 3, 7) | 1.35 | V _{CC} /2 | V _{CC} - 1.25 | V |
| IF Gain Control Range | VGC = 0.5V to 2.5V, IFG = 100 | 85 | | | dB |
| IF Output Power at IFOUTL and IFOUTH, CDMA Mode | VGC = 2.5V, IFG = 100, ACPR = -70dBc | -10 | | | dBm |
| Gain Variation Over Temperature | Relative to +25°C, T _A = -40°C to +85°C (Note 4) | -1 | | +1 | dB |
| Carrier Suppression | VGC = 2.5V, IFG = 100 | 30 | 49 | | dB |
| Sideband Suppression | VGC = 2.5V, IFG = 100 | 30 | 38 | | dB |
| MODULATOR, FM MODE | | | | | |
| IF Gain Control Range | VGC = 0.5V to 2.5V, IFG = 100 | 85 | | | dB |
| Output Power at IFOUTL | VGC = 2.5V, IFG = 111, I/Q modulation | -8.5 | | | dBm |
| | VGC = 2.5V, IFG = 111, direct VCO modulation | -5.5 | | | |
| UPCONVERTER AND PREDRIVER | | | | | |
| IF Frequency Range | IF_BAND = 0 | 120–200 | | | MHz |
| | IF_BAND = 1 | 180–300 | | | |
| RFL Frequency Range | RFL port | 800–1000 | | | MHz |
| RFH Frequency Range | RFH0 and RFH1 ports | 1700–2000 | | | MHz |
| LOL Frequency Range | | 800–1150 | | | MHz |
| LOH Frequency Range | | 1400–2300 | | | MHz |
| RFPLL Frequency Range | Cellular frequency operation | 1300 | | | MHz |
| | PCS frequency operation | 2300 | | | |
| Output Power, RFL Port | VGC = 2.5V | ACPR = -54dBc | 7 | | dBm |
| | | FM mode | 12 | | |
| Output Power, RFH1 Port | VGC = 2.6V, ACPR = -54dBc | 7.5 | | | dBm |
| Output Power, RFH0 Port | VGC = 2.6V, ACPR = -54dBc | 6.6 | | | dBm |
| Power Control Range | VGC = 0.5V to 2.5V | 30 | | | dB |
| Gain Variation Over Temperature | Relative to +25°C, T _A = -40°C to +85°C (Note 4) | | ±1 | ±2 | dB |
| LO Leakage | | -17 | | | dBm |
| Image Signal | | -29 | | | dBc |

Complete Dual-Band Quadrature Transmitters

ELECTRICAL CHARACTERISTICS (continued)

(MAX2366/67/68 evaluation kit: 50Ω system, operating modes as defined in Table 6, input voltage at I and Q = 200mV_{RMS} differential, common mode = $V_{CC}/2$, 300kHz quadrature CW tones, RF and IF synthesizers locked with passive lead-lag second-order loop filter, REF = 200mVp-p at 19.68MHz, V_{CC} = SHDN = IDLE = CS = TXGATE = +2.75V, V_{BAT} = +2.75V, IF output load = 400Ω, LOH, LOL input power = -7dBm, f_{LOL} = 966MHz, f_{LOH} = 1750MHz, IFINH = 125mV_{RMS} at 130MHz, IS-95 CDMA modulation f_{RFH0} = f_{RFH1} = 1880MHz, f_{RFL} = 836MHz, T_A = +25°C, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|---------|-----|--------|-------|
| IF_PLL | | | | | |
| Reference Frequency | | 5 | | 30 | MHz |
| Frequency Reference Signal Level | | 0.1 | | 0.6 | Vp-p |
| IF Main Divide Ratio | | 256 | | 16384 | |
| IF Reference Divide Ratio | | 2 | | 2048 | |
| VCO Operating Range | VCO = 0 | 240–470 | | | MHz |
| | VCO = 1 | 240–600 | | | |
| IF LO Output Power | BUF_EN = 1 | | -6 | | dBm |
| Charge-Pump Source/Sink Current | ICP = 00 (Note 7) | 115 | 175 | 230 | μA |
| | ICP = 01 (Note 7) | 145 | 235 | 315 | |
| | ICP = 10 (Note 7) | 235 | 350 | 470 | |
| | ICP = 11 (Note 7) | 300 | 465 | 625 | |
| TurboLock Boost Current | (Note 5, 7) | 265 | 450 | 615 | μA |
| Charge-Pump Source/Sink Matching | Locked, all values of ICP, over specified compliance range (Note 6) | | 5 | | % |
| Charge-Pump High-Z Leakage | Over specified compliance range (Note 6) | | | 10 | nA |
| RF_PLL | | | | | |
| RF Main Divide Ratio | | 4096 | | 262144 | |
| RF Reference Divide Ratio | | 2 | | 8192 | |
| Maximum Phase-Detector Comparison Frequency | | | 10 | | MHz |
| Charge-Pump Source/Sink Current | RCP = 00 (Note 7) | 100 | 165 | 225 | μA |
| | RCP = 01 (Note 7) | 135 | 230 | 310 | |
| | RCP = 10 (Note 7) | 210 | 340 | 460 | |
| | RCP = 11 (Note 7) | 270 | 450 | 630 | |
| TurboLock Boost Current | (Note 5, 6) | 245 | 435 | 630 | μA |
| Charge-Pump Source/Sink Matching | Locked, all values of RCP, over specified compliance range (Note 6, 7) | | 5 | | % |
| Charge-Pump High-Z Leakage | Over specified compliance range (Note 6) | | | 10 | nA |
| RFPLL Input Sensitivity | | 160 | | | mVp-p |

Note 1: See Table 6 for register settings.

Note 2: ACPR is met over the specified V_{CM} range.

Note 3: V_{CM} must be supplied by the I/Q baseband source with ±6μA capability.

Note 4: Guaranteed by design and characterization.

Note 5: When enabled, turboLock is active during acquisition and injects boost current in addition to the normal charge-pump current.

Note 6: Charge Pump Compliance range is 0.5V to V_{CC} - 0.5V.

Note 7: >25°C guaranteed by production test. <25°C guaranteed by design and characterization.

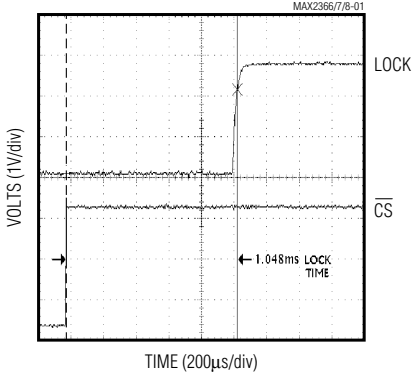
Complete Dual-Band Quadrature Transmitters

Typical Operating Characteristics

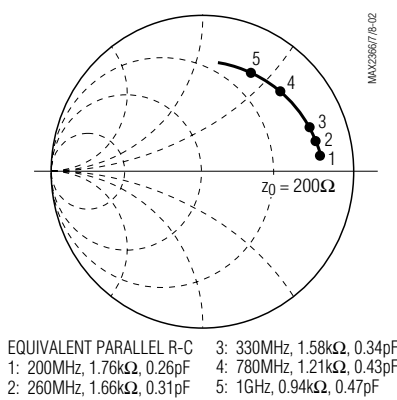
(MAX2366EVKIT, $V_{CC} = +2.75V$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX2366/MAX2367/MAX2368

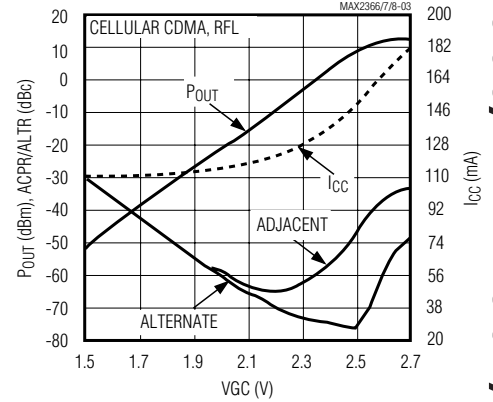
IF VCO VOLTAGE vs. TIME



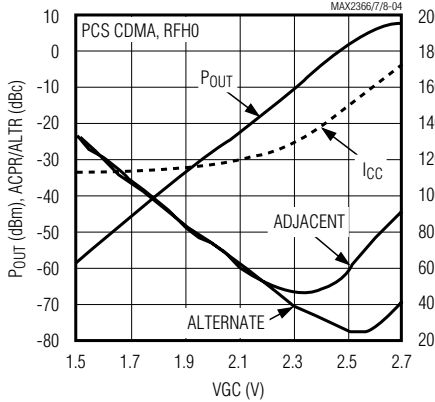
TANK 1/S11 vs. FREQUENCY



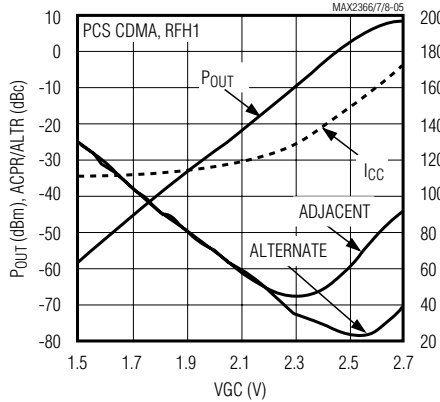
OUTPUT POWER, ACPR
 I_{CC} vs. VGC



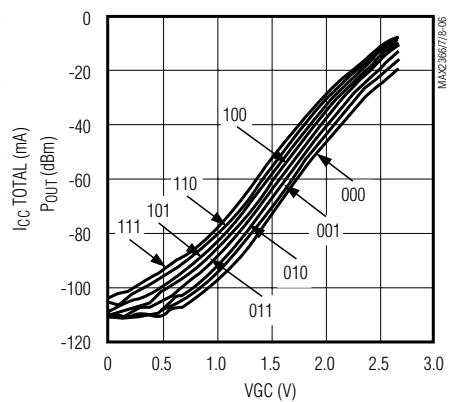
OUTPUT POWER, ACPR,
 I_{CC} vs. VGC



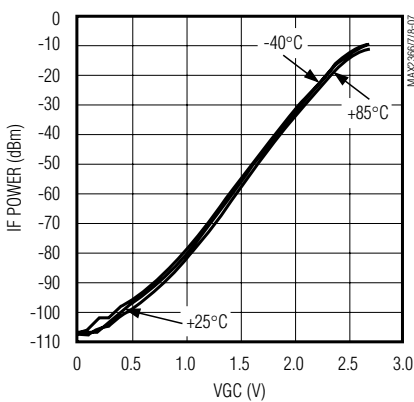
OUTPUT POWER, ACPR,
 I_{CC} TOTAL vs. VGC



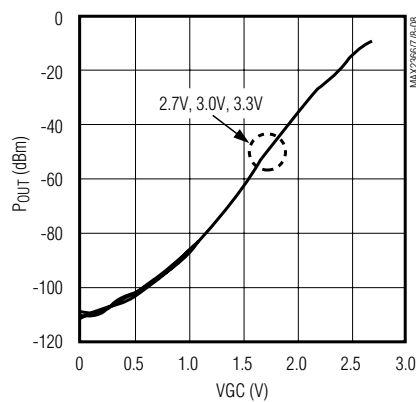
IF OUTPUT POWER
vs. VGC AND IF DAC SETTING



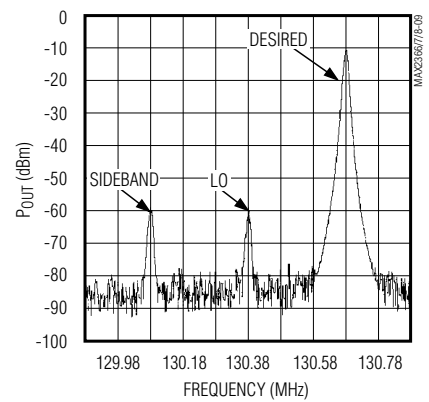
IF OUTPUT POWER vs. VGC



IF OUTPUT POWER vs. VGC



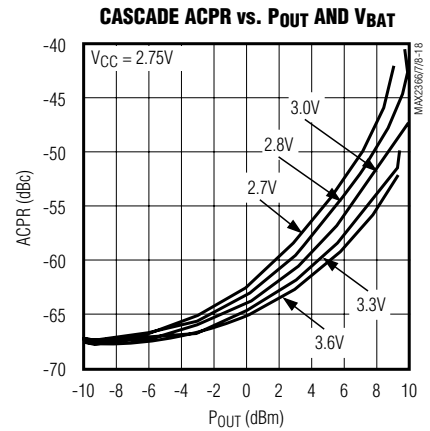
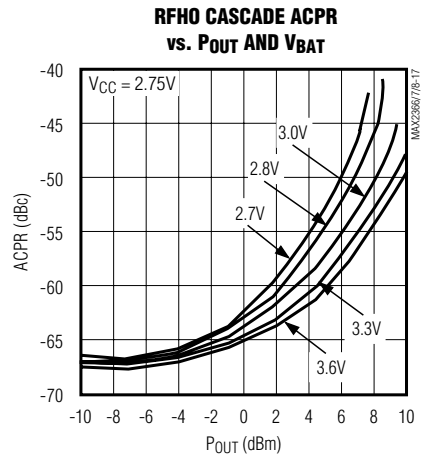
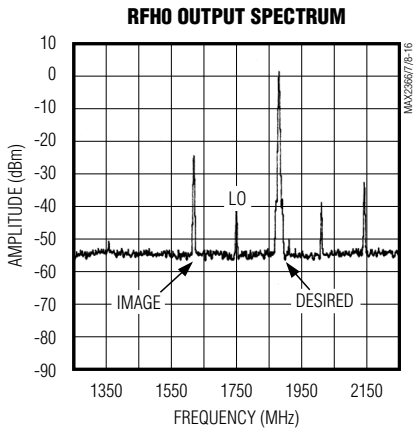
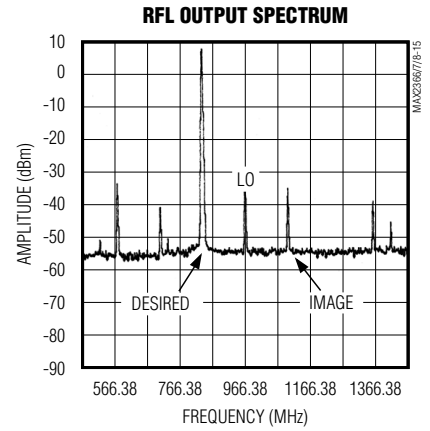
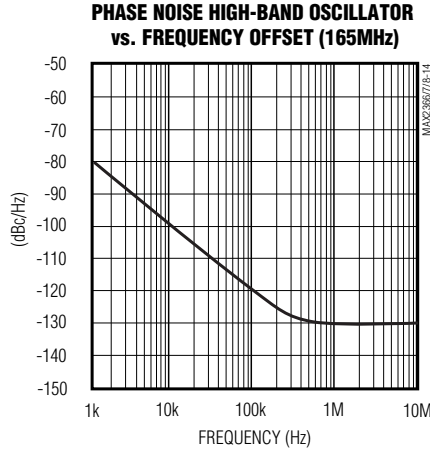
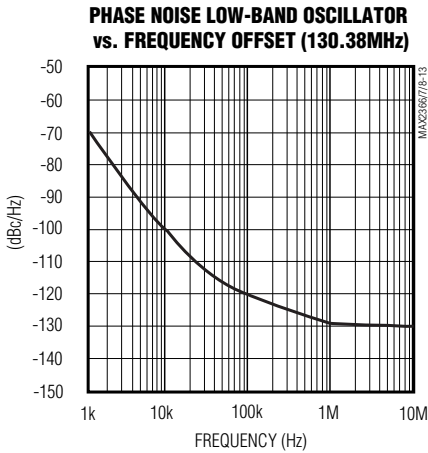
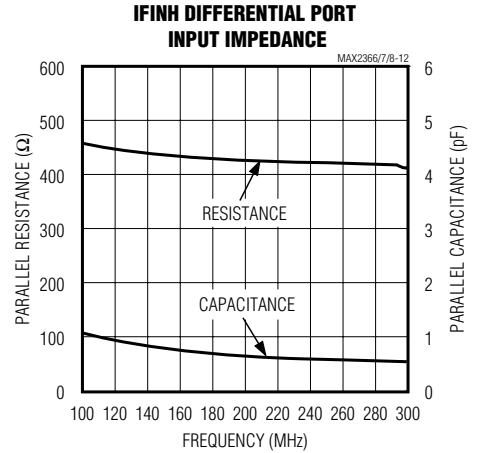
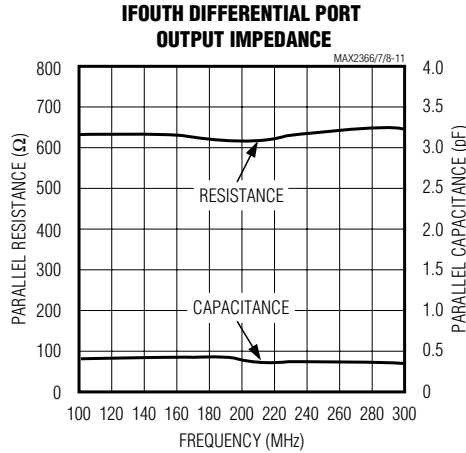
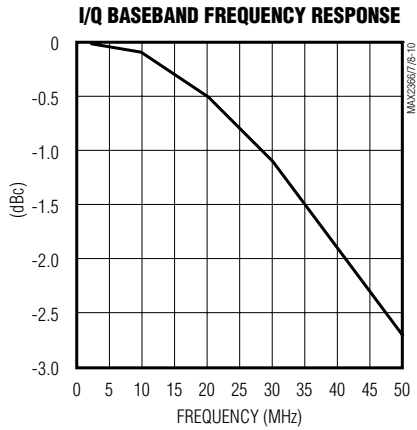
SIDEBAND SUPPRESSION AND
LO FEEDTHROUGH (IFOUTH)



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Typical Operating Characteristics (continued)

(MAX2366EVKIT, $V_{CC} = +2.75V$, $T_A = +25^{\circ}C$, unless otherwise noted.)

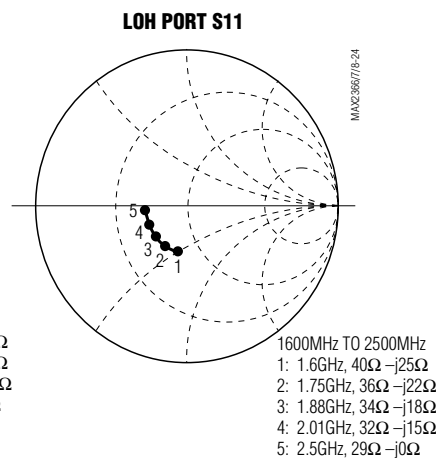
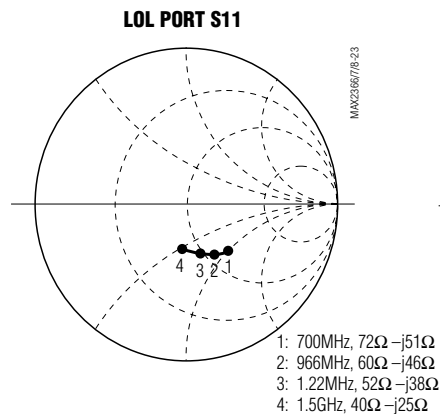
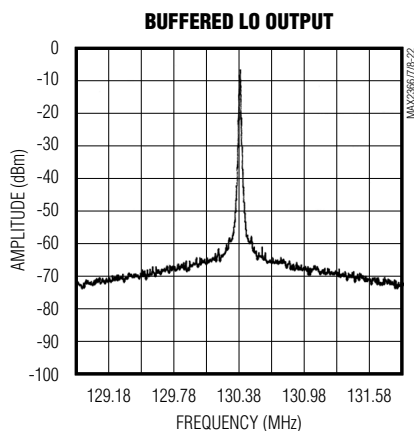
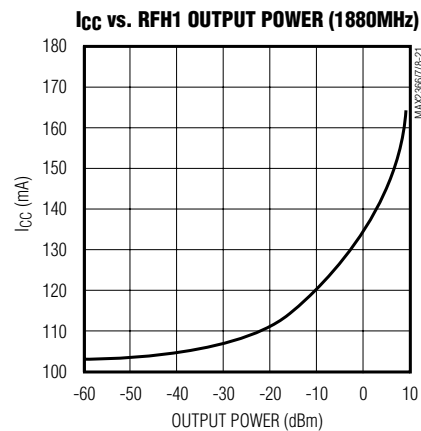
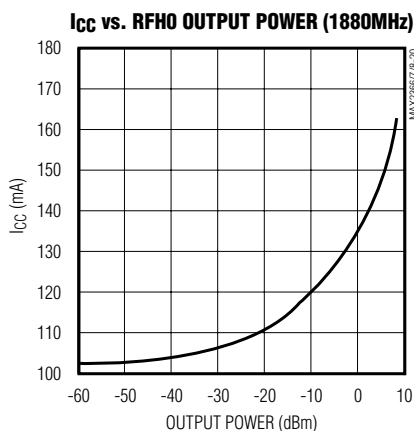
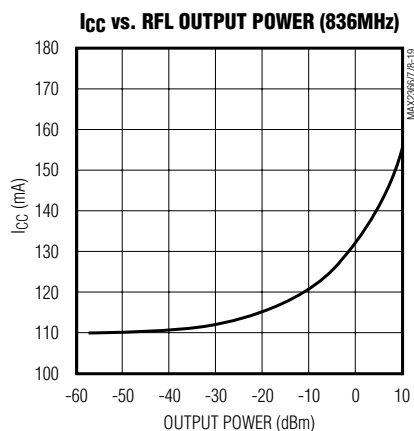


Complete Dual-Band Quadrature Transmitters

Typical Operating Characteristics (continued)

(MAX2366EVKIT, $V_{CC} = +2.75V$, $T_A = +25^{\circ}C$, unless otherwise noted.)

MAX2366/MAX2367/MAX2368



Complete Dual-Band Quadrature Transmitters

Pin Description

| PIN | | | NAME | FUNCTION |
|------------|-------------------------------------|----------------------------------|----------------------------|---|
| MAX2366 | MAX2367 | MAX2368 | | |
| 1 | — | 1 | RFL | Transmitter RF Output for Cellular Band (800MHz to 1000MHz)—for both FM and digital modes. This open-collector output requires a pullup inductor to the supply voltage, which may be part of the output matching network and may be connected directly to the battery. |
| — | 1, 8, 9, 18, 19, 30, 31, 34, 35, 44 | 2, 10, 11, 16, 17, 32–35, 43, 47 | N.C. | No Connection. Make no connection to these pins. |
| 2 | 2 | — | RFH0 | Transmitter RF Output for PCS Band (1700MHz to 2000MHz). This open-collector output requires a pullup inductor to the supply voltage. The pullup inductor may be part of the output matching network and may be connected directly to the battery. |
| 3 | 3 | 3 | LOCK | Open-Collector Output Indicating Lock Status of the IF and/or the RF PLLs. Requires a pullup resistor. Control using configuration register bit LD_MODE0, LD_MODE1. |
| 4 | 4 | 4 | V _{CC} | Power Supply |
| 5 | 5 | 5 | $\overline{\text{IDLE}}$ | Digital Input. A logic low on $\overline{\text{IDLE}}$ shuts down everything except the RF PLL and associated registers. A small R-C lowpass filter may be used to prevent digital noise. |
| 6 | 6 | 6 | V _{CC} | Supply Pin for the Upconverter Stage. V _{CC} must be bypassed to system ground as close to the pin as possible. The ground vias for the bypass capacitor should not be shared by any other branch. |
| 7 | 7 | 7 | $\overline{\text{TXGATE}}$ | Digital Input. A logic low on $\overline{\text{TXGATE}}$ shuts down everything except the RF PLL, IF PLL, IF VCO, and serial bus and registers. This mode is used for gated transmission. |
| 8, 9 | — | 8, 9 | IFINL+, IFINL- | Differential Inputs to the RF Upconverter. These pins are internally biased to +1.5V. The input impedance for these ports is nominally 400 Ω differential. The IF filter should be AC-coupled to these ports. Keep the differential lines as short as possible to minimize stray pickup and shunt capacitance. |
| 10, 11 | 10, 11 | — | IFINH+, IFINH- | Differential Inputs to the RF Upconverter. These pins are internally biased to +1.5V. The input impedance for these ports is nominally 400 Ω differential. The IF filter should be AC-coupled to these ports. Keep the differential lines as short as possible to minimize stray pickup and shunt capacitance. |
| 12 | 12 | 12 | RBIAS | Bias Resistor Pin. RBIAS is internally biased to a bandgap voltage of +1.18V. An external resistor or current source must be connected to this pin to set the bias current for the upconverters and PA driver stages. The nominal resistor value is 16k Ω . This value can be altered to optimize the linearity of the driver stage. |
| 13, 14, 15 | 13, 14, 15 | 13, 14, 15 | CLK, DI, CS | Input Pins from the 3-Wire Serial Bus (SPI/QSPI/MICROWIRE compatible). An R-C filter on each of these pins may be used to reduce noise. |

Complete Dual-Band Quadrature Transmitters

Pin Description (continued)

MAX2366/MAX2367/MAX2368

| PIN | | | NAME | FUNCTION |
|---------|---------|---------|--------------------------|--|
| MAX2366 | MAX2367 | MAX2368 | | |
| 16, 17 | 16, 17 | — | IFOUTH-, IFOUTH+ | Differential IF Outputs. These ports are active when the register bit IF_BAND is 1. They do not support FM mode. These pins must be inductively pulled up to V _{CC} . A differential IF bandpass filter is connected between this port and IFINH+ or IFINH-. The pullup inductors can be part of the filter structure. The differential output impedance of this port is nominally 600Ω. The transmission lines from these pins should be short to minimize the pickup of spurious signals and noise. |
| 18, 19 | — | 18, 19 | IFOUTL+, IFOUTL- | Differential IF Outputs. These ports are active when the register bit IF_BAND is 0. These pins must be inductively pulled up to V _{CC} . A differential IF bandpass filter is connected between this port and IFINL+ and IFINL-. The pullup inductors can be part of the filter structure. The differential output impedance of this port is nominally 600Ω. The transmission lines from these pins should be short to minimize the pickup of spurious signals and noise. |
| 20 | 20 | 20 | VGC | RF and IF Variable-Gain Control Analog Input. VGC floats to +1.5V. Apply +0.5V to +2.6V to control the gain of the RF and IF stages. An RC filter on this pin may be used to reduce DAC noise or PDM clock spurs from this line. |
| 21 | 21 | 21 | V _{CC} | Supply Pin for the IF VGA. Bypass with a capacitor as close to the pin as possible. The bypass capacitor must not share its ground vias with any other branches. |
| 22 | 22 | 22 | V _{CC} | Supply for the I/Q Modulator. Bypass with capacitor as close to the pin as possible. The bypass capacitor must not share its ground vias with any other branches. |
| 23, 24 | 23, 24 | 23, 24 | Q+, Q- | Differential Q-Channel Baseband Inputs to the Modulator. These pins go directly to the bases of a differential pair and require an external common-mode bias voltage. |
| 25, 26 | 25, 26 | 25, 26 | I+, I- | Differential I-Channel Baseband Inputs to the Modulator. These pins go directly to the bases of a differential pair and require an external common-mode bias voltage. |
| 27 | 27 | 27 | $\overline{\text{SHDN}}$ | Shutdown Input. A logic low on $\overline{\text{SHDN}}$ shuts down the entire IC. An R-C low-pass filter may be used to reduce digital noise. |
| 28 | 28 | 28 | V _{CC} | Supply Pin to the VCO Section. Bypass as close to the pin as possible. The bypass capacitor should not share its vias with any other branches. |
| 29 | 29 | 29 | IFLO | NBuffered LO Output. Control the output buffer using register bit BUF_EN and the divide ratio using the register bit BUF_DIV. |
| 30, 31 | — | 30, 31 | TANKL-, TANKL+ | Differential Tank Pins for the Low-Frequency IF VCO. These pins are internally biased to +1.6V. |

Complete Dual-Band Quadrature Transmitters

Pin Description (continued)

| PIN | | | NAME | FUNCTION |
|----------------|----------------|----------------|-------------------|--|
| MAX2366 | MAX2367 | MAX2368 | | |
| 32, 33 | 32, 33 | — | TANKH-, TANKH+ | Differential Tank Pins for the High-Frequency IF VCO. These pins are internally biased to +1.6V. |
| 34, 35 | — | — | N.C. | No Connection. Leave these pins floating. |
| 36 | 36 | 36 | REF | Reference Frequency Input. REF is internally biased to $V_{CC} - 0.7V$ and must be AC-coupled to the reference source. This is a high-impedance port ($25k\Omega \parallel 3pF$). |
| 37 | 37 | 37 | V_{CC} | Supply for the IF Charge Pump. This supply can differ from the system V_{CC} . Bypass as close to the pin as possible. The bypass capacitor must not share its vias with any other branches. |
| 38 | 38 | 38 | IFCP | High-Impedance Output of the IF Charge Pump. Connect to the tune input of the IF VCOs through the IF PLL loop filter. Keep the line from IFCP to the tune input as short as possible to prevent spurious pickup, and connect the loop filter as close to the tune input as possible. |
| 39 | 39 | 39 | V_{CC} | Supply Pin for Digital Circuitry. Bypass as close to the pin as possible. The bypass capacitor must not share its vias with any other branch. |
| 40 | 40 | 40 | RFCP | High-Impedance Output of the RF Charge Pump. Connect to the tune input of the RF VCOs through the RF PLL loop filter. Keep the line from this pin to the tune input as short as possible to prevent spurious pickup, and connect the loop filter as close to the tune input as possible. |
| 41 | 41 | 41 | V_{CC} | Supply for the RF Charge Pump. This supply can differ from the system V_{CC} . Bypass as close to the pin as possible. The bypass capacitor must not share its vias with any other branches. |
| 42 | 42 | 42 | RFPLL | RF PLL Input. AC-couple this port to the RF VCO. |
| 43 | 43 | — | LOH | High-band RF LO Input Port. AC-couple to this port. |
| 44 | — | 44 | LOL | Low-band RF LO Input Port. AC-couple to this port. |
| 45, 46, 48 | 45, 46, 48 | 45, 46, 48 | GND | Ground. Connect to PC board ground plane. |
| 47 | 47 | — | RFH1 | Transmitter RF Output for PCS Band (1700MHz to 2000MHz). This open-collector output requires a pullup inductor to the supply voltage. The pullup inductor may be part of the output matching network and may be connected directly to the battery. |
| Exposed paddle | Exposed paddle | Exposed paddle | GND | DC and AC GND Return for the IC. Connect to PC board ground plane using multiple vias. |

Complete Dual-Band Quadrature Transmitters

Detailed Description

The MAX2366 complete quadrature transmitter accepts differential I/Q baseband inputs with external common-mode bias. A modulator upconverts this to IF frequency in the 120MHz to 300MHz range. A gain control voltage pin (VGC) controls the gain of both the IF and RF VGAs simultaneously to achieve best noise and linearity performance. The IF signal is brought off-chip for filtering, then fed to a single sideband upconverter followed by the RF VGA and PA driver. The RF upconverter requires an external VCO for operation. The IF PLL, RF PLL, and operating mode can be programmed by an SPI/QSPI/MICROWIRE-compatible 3-wire interface.

The following sections describe each block in the MAX2366 *Functional Diagram*.

I/Q Modulator

Differential in-phase (I) and quadrature-phase (Q) input pins are designed to be DC-coupled and biased with the baseband output from a digital-to-analog converter (DAC). I and Q inputs need a DC bias of $V_{CC}/2$ and a current-drive capability of 6 μ A. Common-mode voltage will work within a 1.35V to ($V_{CC} - 1.25V$) range. Typically, I and Q will be driven differentially with a 200mVRMS baseband signal. Optionally, I and Q may be programmed for 100mVRMS operation with the IQ_LEVEL bit in the configuration register. The IF VCO output is fed into a divide-by-two/quadrature generator block to derive quadrature components to drive the IQ modulator. The output of the modulator is fed into the VGA.

IF VCOs

There are two VCOs to support high IF and low IF applications. The VCOs oscillate at twice the desired IF frequency. Oscillation frequency is determined by external tank components (see *Applications Information*). Typical phase-noise performance for the tank is as shown in Table 1. The high-band and low-band VCOs can be selected independently of the IF port being used.

Table 1. Typical VCO Phase Noise (IF = 130.38MHz)

| OFFSET (kHz) | PHASE NOISE (dBc) |
|--------------|-------------------|
| 1 | -80 |
| 12.5 | -105 |
| 30 | -111 |
| 120 | -121 |
| 900 | -128 |

IFLO Output Buffer

IFLO provides a buffered LO output when BUF_EN is 1. The IFLO output frequency is equal to the VCO frequency when BUF_DIV is 0, and half the VCO frequency when BUF_DIV is 1. The output power is -6dBm. This output is intended for applications where the receiver IF is the same frequency as the transmit IF.

IF/RF PLL

The IF/RF PLL uses a charge-pump output to drive a loop filter. The loop filter will typically be a passive second-order lead lag filter. Outside the filter's bandwidth, phase noise will be determined by the tank components. The two components that contribute most significantly to phase noise are the inductor and varactor. Use high-Q inductors and varactors to maximize equivalent parallel resistance. The IF_TURBO_CHARGE and the RF_TURBO_CHARGE bits in the CONFIG register can be set to 1 to enable turbo mode. Turbo mode provides maximum charge-pump current during frequency acquisition. Turbo mode is disabled after the second transition from phase lead to phase lag or from phase lag to phase lead. Turbo mode is also disabled after frequency acquisition is achieved. When turbo mode is disabled, charge-pump current will return to the programmed levels as set by ICP and RCP bits in the CONFIG register (Table 4).

IF VGA

The IF VGA allows varying an IF output level that is controlled by the VGs. The voltage range on VGC of +0.5V to +2.6V provides a gain-control range of 85dB. There are two differential IF output ports from the VGA. IFOUTL+/IFOUTL- are optimized for low IF operation (120MHz to 235MHz) for IFOUTH+/IFOUTH- support high IF operation (120MHz to 300MHz). IFOUTL ports support direct VCO FM modulation. The differential IF output port has an output impedance of 600 Ω when pulled up to V_{CC} through a choke.

Single Sideband Mixer

The RF transmit mixer uses a single sideband architecture to eliminate an off-chip RF filter. The single sideband mixer has IF input stages that correspond to IF output ports of the VGA. The mixer is followed by the RF VGA. The RF VGA is controlled by the same VGC pin as the IF VGA to provide optimum linearity and noise performance. The total power control range is >100dB.

PA Driver

The MAX2366 includes three power-amplifier (PA) drivers. Each is optimized for the desired operating frequency. RFL is optimized for cellular-band operation.

Complete Dual-Band Quadrature Transmitters

RFH0 and RFH1 are optimized for split-band PCS operation. The PA drivers have open-collector outputs and require pullup inductors. The pullup inductors can act as the shunt element in a shunt series match.

Programmable Registers

The MAX2366/MAX2367/MAX2368 include seven programmable registers consisting of four divide registers, a configuration register, an operational control register, and a test register. Each register consists of 24 bits. The 4 least significant bits (LSBs) are the register's address. The 20 most significant bits (MSBs) are used for register data. All registers contain some "don't care" bits. These can be either a zero or a 1 and do not affect operation (Figure 1). Data is shifted in MSB first, followed by the 4-bit address. When \overline{CS} is low, the clock is active and data is shifted with the rising edge of the clock. When \overline{CS} transitions to high, the shift register is latched into the register selected by the contents of the address bits. Power-up defaults for the seven registers are shown in Table 2. The dividers and control registers are programmed from the SPI/QSPI/MICROWIRE-compatible serial port.

The RFM register sets the main frequency divide ratio for the RF PLL. The RFR register sets the reference frequency divide ratio. The RF VCO frequency can be determined by the following:

$$\text{RF VCO frequency} = f_{\text{REF}} \times (\text{RFM} / \text{RFR})$$

IFM and IFR registers are similar:

$$\text{IF VCO frequency} = f_{\text{REF}} \times (\text{IFM} / \text{IFR})$$

where f_{REF} is the external reference frequency.

The operational control register (OPCTRL) controls the state of the MAX2366/MAX2367/MAX2368. See Table 3 for the function of each bit.

The configuration register (CONFIG) sets the configuration for the RF/IF PLL and the baseband I/Q input levels. See Table 4 for a description of each bit.

The test register is not needed for normal use.

Power Management

Bias control is distributed among several functional sections and can be controlled to accommodate many different power-down modes as shown in Table 5.

The shutdown control bit is of particular interest since it differs from the \overline{SHDN} pin. When the shutdown control bit is active ($\text{SHDN_BIT} = 0$), the serial interface is left active so that the part can be turned on with the serial bus while all other functions remain shut off. In contrast, when the \overline{SHDN} pin is low it shuts down everything. In either case, PLL programming and register information is lost. To retain the register information, use standby mode ($\text{STBY} = 0$).

Signal Flow Control

Table 6 shows an example of key registers for triple-mode operation, assuming half-band PCS and IF frequencies of 130MHz/165MHz.

Applications Information

The MAX2366 is designed for use in dual-band, triple-mode systems. It is recommended for triple-mode handsets (Figure 2). The MAX2367 is designed for use in CDMA PCS handsets or WLL single-mode 2.4GHz ISM systems (Figure 3). The MAX2368 is designed for use in dual-mode cellular systems (Figure 4).

3-Wire Interface

Figure 5 shows the 3-wire interface timing diagram. The 3-wire bus is SPI/QSPI/MICROWIRE compatible.

Table 2. Register Power-Up Default States

| REGISTER | DEFAULT | ADDRESS | FUNCTION |
|----------|------------|-------------------|---------------------------------|
| RFM | 172087 dec | 0000 _b | RF M divider count |
| RFR | 1968 dec | 0001 _b | RF R divider count |
| IFM | 6519 dec | 0010 _b | IF M divider count |
| IFR | 0492 dec | 0011 _b | IF R divider count |
| OPCTRL | 892F hex | 0100 _b | Operational control settings |
| CONFIG | D03F hex | 0101 _b | Configuration and setup control |
| TEST | 0000 hex | 0111 _b | Test-mode control |

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| | | 24-BIT REGISTER | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------|--|-------------------------|-----|-----|-----|-----|-----|-----|-----|---------|-----|----|---------|----|---------|---------|----|---------|----|---------|----|----------------|----|----|----|
| | | DATA 20 BITS | | | | | | | | | | | | | | | | | | | | ADDRESS 4 BITS | | | |
| | | B19 | B18 | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | A3 | A2 | A1 | A0 |
| RFM DIVIDE REGISTER | | RFM DIVIDE RATIO (18) | | | | | | | | | | | | | | | | | | ADDRESS | | | | | |
| | | X | X | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 |
| RFR DIVIDE REGISTER | | RFR DIVIDE RATIO (13) | | | | | | | | | | | | | ADDRESS | | | | | | | | | | |
| | | X | X | X | X | X | X | X | | | | | | | | | | | | | | 0 | 0 | 0 | 1 |
| IFM DIVIDE REGISTER | | IFM DIVIDE RATIO (14) | | | | | | | | | | | | | | ADDRESS | | | | | | | | | |
| | | X | X | X | X | X | X | | | | | | | | | | | | | | | 0 | 0 | 1 | 0 |
| IFR DIVIDE REGISTER | | IFR DIVIDE RATIO (11) | | | | | | | | | | | ADDRESS | | | | | | | | | | | | |
| | | X | X | X | X | X | X | X | X | | | | | | | | | | | | | 0 | 0 | 1 | 1 |
| CONTROL REGISTER | | CONTROL BITS (16) | | | | | | | | | | | | | | | | ADDRESS | | | | | | | |
| | | X | X | X | X | | | | | | | | | | | | | | | | | 0 | 1 | 0 | 0 |
| CONFIGURATION REGISTER | | CONFIGURATION BITS (16) | | | | | | | | | | | | | | | | ADDRESS | | | | | | | |
| | | X | X | X | X | | | | | | | | | | | | | | | | | 0 | 1 | 0 | 1 |
| TEST REGISTER | | TEST BITS (8) | | | | | | | | ADDRESS | | | | | | | | | | | | | | | |
| | | X | X | X | X | X | X | X | X | | | | | | | | | | | | | 0 | 1 | 1 | 1 |

X = DON'T CARE

Figure 1. Register Configuration

Electromagnetic Compliance Considerations

Two major concepts should be employed to produce a noise-free and EMC-compliant transmitter: minimize circular current-loop area to reduce H-field radiation and minimize voltage drops to reduce E-field radiation. To minimize the circular current-loop area, bypass as close to the part as possible and use the distributed capacitance of a ground plane. To minimize voltage drops, make VCC traces short and wide, and make RF traces short.

The “don't care” bits in the registers should be zero in order to minimize electromagnetic radiation due to unnecessary bit banging. RC filtering can also be used to slow the clock edges on the 3-wire interface, reducing high-frequency spectral content. RC filtering also

provides for transient protection against IEC802 testing by shunting high frequencies to ground, while the series resistance attenuates the transients for error-free operation. The same applies to the override pins (SHDN, TXGATE, IDLE).

High-frequency bypass capacitors are required close to the pins with a dedicated via to ground. The 48-pin QFN-EP package provides minimal inductance ground by using an exposed paddle under the part. Provide at least five low-inductance vias under the paddle to ground to minimize ground inductance. Use a solid ground plane wherever possible. Any cutout in the ground plane may act as slot radiator and reduce its shield effectiveness.

Keep the RF LO traces as short as possible to reduce LO radiation and susceptibility to interference.

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Table 3. Operation Control Register (OPCTRL)

| BIT NAME | POWER-UP STATE | BIT LOCATION (0 = LSB) | FUNCTION |
|-----------|----------------|------------------------|--|
| LO_SEL | 1 | 15 | 1 selects LOL input port; 0 selects LOH port. |
| RCP_MAX | 0 | 14 | 1 keeps RF turbo-mode current active even when frequency acquisition is achieved. This bit has no effect when RF_TURBO_CHARGE = 0. This mode is used when high operating RF charge-pump current is needed. |
| ICP_MAX | 0 | 13 | 1 keeps IF turbo-mode current active even when frequency acquisition is achieved. This bit has no effect when IF_TURBO_CHARGE = 0. This mode is used when high operating IF charge-pump current is needed. |
| MODE | 01 | 12, 11 | Sets operating mode according to the following: 00 = FM mode 01 = Cellular digital mode; RFL is selected 10 = PCSHIGH mode; RFH1 is selected 11 = PCSLOW mode; RFH0 is selected |
| IF_BAND | 0 | 10 | 1 selects IFINH and IFOUTH; 0 selects IFINL and IFOUTL. For FM mode (MODE = 00), set IF_BAND to 0. |
| VCO | 0 | 9 | 1 selects high-band IF VCO; 0 selects low-band IF VCO. |
| IFG | 100 | 8, 7, 6 | 3-bit IF gain control. Alters IF gain by approximately 2dB per LSB (0 to 14dB). Provides a means for adjusting balance between RF and IF gain for optimized linearity. |
| SIDE_BAND | 1 | 5 | When this register is 1, the upper sideband is selected (LO below RF). When this register is 0, the lower sideband is selected (LO above RF). |
| BUF_EN | 0 | 4 | 0 turns IFLO buffer off; 1 turns IFLO buffer on. |
| MOD_TYPE | 1 | 3 | 0 selects direct VCO modulation. (IF VCO is externally modulated and the I/Q modulator is bypassed); 1 selects quadrature modulation. |
| STBY | 1 | 2 | 0 shuts down everything except registers and serial interface. |
| TXSTBY | 1 | 1 | 0 shuts down modulator and upconverter, leaving PLLs locked and registers active. This is the programmable equivalent to the TXGATE pin. |
| SHDN_BIT | 1 | 0 | 0 shuts down everything except serial interface, and also resets all registers to power-up state. |

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Table 4. Configuration Register (CONFIG)

| BIT NAME | POWER-UP STATE | BIT LOCATION (0 = LSB) | FUNCTION |
|-----------------|----------------|------------------------|---|
| IF_PLL_SHDN | 1 | 15 | 0 shuts down the IF PLL. This mode is used with an external IF VCO and IF PLL. |
| RF_PLL_SHDN | 1 | 14 | 0 shuts down the RF PLL. This mode is used with an external RF PLL. |
| RESERVED | 0 | 13 | Must be set to 0 for normal operation. |
| IQ_LEVEL | 1 | 12 | 1 selects 200mV _{RMS} input mode; 0 selects 100mV _{RMS} input mode. |
| BUF_DIV | 0 | 11 | 1 selects ÷2 on IFLO port; 0 bypasses the divider. |
| VCO_BYPASS | 0 | 10 | 1 bypasses IF VCO and enables a buffered input for external VCO use. |
| ICP | 00 | 9, 8 | A 2-bit register sets the IF charge-pump current as follows: 00 = 175µA 01 = 235µA 10 = 350µA 11 = 465µA |
| RCP | 00 | 7, 6 | A 2-bit register sets the RF charge-pump current as follows: 00 = 165µA 01 = 230µA 10 = 340µA 11 = 450µA |
| IF_PD_POL | 1 | 5 | IF phase-detector polarity; 1 selects positive polarity (increasing tuning voltage on the VCO produces increasing frequency); 0 selects negative polarity (increasing tuning voltage on the VCO produces decreasing frequency). |
| RF_PD_POL | 1 | 4 | RF phase-detector polarity; 1 selects positive polarity (increasing tuning voltage on the VCO produces increasing frequency); 0 selects negative polarity (increasing voltage on the VCO produces decreasing frequency). |
| IF_TURBO_CHARGE | 1 | 3 | 1 activates turbocharge feature, providing an additional 450µA of IF charge-pump current during frequency acquisition. |
| RF_TURBO_CHARGE | 1 | 2 | 1 activates turbocharge feature, providing an additional 435µA of RF charge-pump current during frequency acquisition. |
| LD_MODE | 11 | 1, 0 | Determines output mode for LOCK detector pin as follows: 00 = test mode, LD_MODE cannot be 00 for normal operation 01 = IF PLL lock detector 10 = RF PLL lock detector 11 = logical AND of IF PLL and RF PLL lock detectors |

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Table 5. Power-Down Modes

| POWER-DOWN MODE | COMMENTS | UPCONVERTER | MODULATOR | SERIAL BUS | RF_PLL | RF PLL REGS | OPCTRL REG | IF_LO_BUFF | IF_VCO | IF_PLL | IF PLL REGS | CONFIG REG |
|--------------------------------|--|-------------|-----------|------------|--------|-------------|------------|------------|--------|--------|-------------|------------|
| $\overline{\text{SHDN}}$ Pin | Ultra-low shutdown current | X | X | X | X | X | X | X | X | X | X | X |
| $\overline{\text{IDLE}}$ Pin | $\overline{\text{IDLE}}$ is low in RX mode | X | X | | | | | X | X | X | X | |
| $\overline{\text{TXGATE}}$ Pin | For punctured TX mode | X | X | | | | | | | | | |
| RF PLL SHDN | For external RF PLL use | | | | X | X | | | | | | |
| IF PLL SHDN | For external IF PLL use | | | | | | | | | X | X | |
| TX STBY | TX is OFF, but IF and RF LOs stay locked | X | X | | | | | | | | | |
| REG STBY | Shuts down, but preserves registers | X | X | | X | | | X | X | X | | |
| REG SHDN | Serial bus is still active | X | X | | X | X | X | X | X | X | X | X |

X = Off

Table 6. Register and Control Pin States for Key Operating Modes

| MODE | DESCRIPTION | OPCTRL REGISTER | | | | | | | | CONFIG REGISTER | | CONTROL PINS | | |
|------------------|--------------------------------------|-----------------|------|---------|-----|----------|------|--------|----------|-----------------|-------------|--------------------------|----------------------------|--------------------------|
| | | LO_SEL | MODE | IF_BAND | VCO | MOD_TYPE | STBY | TXSTBY | SHDN_BIT | IF_PLL_SHDN | RF_PLL_SHDN | $\overline{\text{IDLE}}$ | $\overline{\text{TXGATE}}$ | $\overline{\text{SHDN}}$ |
| PCS High | PCS upper half-band, RFH1 selected | 0 | 10 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | H | H | H |
| PCS Low | PCS lower half-band, RFH0 selected | 0 | 11 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | H | H | H |
| Cellular Digital | RFL selected | 1 | 01 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | H | H | H |
| FM | Direct VCO modulation, RFL selected | 1 | 00 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | H | H | H |
| PCS Idle | Listen for pages RX ON, TX OFF | 0 | 1X | X | X | X | 1 | X | 1 | X | 1 | L | H | H |
| Cellular Idle | Listen for pages RX ON, TX OFF | 1 | 0X | X | X | X | 1 | X | 1 | X | 1 | L | H | H |
| PCS TXGATE | Gated transmission, PCS | 0 | 1X | 1 | 1 | 1 | 1 | X | 1 | 1 | 1 | H | L | H |
| Cellular TXGATE | Gated transmission, cellular digital | 1 | 01 | 0 | 0 | 1 | 1 | X | 1 | 1 | 1 | H | L | H |
| Sleep | Everything off | X | XX | X | X | X | X | X | X | X | X | X | X | L |

X = Don't care

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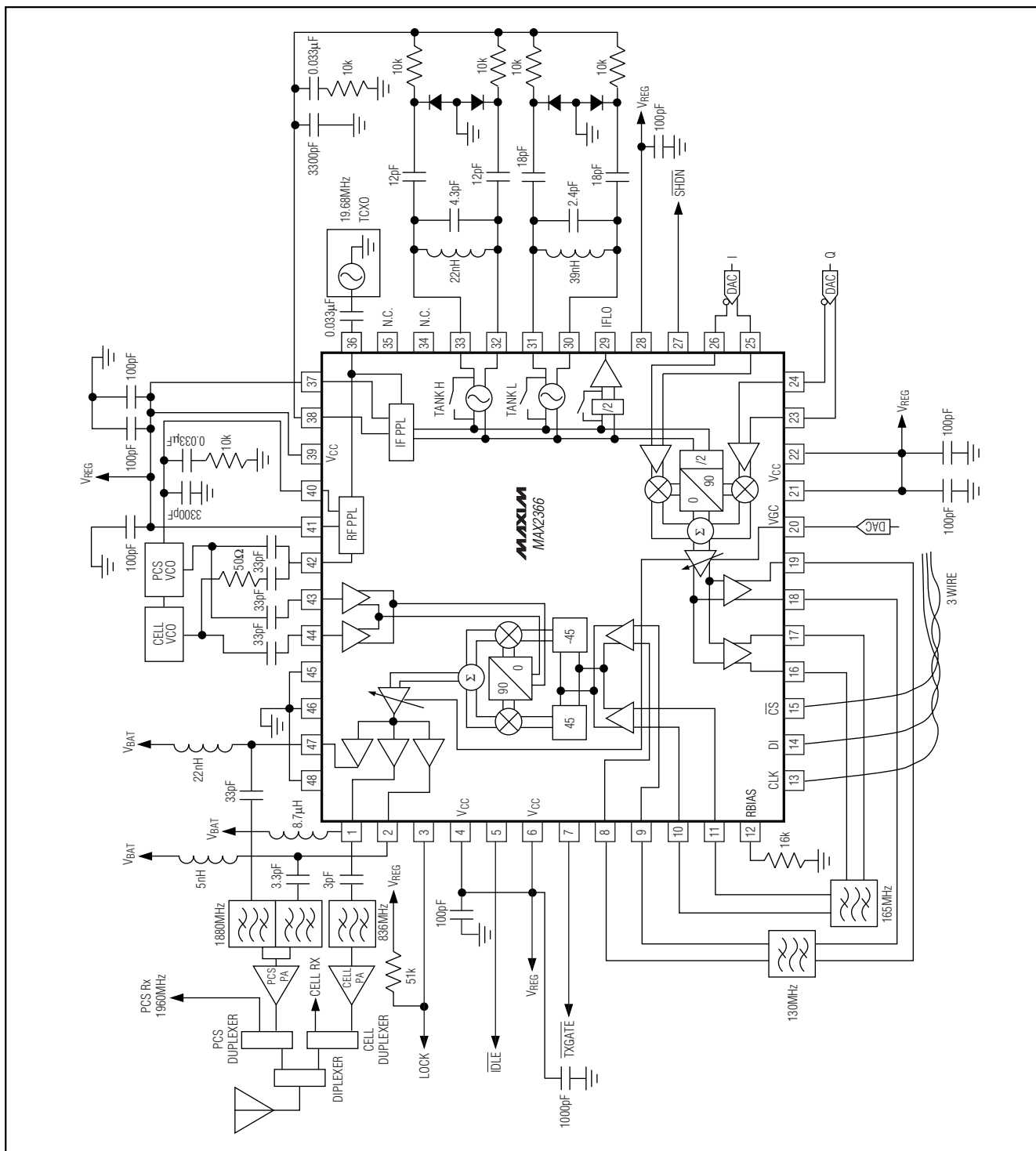


Figure 2. MAX2366 Typical Application Circuit

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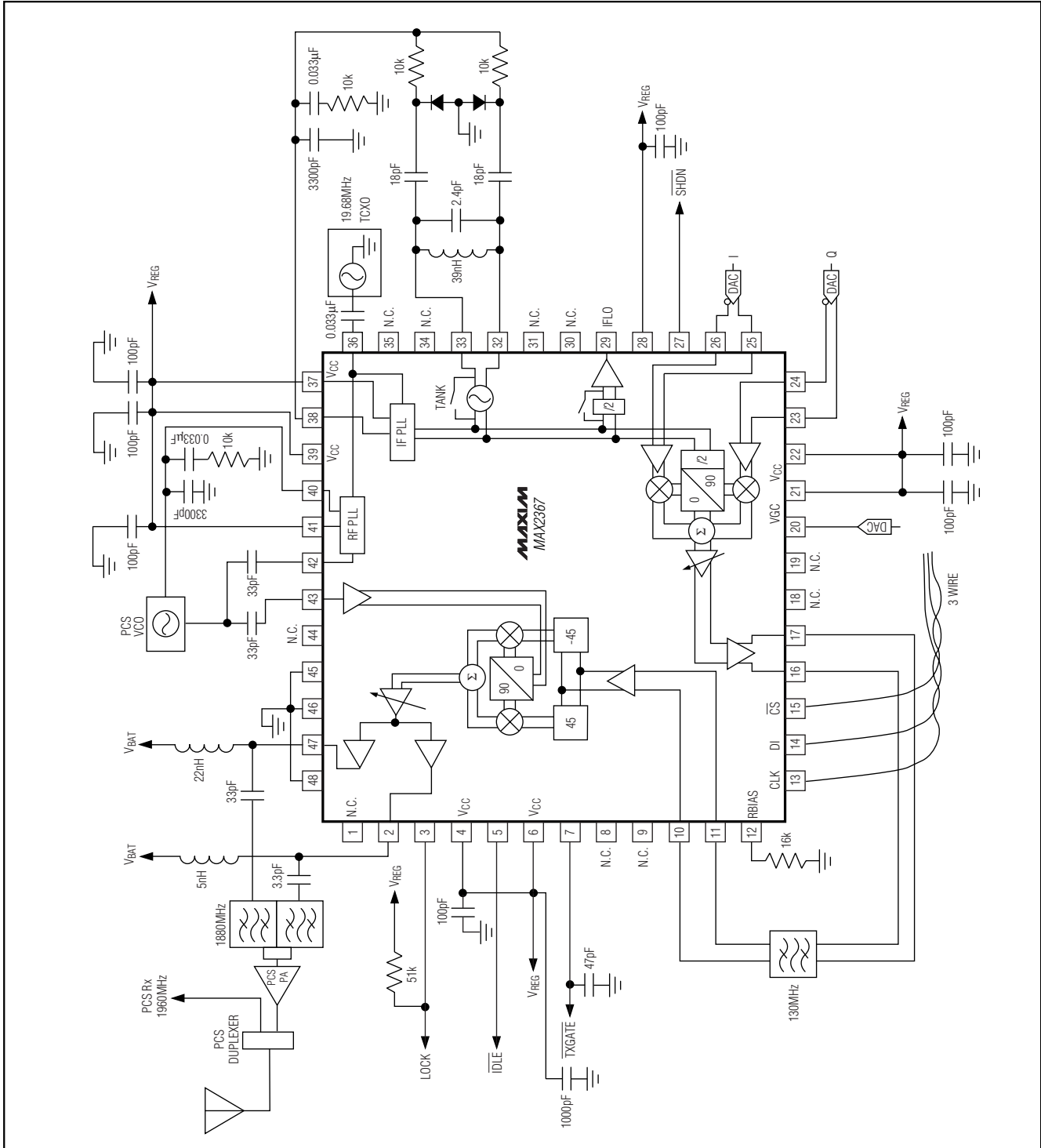


Figure 3. MAX2367 Typical Application Circuit

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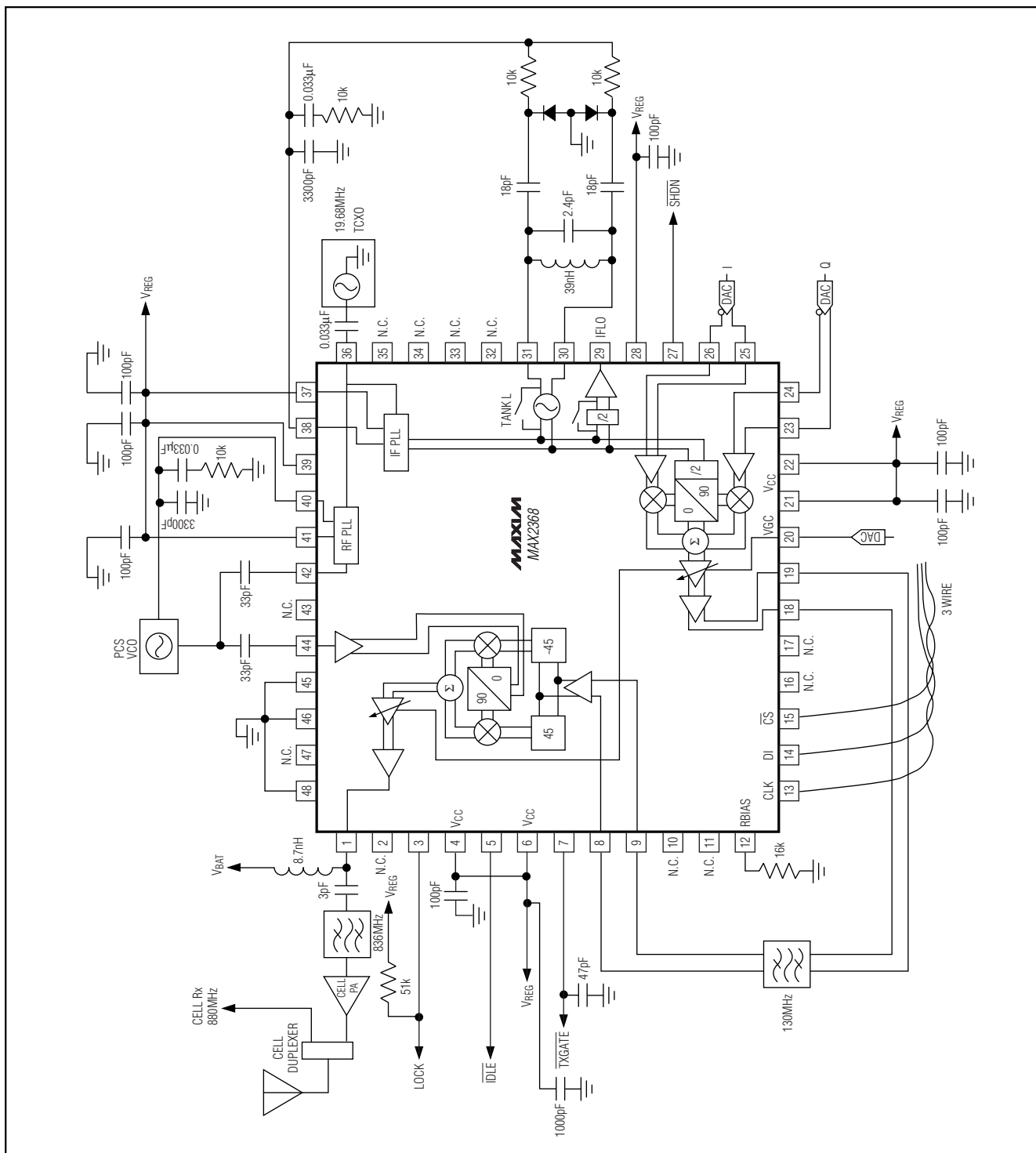


Figure 4. MAX2368 Typical Application Circuit

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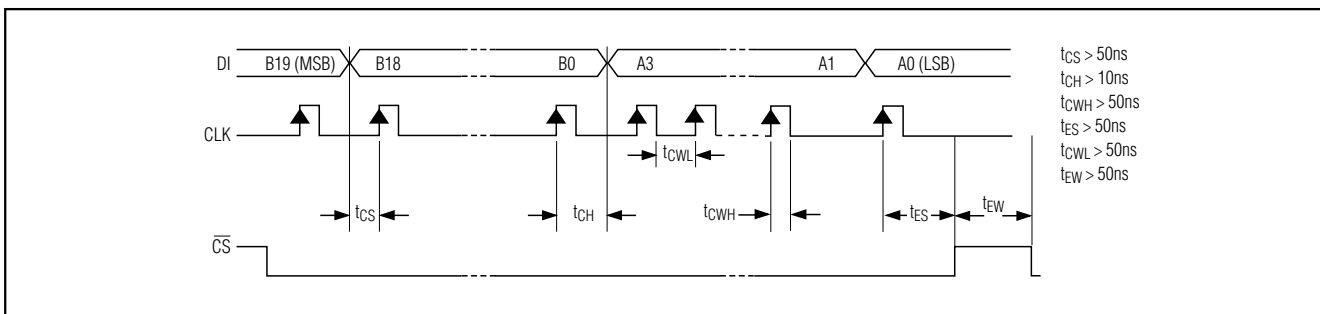


Figure 5. 3-Wire Interface Diagram

IF Tank Design

The low-band tank (TANKL+, TANKL-) and high-band tank (TANKH+, TANKH-) are fully differential. The external tank components are shown in Figure 6. The frequency of oscillation is determined by the following equation:

$$f_{OSC} = \frac{1}{2\pi \sqrt{(C_{INT} + C_{CENT} + C_{VAR} + C_{PAR}) L}}$$

$$C_{VAR} = \frac{C_D \times C_C}{2(C_D + C_C)}$$

C_{INT} = Internal capacitance of TANK port

C_D = Capacitance of varactor

C_{VAR} = Equivalent variable tuning capacitance

C_{PAR} = Parasitic capacitance due to PC board pads and traces

C_{CENT} = External capacitor for centering oscillation frequency

C_C = External coupling capacitor to the varactor

Internal to the IC, the charge pump will have a leakage of less than 10nA. This is equivalent to a 300M Ω shunt resistor. The charge-pump output must see an extremely high DC resistance of greater than 300M Ω . This will minimize charge-pump spurs at the comparison frequency. Make sure there is no solder flux under the varactor or loop filter.

Layout Issues

The MAX2366/MAX2367/MAX2368 EV kit can be used as a starting point for layout. For best performance, take into consideration power-supply issues, as well as the RF, LO, and IF layout.

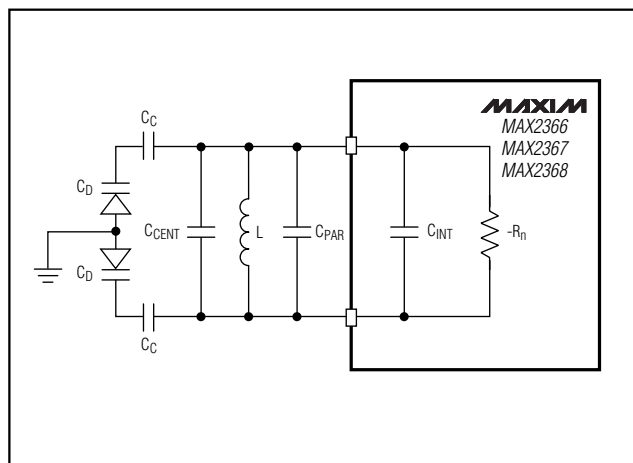


Figure 6. Tank Port Oscillator

Power-Supply Layout

To minimize coupling between different sections of the IC, the ideal power-supply layout is a star configuration, which has a large decoupling capacitor at a central VCC node. The VCC traces branch out from this node, each going to a separate VCC node in the MAX2366/MAX2367/MAX2368 circuit. At the end of each trace is a bypass capacitor with impedance to ground less than 1 Ω at the frequency of interest. This arrangement provides local decoupling at each VCC pin. Use at least one via per bypass capacitor for a low-inductance ground connection.

Matching Network Layout

The layout of a matching network can be very sensitive to parasitic circuit elements. To minimize parasitic inductance, keep all traces short and place components as close to the IC as possible. To minimize parasitic capacitance, a cutout in the ground plane (and

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any other planes) below the matching network components can be used.

On the high-impedance ports (e.g., IF inputs and outputs), keep traces short to minimize shunt capacitance.

Tank Layout

Keep the traces coming out of the tank short to reduce series inductance and shunt capacitance. Keep the inductor pads and coupling capacitor pads small to minimize stray shunt capacitance.

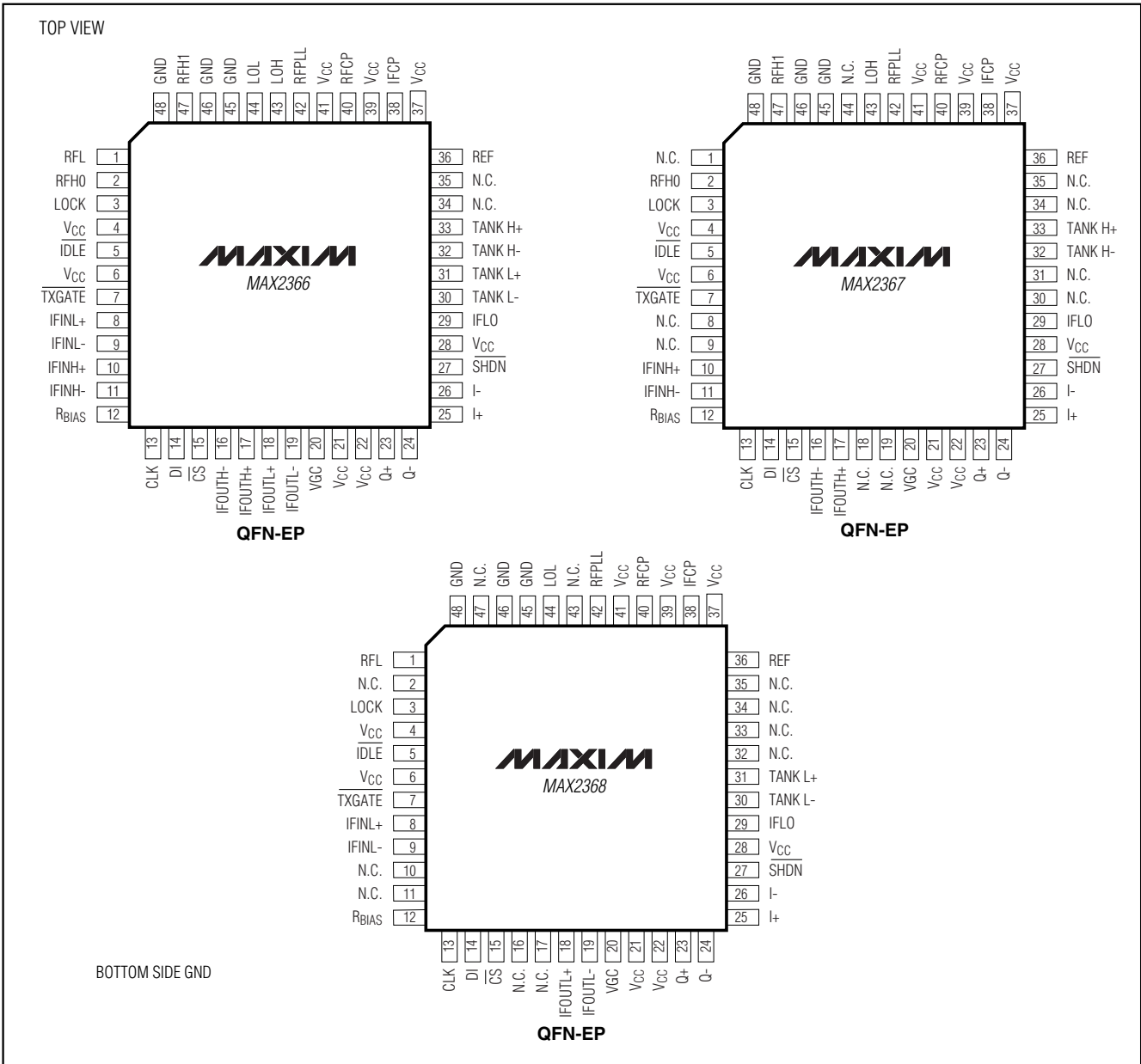
Selector Guide

| PART | IF RANGE (MHz) | RF LO RANGE (MHz) | RF RANGE (MHz) |
|---------|----------------|-------------------|----------------|
| MAX2366 | 120 to 235 | 800 to 1150 | 800 to 1000 |
| | 120 to 300 | 1400 to 2300 | 1700 to 2000 |
| MAX2367 | 120 to 300 | 1400 to 2300 | 1700 to 2000 |
| MAX2368 | 120 to 235 | 800 to 1150 | 800 to 1000 |

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Pin Configurations (continued)



Package Information

For the latest package outline information, go to www.maxim-ic.com/packages.

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