LVDS QUAD DIFFERENTIAL LINE DRIVER

FEATURES

- >400 Mbps (200 MHz) Signaling Rates
- Flow-Through Pinout Simplifies PCB Layout
- 300 ps Maximum Differential Skew
- Propagation Delay Times 1.8 ns (Typical)
- 3.3 V Power Supply Design
- ±350 mV Differential Signaling
- High Impedance on LVDS Outputs on Power Down
- Conforms to TIA/EIA-644 LVDS Standard
- Industrial Operating Temperature Range (-40°C to 85°C)
- Available in SOIC and TSSOP Packages

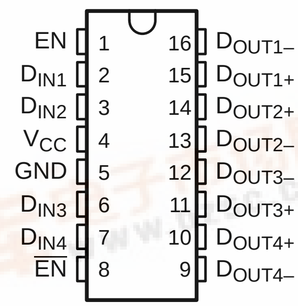
DESCRIPTION

The SN65LVDS047 is a quad differential linedriver that implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

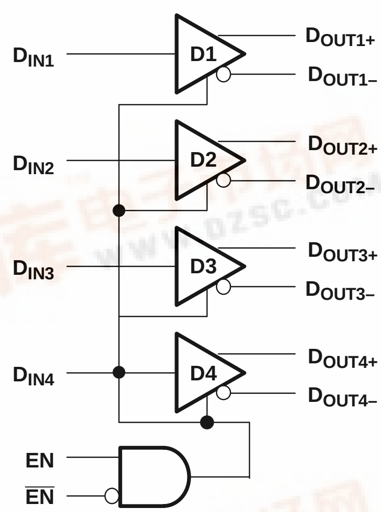
The intended application of this device and signaling technique is for point-to-point and multi-drop baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.

The SN65LVDS047 is characterized for operation from -40°C to 85°C.

D OR PW PACKAGE
(Marked as LVDS047)
(TOP VIEW)



functional block diagram



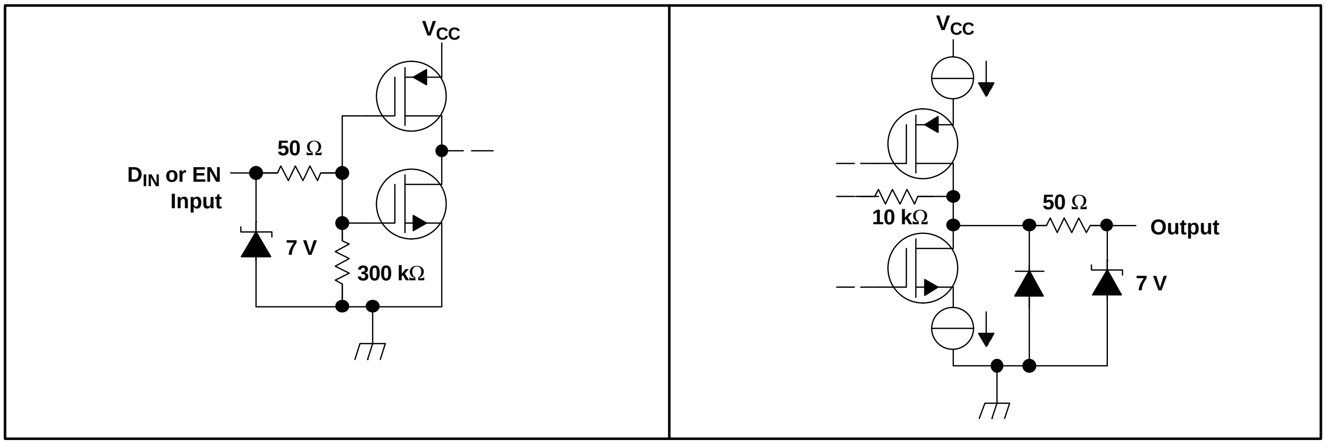
TRUTH TABLE(1)

INPUT	ENABLES		OUTPUTS	
D_{IN}	EN	$\overline{EN}$	D_{OUT+}	D_{OUT-}
L	H	L or OPEN	L	H
H			H	L
X	All other conditions		Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature (see [2] range (unless otherwise noted)

		UNIT
(V_{CC})	Supply voltage	-0.3 V to 4 V
$V_I(D_{IN})$	Input voltage range	-0.3 V to (V_{CC} +0.3 V)
(EN, $\overline{EN}$)	Enable input voltage	-0.3 V to (V_{CC} +0.3 V)
$V_O(D_{OUT+},D_{OUT-})$	Output voltage	-0.5 V to (V_{CC} +0.5 V)
(D_{OUT+},D_{OUT-})	Bus-pin--electrostatic discharge, see [3]	>10 kV
($D_{OUT+},(D_{OUT-}$)	Short circuit duration	Continuous
	Storage temperature range	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR[1] ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
PW	774 mW	6.2 mW/°C	402 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	-40	25	85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (see [(1)] and [(2)]) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[(3)]	MAX	UNIT
V_{OD}	Differential output voltage	R_L = 100 Ω, see Figure 1	250	310	450	mV
$n\|V_{OD}\|$	Change in magnitude of V_{OD} for complementary output states			1	35	|mV|
$V_{OC(SS)}$	Steady-state, common-mode output voltage		1.125	1.17	1.375	V
$nV_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			1	25	|mV|
V_{OH}	Output high voltage			1.33	1.6	V
V_{OL}	Output low voltage		0.90	1.02		V
V_{IH}	Input high voltage		2		V_{CC}	V
V_{IL}	Input low voltage		GND		0.8	V
I_{IH}	Input high current	$V_{IN} = V_{CC}$ or 2.5 V	-10	3	10	µA
I_{IL}	Input low current	V_{IN} = GND or 0.4 V	-10	1	10	µA
V_{IK}	Input clamp voltage	I_{CL} = -18 mA	-1.5	-0.8		V
I_{OS}	Output short circuit current, see [(4)]	Enabled, $D_{IN} = V_{CC}$, D_{OUT+} = 0 V or D_{IN} = GND, D_{OUT-} = 0 V		-3.1	-9	mA
I_{OSD}	Differential output short circuit current, see [(4)]	Enabled, V_{OD} = 0 V			-9	mA
I_{OFF}	Power-off leakage	V_O = 0 V or 3.6 V, V_{CC} = 0 V or Open	-1		1	µA
I_{OZ}	Output 3-state current	EN = 0.8 V and $\overline{EN}$ = 2 V, V_O = 0 V or V_{CC}	-1		1	µA
I_{CC}	No load supply current, drivers enabled	$D_{IN} = V_{CC}$ or GND		7		mA
I_{CCL}	Loaded supply current, drivers enabled	R_L = 100 Ω all channels, $D_{IN} = V_{CC}$ or GND (all inputs)		20	26	mA
$I_{CC(Z)}$	No load supply current, drivers disabled	$D_{IN} = V_{CC}$ or GND, EN = GND, $\overline{EN} = V_{CC}$		0.5	1.3	mA

(1) Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.
(2) The SN65LVDS047 is a current mode device and only functions within data sheet specifications when a resistive load is applied to the driver outputs, 90 Ω to 110 Ω typical range.
(3) All typical values are given for: V_{CC} = 3.3 V, T_A = 25°C.
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

SWITCHING CHARACTERISTICS

over recommended operating conditions (see (1), (2) and (3))(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(4)	MAX	UNIT
t_{PHL}	Differential propagation delay, high-to-low	R_L = 100 Ω,, C_L = 15 pF, see Figure 2 and Figure 3	1.4	1.8	2.8	ns
t_{PLH}	Differential propagation delay, low-to-high		1.4	1.8	2.8	ns
$t_{SK(p)}$	Differential pulse skew (t_{PHLD} - t_{PLHD}), see (5)			50	300	ps
$t_{SK(o)}$	Channel-to-channel skew, see (6)			40	300	ps
$t_{SK(pp)}$	Differential part-to-part skew, see (7)				1	ns
$t_{SK(lim)}$	Differential part-to-part skew, see (8)				1.2	ns
t_r	Rise time			0.5	1.5	ns
t_f	Fall time			0.5	1.5	ns
t_{PHZ}	Disable time high to Z	R_L = 100 Ω,, C_L = 15 pF, see Figure 4 and Figure 5		5.5	8	ns
t_{PLZ}	Disable time low to Z			5.5	8	ns
t_{PZH}	Enable time Z to high			8.5	12	ns
t_{PZL}	Enable time Z to low			8.5	12	ns
$f_{(MAX)}$	Maximum operating frequency, see (9)			250		MHz

(1) Generator waveform for all tests unless otherwise: f = 1 MHz, Z_o = 50 Ω, t_r < 1 ns, and t_f < 1 ns.
(2) C_L includes probe and jig capacitance.
(3) All input voltages are for one channel unless otherwise specified. Other inputs are set to GND.
(4) All typical values are given for: V_{CC} = 3.3 V, T_A = 25°C.
(5) $t_{SK(p)}|t_{PHL}-t_{PLH}|$ is the magnitude difference in differential propagation delay time between the positive going edge andthe negative going edge of the same channel.
(6) $t_{SK(o)}$ is the differential channel-to-channel skew of any event on the same device.
(7) $t_{SK(pp)}$ is the differential part-to-part skew, and is defined as the difference between the minimum and the maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(8) $t_{SK(lim)}$ part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. $t_{SK(lim)}$ is defined as|Min - Max| differential propagation delay.
(9) $f_{(MAX)}$ generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% to55,V_{OD} > 250 mV, all channels switching

PARAMETER MEASUREMENT INFORMATION

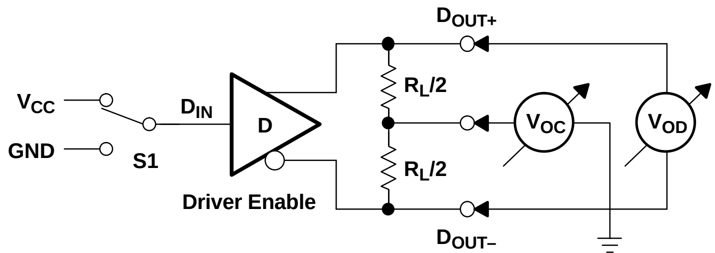


Figure 1. Driver V_{OD} and V_{OC} Test Circuit

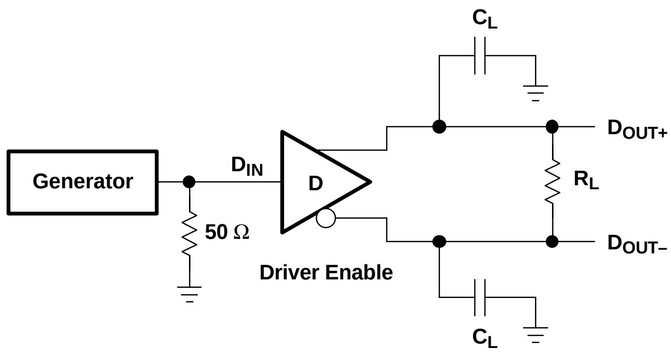


Figure 2. Driver Propagation Delay and Transition Time Test Circuit

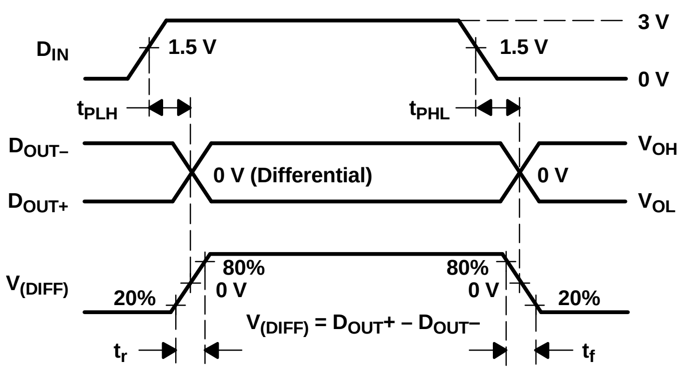


Figure 3. Driver Propagation Delay and Transition Time Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

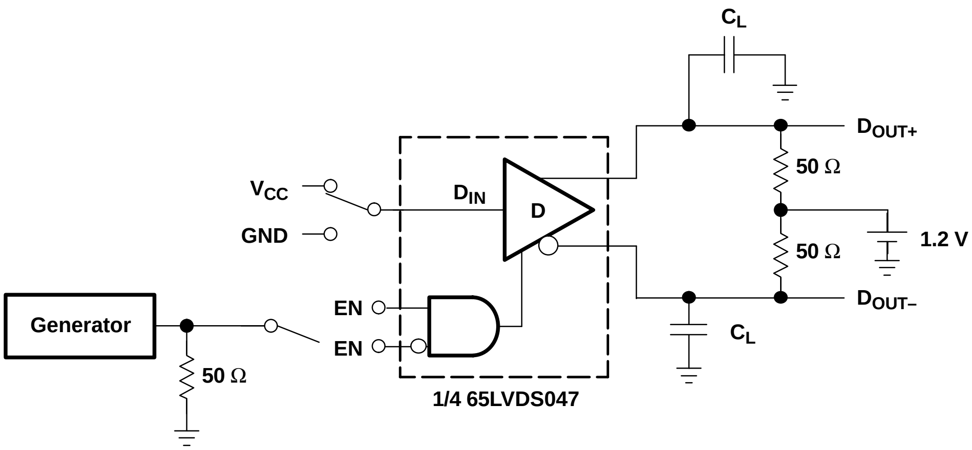


Figure 4. Driver 3-State Delay Test Circuit

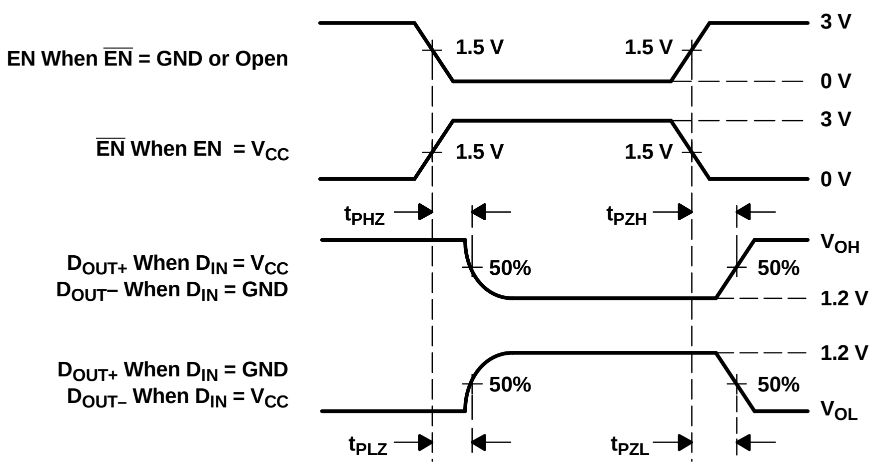


Figure 5. Driver 3-State Delay Waveform

TYPICAL CHARACTERISTICS

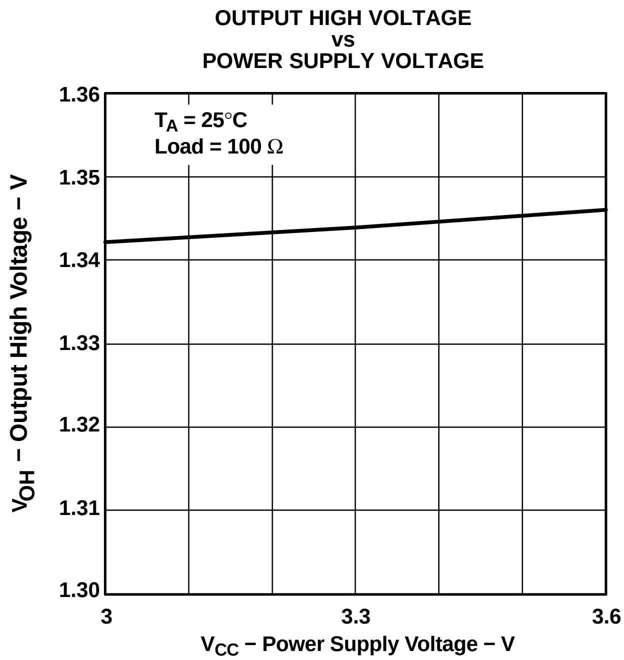


Figure 6.

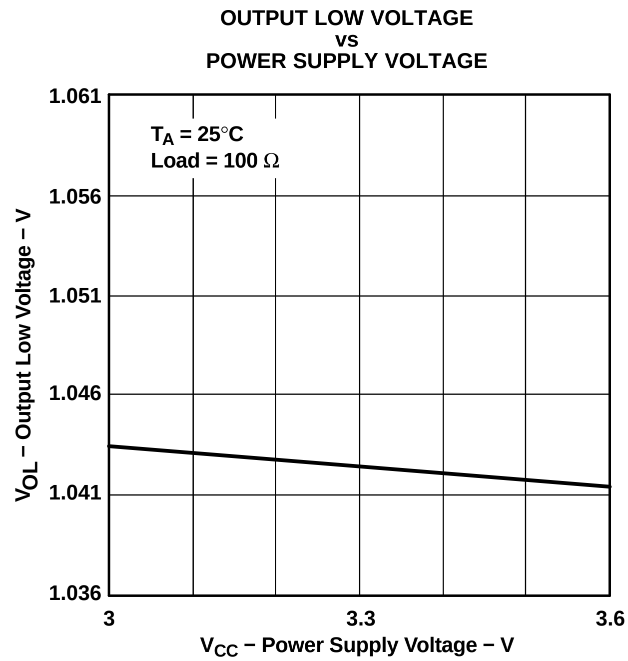


Figure 7.

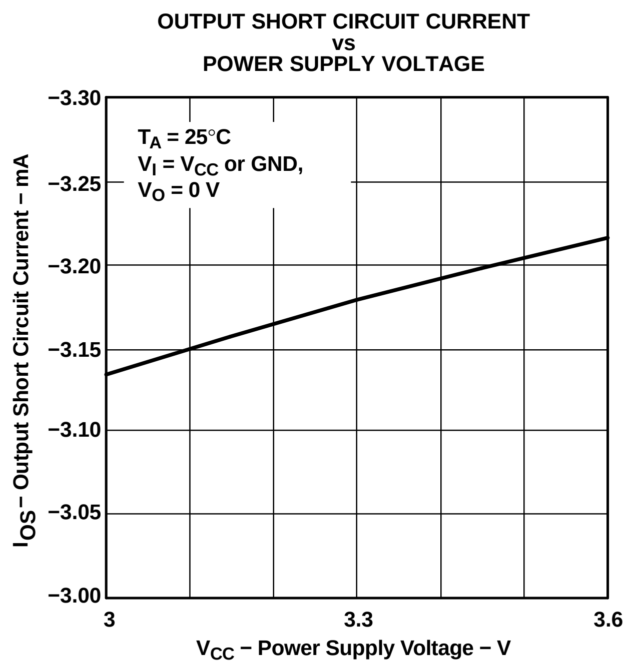


Figure 8.

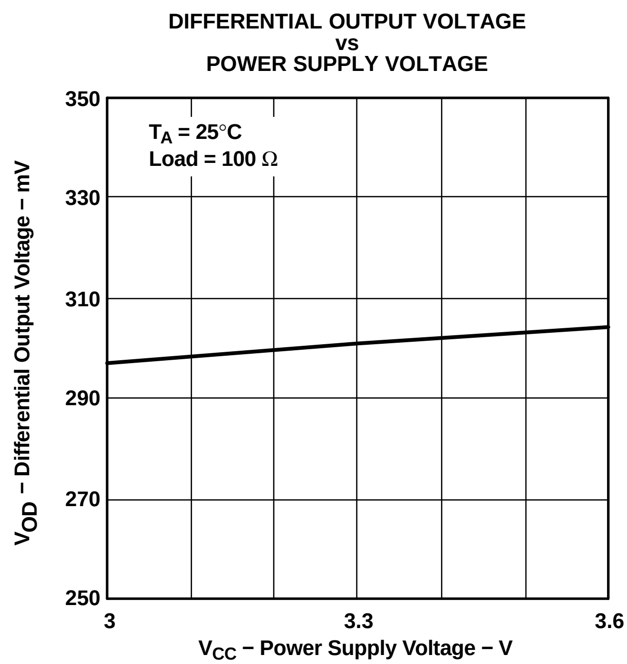


Figure 9.

TYPICAL CHARACTERISTICS (continued)

COMMON-MODE OUTPUT VOLTAGE vs POWER SUPPLY VOLTAGE

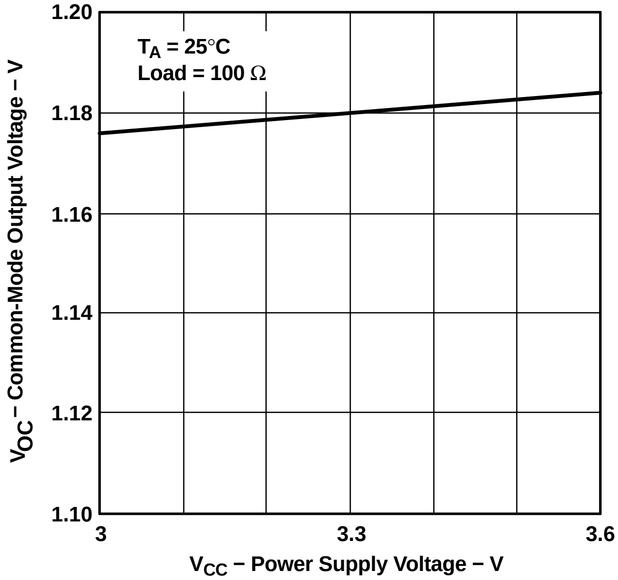


Figure 10.

POWER SUPPLY CURRENT vs FREQUENCY

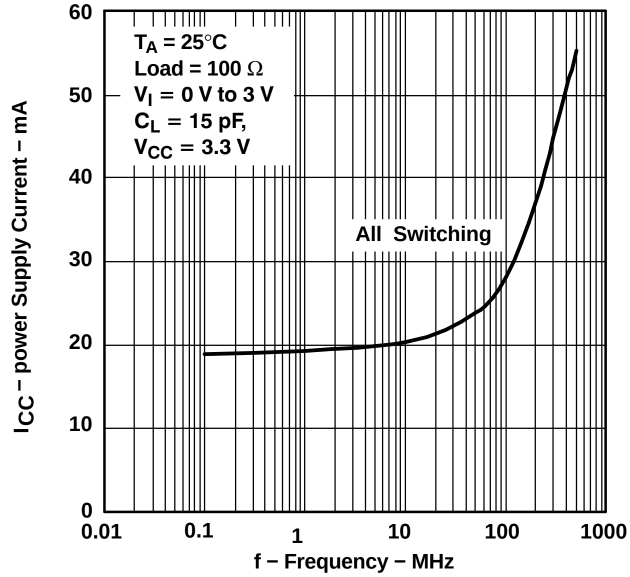


Figure 11.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVDS047D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS047DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS047DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS047DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS047PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS047PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS047PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS047PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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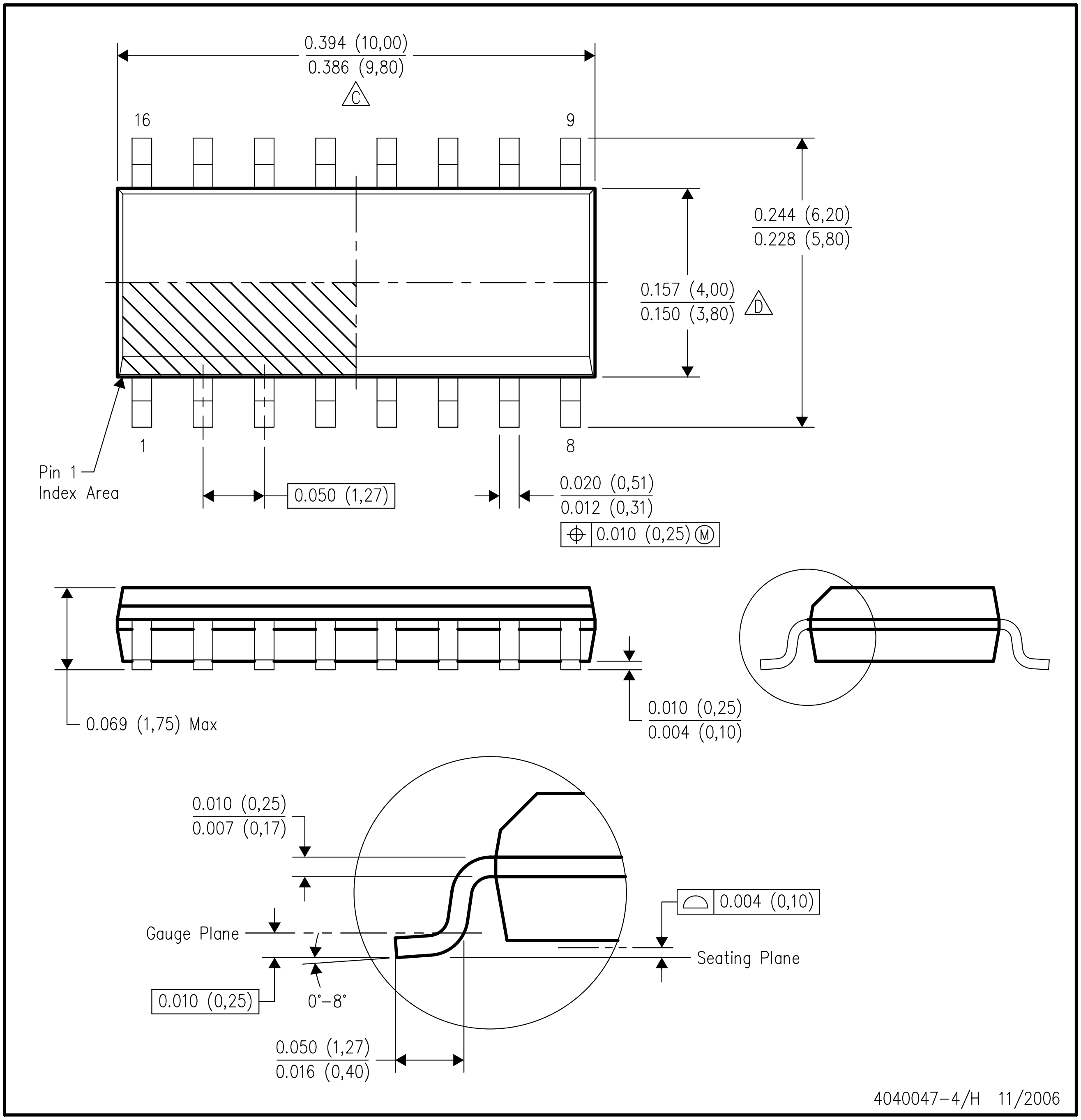
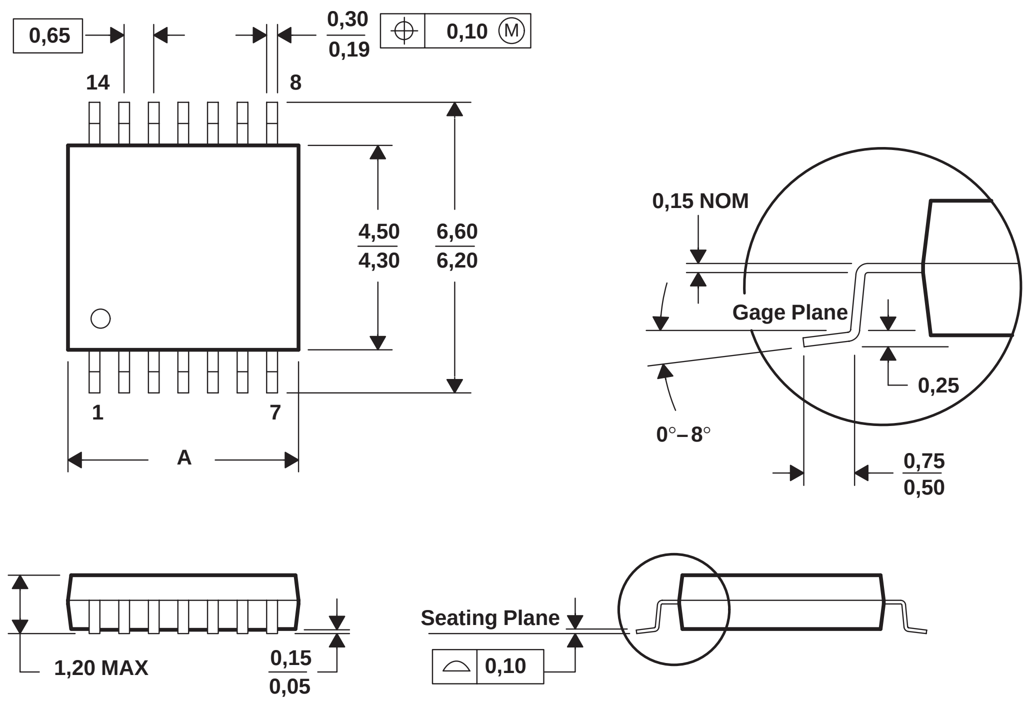
D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS–012 variation AC.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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