ISO 9001 CERTIFIED BY DSCC

# HIGH EFFICIENCY, 4 AMP STEP-DOWN SWITCHING REGULATORS

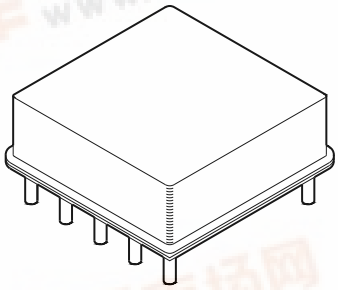
# 5030 SERIES

M.S.KENNEDY CORP.
4707 Dey Road Liverpool, N.Y. 13088 (315) 701-6751

## FEATURES:

MIL-PRF-38534 QUALIFIED

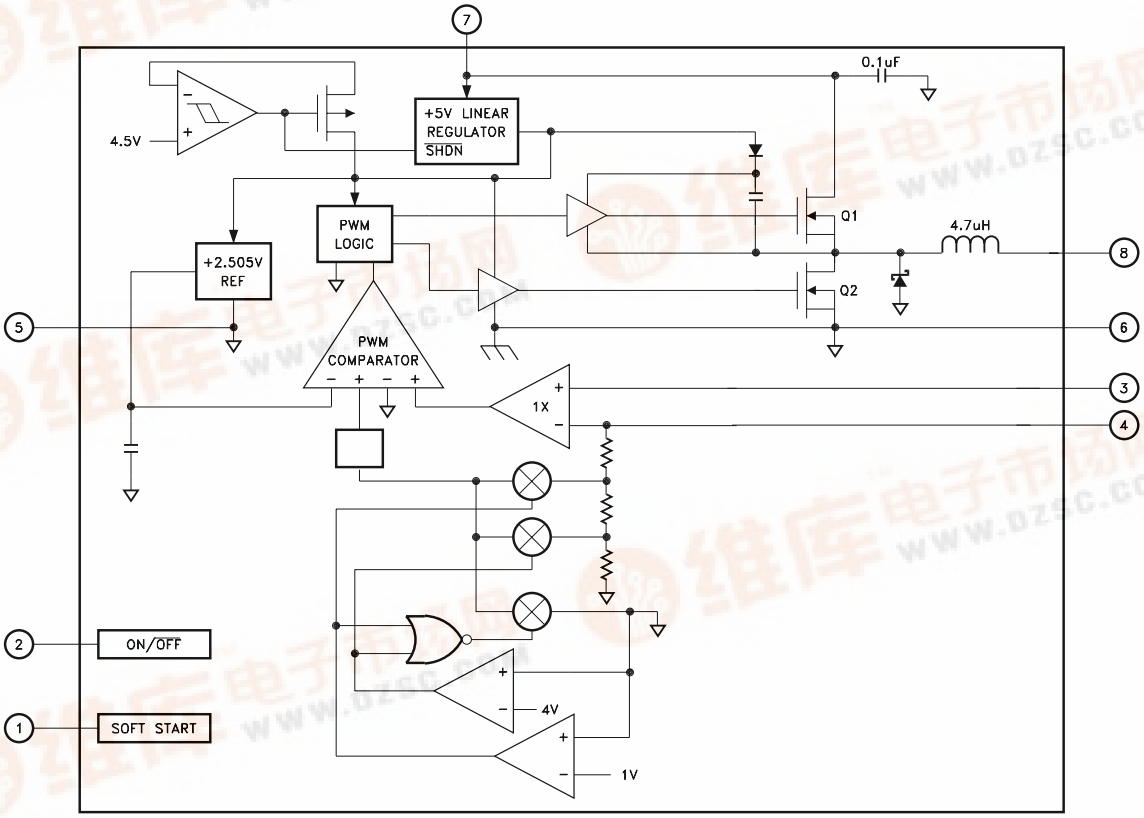
- Up To 95% Efficiency For 5V Version
- 4 Amp Output Current
- 4.5V to 30V Input Range
- Preset 2.5V, 3.3V or 5.0V Output Versions
- 300KHz Switching Frequency @ 1 Amp
- User Programmable Soft-Start
- Quiescent Current < 0.5mA
- User Programmable Current Limit



## DESCRIPTION:

The MSK 5030 series are high efficiency, 4 amp, step-down switching regulators. The output voltage is configured for 2.5V, 3.3V or 5.0V internally and the input range is 4.5V to 30V. The operating frequency of the MSK 5030 is 300KHz and is internally set. An external "soft start" capacitor allows the user to control how quickly the output comes up to regulation voltage after the application of an input. An extremely low quiescent current of typically less than 0.5mA and 95% operating efficiency keeps the total internal power dissipation of the MSK 5030 down to an absolute minimum. A surface mount version, MSK 5040, is also available if desired.

## EQUIVALENT SCHEMATIC




## TYPICAL APPLICATIONS

- Step-down Switching Regulator
- Microprocessor Power Source
- High Efficiency Low Voltage Subsystem Power Supply

## PIN-OUT INFORMATION

| | | | |
|---|---|---|---|
| 1 | Cton | | |
| 2 | Enable | 8 | Output |
| 3 | Sense High | 7 | Input |
| 4 | Sense Low | 6 | PGround |
| 5 | Ground | | |

## ABSOLUTE MAXIMUM RATINGS

Input Voltage . . . . . -0.3V, +36V
Enable Voltage . . . . . -0.3V, +36V
Output Current . . . . . 4.0 Amps
Sense Pin Voltage . . . . . -0.3V, +7V
Thermal Resistance
(Each MOSFET) . . . . . 15°C/W

$T_{ST}$ Storage Temperature Range . . -65°C to +150°C
$T_{LD}$ Lead Temperature Range . . . . . 300°C
(10 Seconds)
$T_C$ Case Operating Temperature
MSK5030 Series . . . . . -40°C to +85°C
MSK5030B/E Series . . . . . -55°C to +125°C
$T_J$ Junction Temperature . . . . . +150°C

## ELECTRICAL SPECIFICATIONS

| Parameter | | Test Conditions ① | Group A Subgroup | MSK 5030B/E SERIES Min. | Typ. | Max. | MSK 5030 SERIES Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Input Supply Range ② | | | 1,2,3 | 4.5 | - | 30 | 5.0 | - | 30 | V |
| Output Voltage 5030-2.5 ⑧ | | $I_{OUT}$ = 1A $V_{IN}$ = 4.5V | 1 | 2.40 | 2.51 | 2.63 | 2.26 | 2.51 | 2.76 | V |
| Output Voltage 5030-3.3 ⑧ | | $I_{OUT}$ = 1A $V_{IN}$ = 4.5V | 1 | 3.19 | 3.35 | 3.47 | 3.05 | 3.35 | 3.55 | V |
| Output Voltage 5030-5.0 ⑧ | | $I_{OUT}$ = 1A $V_{IN}$ = 6V | 1 | 4.85 | 5.1 | 5.25 | 4.75 | 5.1 | 5.35 | V |
| Output Current ② | | Within SOA | 1 | 4.0 | 4.5 | - | 4.0 | 4.5 | - | A |
| Load Regulation ② | | Output not current limited | - | - | 2.5 | - | - | 2.5 | - | % |
| Line Regulation | | $I_{OUT}$ = 1A 6V≤$V_{IN}$≤30V | 1,2,3 | - | 0.04 | 0.07 | - | 0.04 | 0.08 | %/V |
| Quiescent Power Consumption ② | | $I_{OUT}$ = 0mA | - | - | 5.0 | - | - | 5.0 | - | mW |
| Oscillator Frequency ② ⑦ | | Internal $I_{OUT}$≥1.5A | - | 270 | 300 | 330 | 270 | 300 | 330 | KHz |
| Enable Input Voltage ② | | High | 1,2,3 | 2.0 | - | - | 2.0 | - | - | V |
| | | Low | 1,2,3 | - | - | 0.5 | - | - | 0.5 | V |
| Enable Input Current ② | | $V_{EN}$ = $V_{IN}$ | 1 | - | 0.5 | 2.0 | - | 0.5 | 2.0 | µA |
| | | $V_{EN}$ = 0V | 1 | - | 0.2 | 2.0 | - | 0.2 | 2.0 | µA |
| Disabled Quiescent Current ② | | $V_{EN}$ = 0V $V_{IN}$ = 30V | 1 | - | 1.0 | 5.0 | - | 1.0 | 5.0 | µA |
| Current Limit Threshold ② | | Positive | 1 | 80 | 100 | 120 | 75 | 100 | 125 | mV |
| | | Negative | 1 | -50 | -100 | -160 | -45 | -100 | -165 | mV |
| Cton Current ② | | Source | 1 | 2.5 | 4.0 | 6.5 | 2.5 | 4.0 | 6.5 | µA |
| | | Fault Sink | 1 | 2.0 | - | - | 2.0 | - | - | mA |
| Efficiency ② | 5030-2.5 | $V_{IN}$ = 4.5V $I_{OUT}$ = 1A | 1 | - | 80 | - | - | 80 | - | % |
| | 5030-3.3 | $V_{IN}$ = 4.5V $I_{OUT}$ = 1A | 1 | - | 90 | - | - | 90 | - | % |
| | 5030-5.0 | $V_{IN}$ = 6V $I_{OUT}$ = 1A | 1 | - | 95 | - | - | 95 | - | % |

*NOTES:*

① $V_{IN}$ = Enable, 5mV≤(sense high-sense low)≤75mV, $I_L$ = 0A, $C_{OUT}$ = 5x220µF, $C_{IN}$ = 2x22µF, $C_{TON}$ = 0.01µF unless otherwise specified.
② Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
③ All output parameters are tested using a low duty cycle pulse to maintain $T_J$ = $T_C$.
④ Industrial grade and "E" suffix devices shall be tested to subgroup 1 unless otherwise specified.
⑤ Military grade devices ('B' suffix) shall be 100% tested to subgroups 1,2 and 3.
⑥ Subgroup 1 $T_A$ = $T_C$ = +25°C
Subgroup 2 $T_A$ = $T_C$ = +125°C
Subgroup 3 $T_A$ = $T_C$ = -55°C
⑦ Actual switching frequency is load dependent. Refer to typical performance curves.
⑧ Alternate output voltages are available. Please contact the factory.

## APPLICATION NOTES

### *CURRENT LIMITING:*

The MSK 5030 is equipped with a pair of sense pins that are used to sense the load current using an external resistor (Rs). The current-limit circuit resets the main PWM latch and turns off the internal high-side MOSFET switch whenever the voltage difference between Sense High and Sense Low exceeds 100mV. This limiting occurs in both current flow directions, putting the threshold limit at ±100mV. The tolerance on the positive current limit is ±20%. The external low-value sense resistor must be sized for 80mV/Rs to guarantee enough load capacity. Load components must be designed to withstand continuous current stresses of 120mV/Rs.

For very high-current applications, it may be useful to wire the sense inputs with a twisted pair instead of PCB traces. This twisted pair needn't be anything unique, perhaps two pieces of wire-wrap wire twisted together. Low inductance current sense resistors, such as metal film surface mount styles are best.

### *SOFT START/Cton:*

The internal soft-start circuitry allows a gradual increase of the internal current-limit level at start-up for the purpose of reducing input surge currents, and possibly for power-supply sequencing. In Disable mode, the soft-start circuit holds the Cton capacitor discharged to ground. When Enable goes high, a 4$\mu$A current source charges the Cton capacitor up to 3.2V. The resulting linear ramp causes the internal current-limit threshold to increase proportionally from 20mV to 100mV. The output capacitors charge up relatively slowly, depending on the Cton capacitor value. The exact time of the output rise depends on output capacitance and load current and is typically 1mS per nanofarad of soft-start capacitance. With no capacitor connected, maximum current limit is reached typically within 10$\mu$S.

### *ENABLE FUNCTION:*

The MSK 5030 is enabled by applying a logic level high to the Enable pin. A logic level low will disable the device and quiescent input current will reduce to approximately 1$\mu$A. The Enable threshold voltage is 1V. If automatic start up is required, simply connect the pin to $V_{IN}$. Maximum Enable voltage is +36V.

### *POWER DISSIPATION:*

In high current applications, it is very important to ensure that both MOSFETS are within their maximum junction temperature at high ambient temperatures. Temperature rise can be calculated based on package thermal resistance and worst case dissipation for each MOSFET. These worst case dissipations occur at minimum voltage for the high side MOSFET and at maximum voltage for the low side MOSFET.

Calculate power dissipation using the following formulas:

$$Pd\ (upper\ FET) = I_{LOAD}^2 \times 0.035\Omega \times DUTY + V_{IN} \times I_{LOAD} \times f \times \left[\frac{V_{IN} \times C_{RSS}}{I_{GATE}} + 20ns\right]$$

$$Pd\ (lower\ FET) = I_{LOAD}^2 \times 0.035\Omega \times (1\text{-}DUTY)$$

$$DUTY = \left[\frac{(V_{OUT} + V_{Q2})}{(V_{IN} - V_{Q1})}\right]$$

Where: $V_{Q1}$ or $V_{Q2}$ (on state voltage drop) = $I_{LOAD} \times 0.035\Omega$

$C_{RSS}$ = 94pF

$I_{GATE}$ = 1A

During output short circuit, Q2, the synchronous-rectifier MOSFET, will have an increased duty factor and will see additional stress. This can be calculated by:

$$Q2\ DUTY = 1 - \left[\frac{V_{Q2}}{V_{IN(MAX)} - V_{Q1}}\right]$$

### *INPUT CAPACITOR SELECTION:*

The MSK 5030 has an internal high frequency ceramic capacitor (0.1uF) between $V_{IN}$ and GND. Connect a low-ESR bulk capacitor directly to the input pin of the MSK 5030. Select the bulk input filter capacitor according to input ripple-current requirements and voltage rating, rather than capacitor value. Electrolytic capacitors that have low enough ESR to meet the ripple-current requirement invariably have more than adequate capacitance values. Aluminum-electrolytic capacitors are preferred over tantalum types, which could cause power-up surge-current failure when connecting to robust AC adapters or low-impedance batteries. RMS input ripple current is determined by the input voltage and load current, with the worst possible case occuring at $V_{IN} = 2 \times V_{OUT}$:

$$I_{RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

### *OUTPUT CAPACITOR SELECTION:*

The output capacitor values are generally determined by the ESR and voltage rating requirements rather than capacitance requirements for stability. Low ESR capacitors that meet the ESR requirement usually have more output capacitance than required for stability. Only specialized low-ESR capacitors intended for switching-regulator applications, such as AVX TPS, Sprague 595D, Sanyo OS-CON, Nichicon PL series or Kemet T510 series should be used. The capacitor must meet minimum capacitance and maximum ESR values as given in the following equations:

$$C_F > \frac{2.5V(1 + V_{OUT}/V_{IN(MIN)})}{V_{OUT} \times R_{SENSE} \times f}$$

$$R_{ESR} < \frac{R_{SENSE} \times V_{OUT}}{2.5V}$$

These equations provide 45 degrees of phase margin to ensure jitter-free fixed-frequency operation and provide a damped output response for zero to full-load step charges. Lower quality capacitors can be used if the load lacks large step charges. Bench testing over temperature is recommended to verify acceptable noise and transient response. As phase margin is reduced, the first symptom is timing jitter, which shows up in the switching waveforms. Technically speaking, this typically harmless jitter is unstable operation, since the swithcing frequency is non-constant. As the capacitor ESR is increased, the jitter becomes worse. Eventually, the load-transient waveform has enough ringing on it that the peak noise levels exceed the output voltage tolerance. With zero phase margin and instability present, the output voltage noise never gets much worse than $I_{PEAK} \times R_{ESR}$ (under constant loads). Designers of industrial temperature range digital systems can usually multiply the calculated ESR value by a factor of 1.5 without hurting stability or transient response.

The output ripple is usually dominated by the ESR of the filter capacitors and can be approximated as $I_{RIPPLE} \times R_{ESR}$. Including the capacitive term, the full equation for ripple in the continuous mode is $V_{NOISE(p\text{-}p)} = I_{RIPPLE} \times (R_{ESR} + 1/(2\pi fC))$. In idle mode, the inductor current becomes discontinuous with high peaks and widely spaced pulses, so the noise can actually be higher at light load compared to full load. In idle mode, the output ripple can be calculated as follows:

$$V_{NOISE(p\text{-}p)} = \frac{0.02 \times R_{ESR}}{R_{SENSE}} + \frac{0.0003 \times 4.7\mu H \times [1/V_{OUT} + 1/(V_{IN} - V_{OUT})]}{(R_{SENSE})^2 \times C}$$

## APPLICATION NOTES CONT'D

*MODES OF OPERATION:*

Under heavy loads, the MSK 5030 operates in full PWM mode. Each pulse from the oscillator sets the internal PWM latch that turns on the high-side MOSFET. As the high-switch turns off, the synchronous rectifier latch is set. 60ns later the low-side MOSFET turns on until the start of the next clock cycle or until the inductor current crosses zero. Under fault conditions the current exceeds the ±100mV current-limit threshold and the high-side switch turns off.

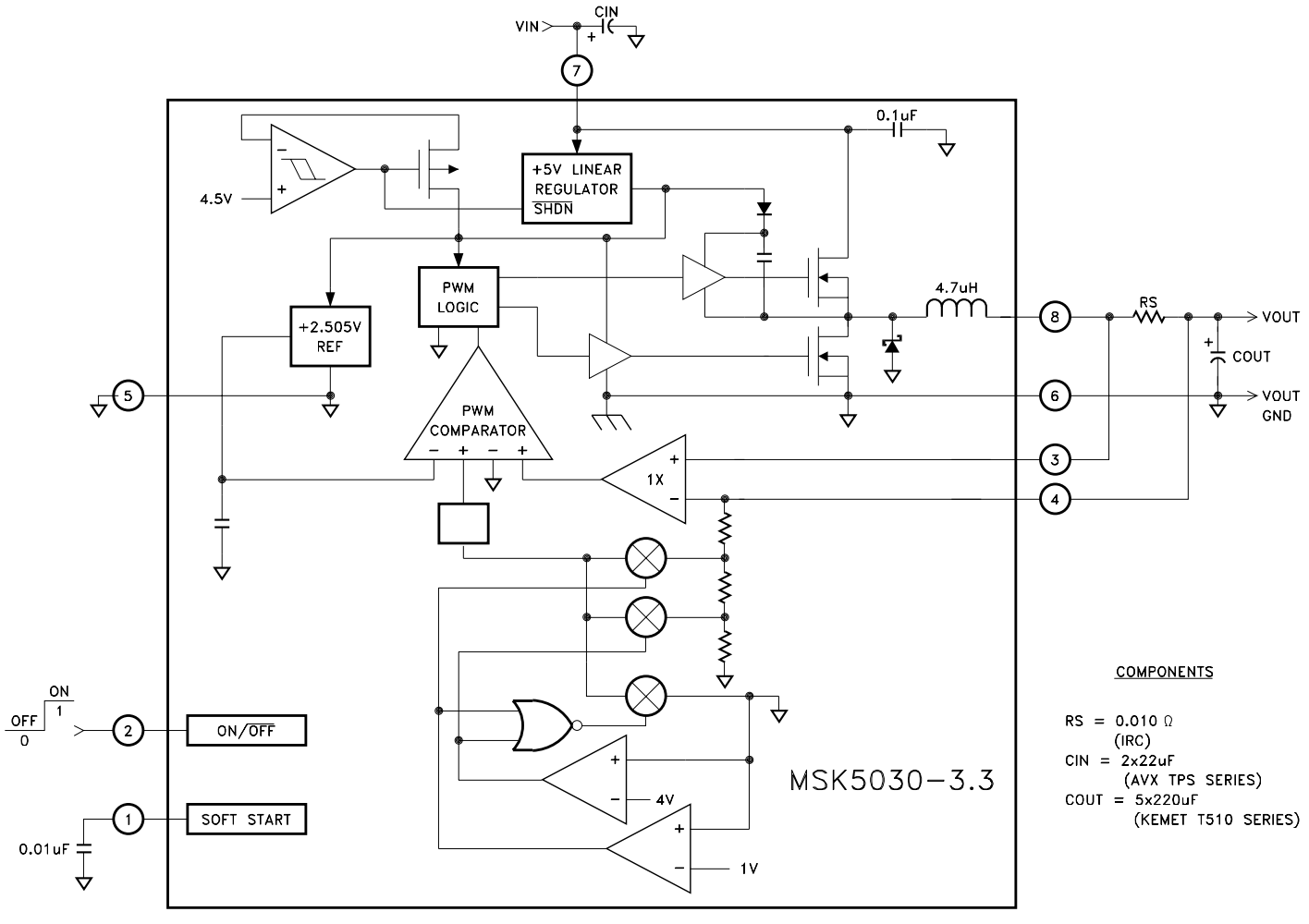
At light loads the inductor current does not exceed the 30mV threshold set by the minimum-current comparator. When this occurs, the MSK 5030 goes into idle mode, skipping most of the oscillator pulses in order to reduce the switching frequency and cut back gate-charge losses. The oscillator is gated off at light loads because the minimum-current comparator immediately resets the high-side latch at the start of each cycle. Refer to Table 1 for the operational characteristics.

### OPERATIONAL CHARACTERISTICS

| ENABLE | LOAD | DESCRIPTION |
|---|---|---|
| 0 | X | DEVICE DISABLED |
| 1 | LOW <10% | PULSE SKIPPING MODE DISCONTINUOUS INDUCTOR CURRENT |
| 1 | MED <30% | PULSE SKIPPING MODE CONTINUOUS INDUCTOR CURRENT |
| 1 | HIGH >30% | CONSTANT FREQ. PWM MODE CONTINUOUS INDUCTOR CURRENT |

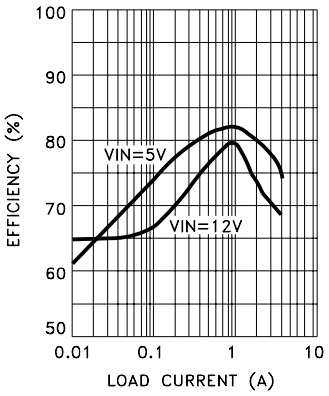
**TABLE 1**

### TYPICAL 3.3V APPLICATION CIRCUIT

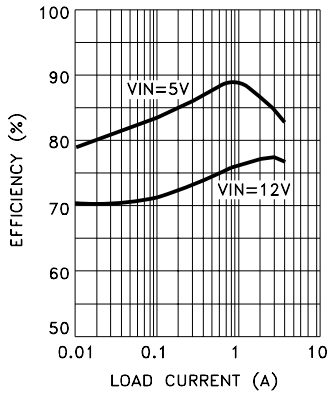


## TYPICAL PERFORMANCE CURVES

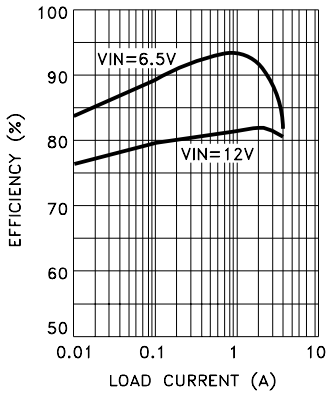
EFFICIENCY vs LOAD CURRENT
MSK5030–2.5



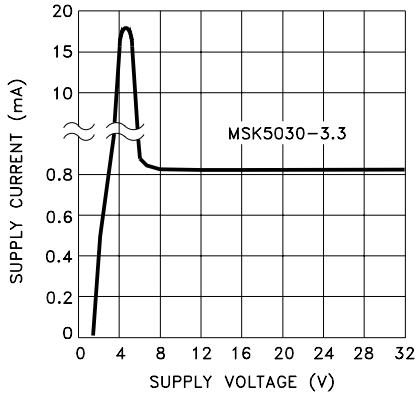

EFFICIENCY vs LOAD CURRENT
MSK5030–3.3



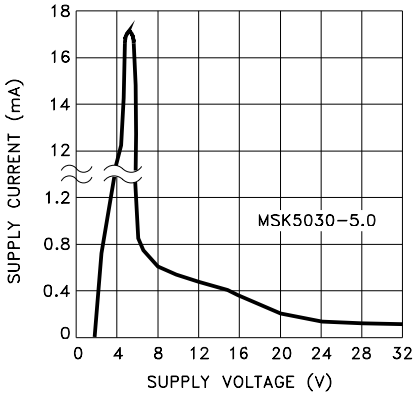

EFFICIENCY vs LOAD CURRENT
MSK5030–5.0



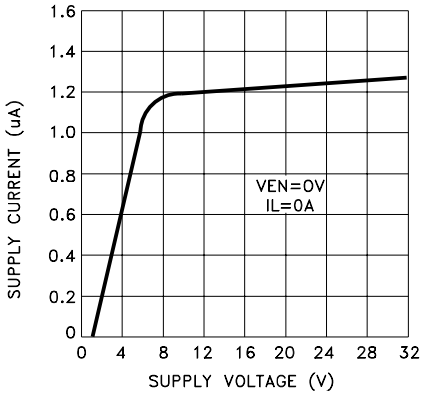

QUIESCENT SUPPLY CURRENT vs
SUPPLY VOLTAGE IN IDLE MODE



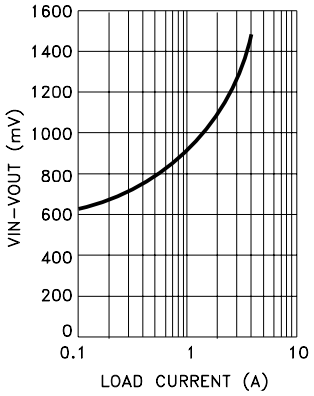

QUIESCENT SUPPLY CURRENT vs
SUPPLY VOLTAGE IN IDLE MODE



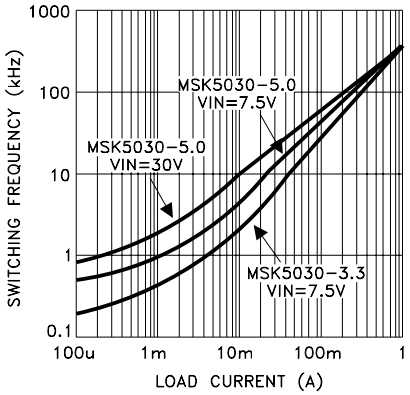

DISABLED SUPPLY CURRENT vs SUPPLY VOLTAGE



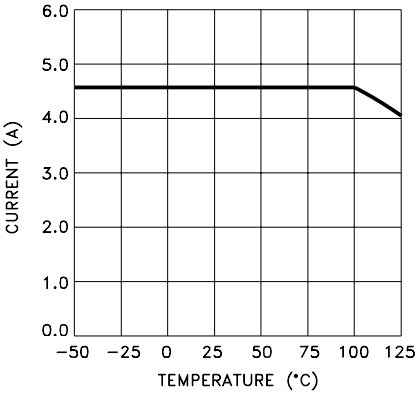

DROPOUT VOLTAGE vs LOAD CURRENT



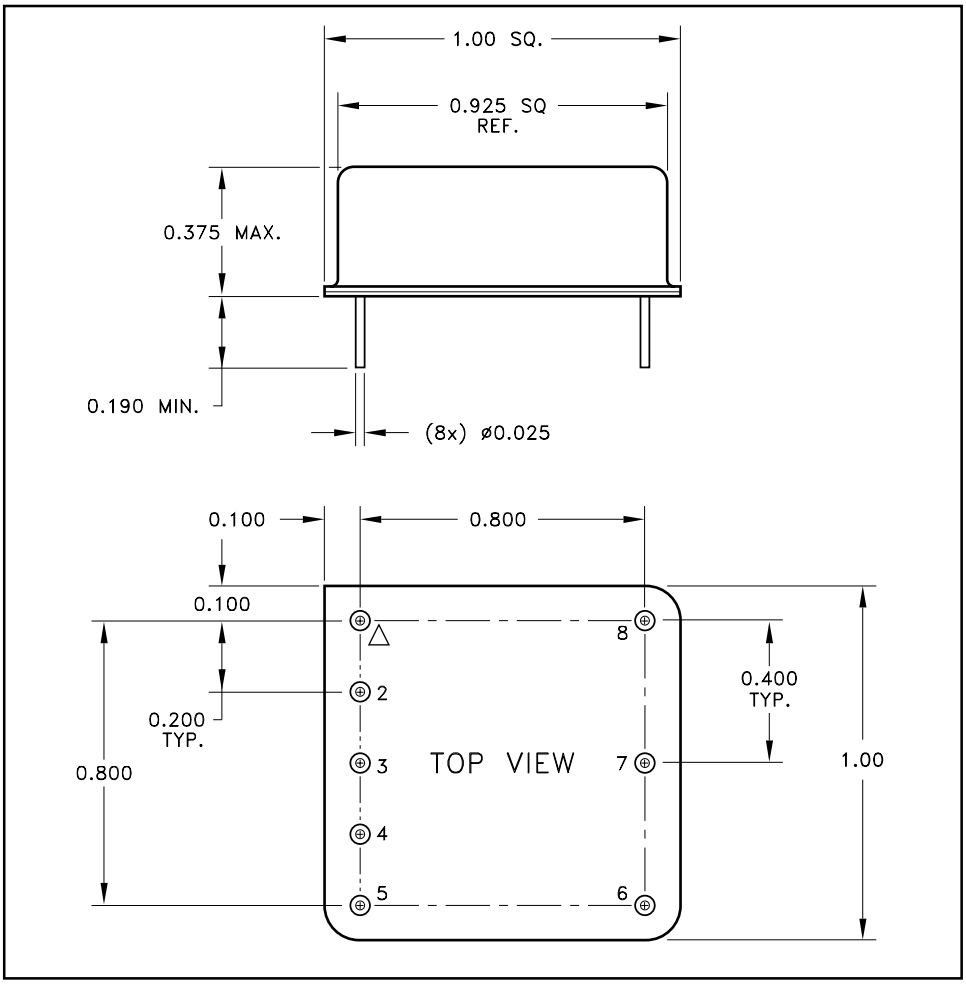

SWITCHING FREQUENCY vs LOAD CURRENT




OUTPUT CURRENT vs TEMPERATURE



## MECHANICAL SPECIFICATIONS




ESD Triangle indicates Pin 1.
NOTE: ALL DIMENSIONS ARE ±0.010 INCHES UNLESS OTHERWISE LABELED.

# *ORDERING INFORMATION*

MSK5030-3.3 B

**SCREENING**
BLANK = INDUSTRIAL; E = EXTENDED RELIABILITY
B = MIL-PRF-38534 CLASS H

**OUTPUT VOLTAGE**
2.5 = +2.5V; 3.3 = +3.3V; 5.0 = +5.0V

**GENERAL PART NUMBER**

The above example is a +3.3V, Military regulator.

M.S. Kennedy Corp.
4707 Dey Road, Liverpool, New York 13088
Phone (315) 701-6751
FAX (315) 701-6752
www.mskennedy.com