Features

- 3.0V to 3.6V Read/Write
- Burst Read Performance
  - ≤100 MHz (RAS Latency = 2, CAS Latency = 6), 10 ns Cycle Time
    t_{SAC} = 7 ns
  - ≤75 MHz (RAS Latency = 2, CAS Latency = 5), 13 ns Cycle Time
    t_{SAC} = 8 ns
  - ≤50 MHz (RAS Latency = 1, CAS Latency = 4), 20 ns Cycle Time
    t_{SAC} = 9 ns
- MRS Cycle with Address Key Programs
  - RAS Latency (1 and 2)
  - CAS Latency (2 ~ 8)
  - Burst Length: 4, 8
  - Burst Type: Sequential and Interleaved
- Word Selectable Organization
  - 16 (Word Mode)/x 32 (Double Word Mode)
- Sector Erase Architecture
  - Eight 256K Word or 128K Double Word (4-Mbit) Sectors
- Independent Asynchronous Boot Block
  - 8K x 16 Bits with Hardware Lockout
- Fast Program Time
  - 3-volt, 100 µs per Word/Double Word Typical
  - 12-volt, 30 µs per Word/Double Word Typical
- Fast Sector Erase Time
  - 2.5 Seconds at 3 Volts
  - 1.6 Seconds at 12 Volts
- Low-power Operation
  - I_{CC} Read = 75 mA Typical
- Input and Output Pin Continuity Test Mode Optimizes Off-board Programming
- Package:
  - 86-pin TSOP Type II with Off-center Parting Line (OCPL) for Improved Reliability
- LVTTL-compatible Inputs and Outputs

Description

The AT49LD3200 or AT49LD3200B SFlash™ is a synchronous, high-bandwidth Flash memory fabricated with Atmel's high-performance CMOS process technology and is organized either as 2,097,152 x 16 bits (word mode) or as 1,048,576 x 32 bits (double word mode), depending on the polarity of the $\overline{\text{WORD}}$ pin (see Pin Function Description Table). Synchronous design allows precise cycle control. I/O transactions are possible on every clock cycle. All operations are synchronized to the rising edge of the system clock. The range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high-bandwidth, high-performance memory system applications.

The AT49LD3200B will automatically activate the Asynchronous Boot Block after power-up, whereas with the AT49LD3200, the Asynchronous Boot Block can be activated through Mode Register Set.

The synchronous DRAM interface allows designers to maximize system performance while eliminating the need to shadow slow asynchronous Flash memory into high-speed RAM.

The 32-megabit SFlash device is designed to sit on the synchronous memory bus and operate alongside SDRAM.

32-megabit (1M x 32 or 2M x 16) High-speed Synchronous Flash Memory

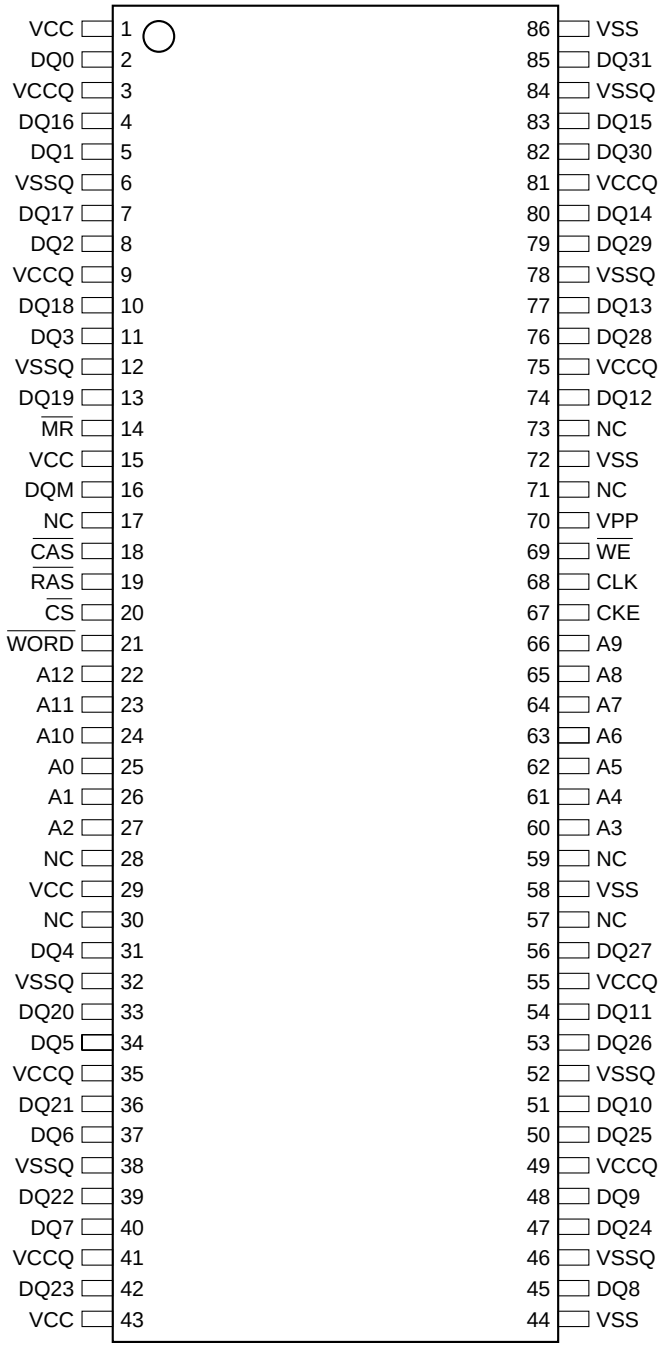
AT49LD3200
AT49LD3200B
SFlash™

Rev. 1940B–FLASH–11/01

To maximize system manufacturing throughput the AT49LD3200(B) features high-speed 12-volt program and erase options. Additionally, stand-alone programming cycle time of individual devices or modules is optimized with Atmel's unique input and output pin continuity test mode.

Pin Configuration

TSOP (Type II)
Top View



Pin Function Description

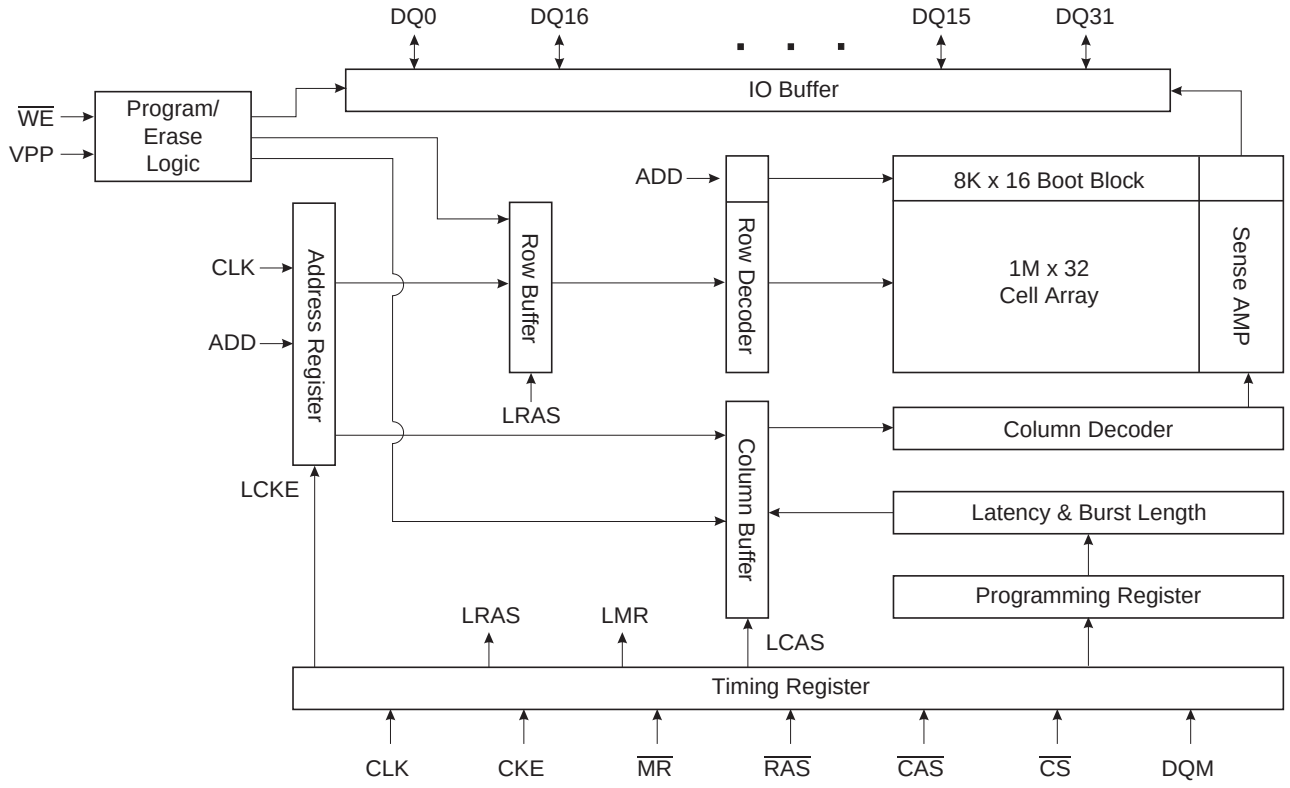
Pin	Name	Input Function
CLK	System Clock	Active on the rising edge to sample all inputs.
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK and CKE.
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power-down in standby mode.
A0 - A12	Address	Row/column addresses are multiplexed on the same pins. Row address: RA_0 ~ RA_{12}, Column address: CA_0 ~ CA_6 (x32), CA_0 ~ CA_7 (x16)
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the rising edge of the CLK with $\overline{RAS}$ low. Enables row access.
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the rising edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{MR}$	Mode Register Set	Enables mode register set with $\overline{MR}$ low. (Simultaneously $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are low).
DQ0 - DQ31	Data Input/Output	Data input for program/erase. Data output for read.
VCC/VSS	Power Supply/Ground	Power and ground for the input buffers and the core logic.
VCCQ/VSSQ	Data Output Power/Ground	Power and ground for the output buffers.
$\overline{WORD}$	x32/x16 Mode Selection	Double word mode/word mode, depending on polarity of $\overline{WORD}$ pin ($\overline{WORD}$ = high, double word mode; $\overline{WORD}$ = low, word mode). Should be set to the desired state during power-up and prior to any device operation.
DQM	Data-out Masking	Masks output operation when a complete burst is not required.
NC	No Connection	Not connected
$\overline{WE}$	Write Enable	Enables the chip to be written.
VPP	Program/Erase Pin Supply	Program/Erase power supply.

Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +4.6V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on V_{PP} with Respect to Ground	-0.6V to +13.5V
Power Dissipation	1 W

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Functional Block Diagram



DC and AC Operating Range

		AT49LD3200(B)-10	AT49LD3200(B)-13	AT49LD3200(B)-20
Operating Temperature (Case)	Commercial	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Industrial	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC}, V_{CCQ} Power Supply		3.0V to 3.6V	3.0V to 3.6V	3.0V to 3.6V

DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{SB1}	V_{CC} Standby Current CMOS	CKE = 0, t_{CC} = Min		20	mA
I_{SB2}	V_{CC} Standby Current TTL	CKE ≤ V_{IL} (Max), t_{CC} = Min		20	mA
I_{SB3}	V_{CC} Active Standby Current	$\overline{CS}$ ≥ V_{IH} (Min), t_{CC} = Min		50	mA
I_{CC}	V_{CC} Active Current	t_{CC} = Min, All Outputs Open		150	mA
I_{IL}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD} + 0.3V Pins not under test = 0V	-10	10	µA
I_{OL}	Output Leakage Current (IO_{OUT} Disabled)	(0V ≤ V_{OUT} ≤ V_{DD} Max) All Outputs in High-Z	-10	10	µA
V_{IH}	Input High Voltage, All Inputs	Note(1)	2.0	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage, All Inputs	Note(2)	-0.3	0.8	V
V_{OH}	Output High Voltage Level (Logic 1)	I_{OH} = -2 mA	2.4		V
V_{OL}	Output Low Voltage Level (Logic 0)	I_{OL} = 2 mA		0.4	V

Notes: 1. V_{IH} (max) = 4.6V for pulse width <10 ns acceptable, pulse width measured at 50% of pulse amplitude.
2. V_{IL} (min) = -1.5V for pulse width <10 ns acceptable, pulse width measured at 50% of pulse amplitude.

AC Operating Test Conditions

T_A = 0 to 70°C, V_{CC} = 3.3V ± 0.3V, unless otherwise noted.

Parameter(1)	Value
Timing Reference Levels of Input/Output Signals	1.4V
Input Signal Levels	V_{IH}/V_{IL} = 2.4V/0.4V
Transition Time (Rise & Fall) of Input Signals	t_r/t_f = 1 ns/1 ns
Output Load	LVTTL

Note: 1. If CLK transition time is longer than 1 ns, timing parameters should be compensated. Add [(t_r + t_f)/2-1] ns for transition time longer than 1 ns. Transition time is measured between V_{IL} (max) and V_{IH} (min).

Figure 1. DC Output Load Circuit

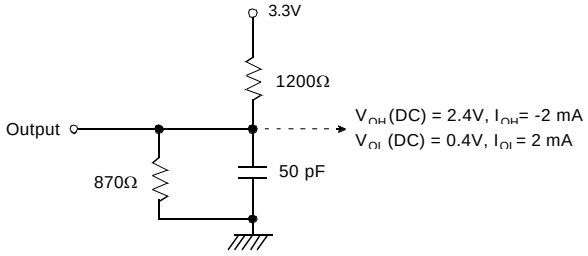
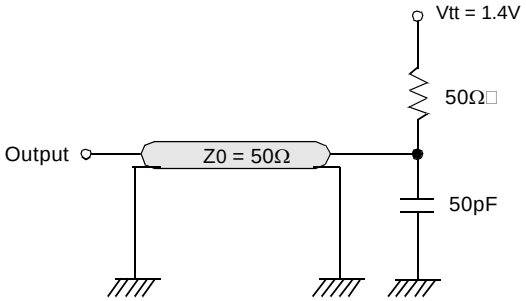


Figure 2. AC Output Load Circuit



Pin Capacitance[1]

f = 1 MHz, T = 25°C

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}[2]	8	12	pF	V_{OUT} = 0V

Notes: 1. This parameter is characterized and is not 100% tested.
2. V_{PP} behaves as an output pin.

AC Read Characteristics

AC operating conditions unless otherwise noted.

Symbol	Parameter	≤100 MHz		≤75 MHz		≤50 MHz		Units
		Min	Max	Min	Max	Min	Max	
t_{CC}	CLK Cycle Time	10		13		20		ns
t_{SAC}	CLK to Valid Output Delay		7		8		9	ns
t_{OH}	Data Output Hold Time	3		4		4		ns
t_{CH}	CLK High Pulse Width	3		4		6.5		ns
t_{CL}	CLK Low Pulse Width	3		4		6.5		ns
t_{RC}	Row-active to Row-active[1]	11		10		9		clks
t_{SS}	Input Setup Time	2		4		4		ns
t_{SH}	Input Hold Time	1		2		2		ns
t_{SLZ}	CLK to Output in Low-Z	0		0		0		ns
t_{SHZ}	CLK to Output in High-Z		7		10		15	ns
t_{T}	Transition Time	0.1	10	0.1	10	0.1	10	ns
t_{VCVC}	Valid CAS Enable to Valid CAS Enable[2]	9		8		7		clks

Notes:
1. These t_{RC} values are for BL = 8. For BL = 4, t_{RC} = 7 CLKs for up to 100 MHz, t_{RC} = 6 CLKs for up to 75 MHz, t_{RC} = 5 CLKs for up to 50 MHz. RAS latency increase means a simultaneous t_{RC} increase in the same number of cycles. (If RAS latency is 3 CLKs, t_{RC} is 12 CLKs for BL = 8.) Refer to page 27 for gapless operation.
2. These t_{VCVC} values are for BL = 8. For BL = 4, t_{VCVC} = 5 CLKs for up to 100 MHz, t_{VCVC} = 4 CLKs for up to 75 MHz, t_{VCVC} = 3 CLKs for up to 50 MHz. Refer to page 27 for gapless operation.

Function Truth Table

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

Abbreviations (RA: Row Address, CA: Column Address, NOP: No Operation Command, DWM: Double Word Mode, WM: Word Mode)

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{MR}$[9]	DQM	Add.	$\overline{WORD}$	VPP	$\overline{WE}$
Register[1]	Mode Register Set		H	X	L	L	L	L	X	Code	X	X	X
Row Active	Row Access & Latch		H	X	L	L	H	H	X	RA	X	X	X
Read	Column Access & Latch		H	X	L	H	L	H	X	CA	X	X	H
Burst Stop			H	X	L	H	H	L	X	X	X	X	X
	(Precharge on Synch. DRAM)		H	X	L	L	H	L	X	X	X	X	X
Power-down and Clock Suspend[2]	Two Standby Mode	Entry	H	L	X	X	X	X	X	X	X	X	X
		Exit	L	H	X	X	X	X	X	X	X	X	X
DQM[3]			H	X	X	X	X	X	V	X	X	X	X
No Operation Command[4]			H	X	H	X	X	X	X	X	X	X	X
			H	X	L	H	H	H	X	X	X	X	X
Organization Control[5]			H	X	L	H	L	H	X	CA	H	X	H
											L		
Program/Erase[6]			H	X	L	H	L	X	X	CA	X	X	L
Fast Program/Erase[6]			H	X	L	H	L	X	X	CA	X	12V	L
Program/Erase Inhibit			H	X	H	X	X	X	X	X	X	X	X
Product Identification[7]	Mode Register Set		H	X	L	L	L	L	X	A_7 = H	X	X	X
	Read		H	X	L	H	L	H	X	L	X	X	H
Continuity Test Mode		Entry	H	X	L	H	L	X	X	CA	X	X	L
		Exit	X	X	X	X	X	X	X	Code[8]	X	X	X

Notes:
1. A_0 ~ A_6: Program keys (@MRS). After power-up, mode register set can be set before issuing other input command. After the Mode Register Set command is completed, no new commands can be issued for 3 CLK Cycles, and $\overline{CS}$ or $\overline{MR}$ state must be defined "H" within 3 CLK cycles. Refer to the Mode Register Control Table.
2. In the case CKE is low, two standby modes are possible. Those are standby mode in power-down, and active standby mode in clock suspend (non-power-down).
   Power-down: CKE = "L" (after no command is issued for 60 µs)
   Clock Suspend: CKE = "L" (at the range of Row Active, Read and Data Out)
3. DQM sampled at rising edge of a CLK makes a high-Z state the data-out state, delayed by 2 CLK cycles.
4. Precharge command on Synch. DRAM can be used for Burst Stop operation during burst read operation only.
5. Mode selection is controlled by the polarity of $\overline{WORD}$ pin, "H" state is DWM, "L" state is WM. $\overline{WORD}$ should be set to the desired state during power-up and prior to any device operation.
6. Data is provided through DQ_0 ~ DQ_{31}. Refer to AC programming and erasing waveforms.
7. DQ_0 ~ DQ_{31} will output Manufacturer Code/Device Code.
8. $A_0 = A_2 = A_{11}$ = "H", $A_1 = A_{10} = A_{12}$ = "L"
9. The user can tie $\overline{MR}$ and $\overline{WE}$ together to simplify the interface of the AT49LD3200(B) onto the standard SDRAM bus.

Asynchronous Boot Block Function Truth Table

Command	CLK[2]	CKE[2]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{MR}$	DQM	Add.	$\overline{WORD}$	VPP	$\overline{WE}$
Read	X	X	L	X	X	X	L	Add	X	X	X
Output Disable	X	X	L	X	X	X	H	X	X	X	X
Program/Erase[1]	↑	H	L	H	L	X	X	Add	X	X	L
Fast Program/Erase[1]	↑	H	L	H	L	X	X	Add	X	12V	L
Program/Erase Inhibit	↑	H	H	X	X	X	X	X	X	X	X

Notes: 1. Program/Erase is performed through the synchronous bus cycle operation after the boot block is activated through either power-up or Mode Register Set.
2. It is recommended to hold CKE Low if CLK is running during asynchronous boot block mode except for synchronous command cycle and MRS operations.

Mode Register Control Table[1]

Register Programmed with MRS

Address	A7	A6	A5	A4	A3	A2	A1	A0
Function	Product ID	RAS Latency	CAS Latency			Burst Type	Burst Length	

Product ID		RAS Latency		CAS Latency				Burst Type		Burst Length		
A7	"Read"	A6	Type	A5	A4	A3	Length	A2	Type	A1	A0	Length
0	Array	0	1	0	0	0	Reserved	0	Sequential	0	0	Reserved
1	ID	1	2	0	0	1	2	1	Interleave	0	1	4
				0	1	0	3			1	0	8
				0	1	1	4			1	1	Boot Block
				1	0	0	5					
				1	0	1	6					
				1	1	0	7					
				1	1	1	8					

Note: 1. After power-up, when the user wants to change Mode Register Set, the user must exit from power-down mode and start Mode Register Set before entering normal operation mode. Reserved modes are not to be used; device function in these modes is not guaranteed.

Addressing Map

$\overline{\text{WORD}}$ = "H": x32 Organization[1]

Function	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}
Row Address	RA_0	RA_1	RA_2	RA_3	RA_4	RA_5	RA_6	RA_7	RA_8	RA_9	RA_{10}	RA_{11}	RA_{12}
Column Address	CA_0	CA_1	CA_2	CA_3	CA_4	CA_5	CA_6[1]	X	X	X	X	X	X

Note: 1. Column Address MSB (at x32 organization) (X = Don't Care)

$\overline{\text{WORD}}$ = "L": x16 Organization[1]

Function	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}
Row Address	RA_0	RA_1	RA_2	RA_3	RA_4	RA_5	RA_6	RA_7	RA_8	RA_9	RA_{10}	RA_{11}	RA_{12}
Column Address	CA_0	CA_1	CA_2	CA_3	CA_4	CA_5	CA_6	CA_7[1]	X	X	X	X	X

Note: 1. Column Address MSB (at x16 organization) (X = Don't Care)

Each Address is Arranged as Follows[1][2]

For X32 operation,

MSB LSB

Address Register	AR_{19}	AR_{18}	AR_{17}	...	AR_8	AR_7	AR_6	...	AR_3	AR_2	AR_1	AR_0
Address	RA_{12}	RA_{11}	RA_{10}	...	RA_1	RA_0	CA_6	...	CA_3	CA_2	CA_1	CA_0

BL = 4

* Initial Address BL = 8

Notes: 1. For X16 operation, when CA_0 is set to Low, data belonging to 0 ~ 15th registers are output to DQ_0 ~ DQ_{15} pins, and when CA_0 is set to High, data belonging to 16 ~ 31th registers are output to DQ_0 ~ DQ_{15} pins.
2. Asynchronous Boot Block uses x16 operation and A_0 ~ A_{12} as address inputs.

Burst Sequence (Burst Length = 4)

Initial Address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

Burst Sequence (Burst Length = 8)

Initial Address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

Device Operations

Clock (CLK)

A square wave signal (CLK) must be applied externally at cycle time t_{CC}. All operations are synchronized to the rising edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high, all inputs are assumed to be in valid state (low or high) for the duration of setup and hold time around the positive edge of the clock for proper functionality and I_{CC} specifications.

Clock Enable (CKE)

The clock enable (CKE) gates the clock into the AT49LD3200(B) and is asserted high during all cycles, except for power-down, standby and clock suspend mode. If CKE goes low synchronously with clock (setup and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen for as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. The AT49LD3200(B) remains in the power-down mode, ignoring other inputs for as long as CKE remains low. The power-down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1 CLK + t_{SS}" before the rising edge of the clock, then the AT49LD3200 becomes active from the same clock edge accepting all the input commands.

NOP and Device Deselect

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{MR}$ are high, the AT49LD3200(B) performs no operation (NOP). NOP does not initiate any new operation. Device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{MR}$

and all the address inputs are ignored. In addition, entering a Mode Register Set command in the middle of a normal operation results in an illegal state in the AT49LD3200(B).

Power-up

The following power-up sequence is recommended.

1. Apply power and start clock. Hold the $\overline{MR}$, CKE and DQM inputs high; all other pins are a NOP condition at the inputs before or along with V_{CC} (and V_{CCQ}) supply.
2. Set $\overline{WORD}$ to the desired state (prior to any device operation).
3. To change the default Mode Register Set values, perform a Mode Register Set cycle to program the RAS latency, CAS latency, burst length and burst type.
4. At the end of three clock cycles after the mode register set cycle, the device is ready for operation.

When the above sequence is used for power-up, all outputs will be in high impedance state. The high impedance of outputs is not guaranteed in any other power-up sequence.

For AT49LD3200B, Asynchronous Boot Block will be selected after power-up.

Mode Selection Control

Mode selection is controlled by the polarity of $\overline{WORD}$ pin. $\overline{WORD}$ should be set to the desired state during power-up and prior to any device operation. The AT49LD3200(B) can be organized as either double word wide (x32) or word wide (x16). The organization is selected via the $\overline{WORD}$ pin. When $\overline{WORD}$ is asserted high (V_{IH}), the double word-wide organization is selected. When $\overline{WORD}$ is asserted low (V_{IL}), the word-wide organization is selected.

Address Decoding

The address bits required to decode one of the available cell locations out of the total depth are multiplexed onto the address select pins and latched by externally applying two commands. The first command, $\overline{RAS}$ asserted low, latches the row address into the device. A second command, $\overline{CAS}$ asserted low, subsequently latches the column address.

Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of AT49LD3200(B). It programs the RAS latency, CAS latency, burst length, burst type, selects product ID Read or activates the Asynchronous Boot Block. For AT49LD3200(B), the default value of the mode register is defined as array read with RAS latency = 2, CAS latency = 5, burst length = 4, sequential burst type. When and if the user wants to change its values, the user must exit from power-down mode and start Mode Register Set before entering normal operation mode. The mode register is reprogrammed by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{MR}$ (the AT49LD3200(B) should be in active mode with CKE already high prior to writing the mode register). The state of address pins A_0 ~ A_7 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{MR}$ going low is the data written in the mode register. Three clock cycles are required to complete the program in the mode register, therefore after a Mode Register Set command is completed, no new commands can be issued for 3 clock cycles and $\overline{CS}$ or $\overline{MR}$ must be high within 3 clock cycles. The mode register is divided into various fields, depending on functionality. The burst length field uses A_0 ~ A_1, burst type uses A_2, CAS latency (read latency from column address) uses A_3 ~ A_5, RAS latency uses A_6 ($\overline{RAS}$ to $\overline{CAS}$ delay), array read or product ID read uses A7. Refer to Mode Register Control Table for specific codes for various burst lengths, burst types, CAS latencies, RAS latencies, and read modes.

Latency

There are latencies between the issuance of a Row Active command and when data is available on the I/O buffers. The $\overline{RAS}$ to $\overline{CAS}$ delay is defined as the RAS latency. The CAS to data out delay is the CAS latency. The CAS and RAS latencies are programmable through the mode register. RAS latencies of 1 and 2, and CAS latencies of 2 through 6 are supported. It is understood that some RAS and CAS latency values are reserved for future use, and are not available in this generation of synchronous Flash. The following are the supported minimum values: RAS latency = 2, and CAS latency = 6 for 100 MHz operation, and RAS latency = 2, and CAS latency = 5 for 66 MHz operation, and RAS latency = 1, and CAS latency = 4 for 50 MHz operation, and RAS latency = 1, and CAS latency = 3 for 33 MHz operation.

DQM Operation

The DQM is used to mask output operations when a complete burst read is not required. It works similar to $\overline{OE}$ during a read operation. The read latency is two cycles from DQM, which means DQM masking occurs two cycles later in the read cycle. DQM operation is synchronous with the clock. The masking occurs for a complete cycle. (Also refer to the DQM timing diagram.)

Burst Read

The Burst Read command is used to access a burst of data on consecutive clock cycles from an active row state. The Burst Read command is issued by asserting low $\overline{CS}$ and $\overline{CAS}$ with $\overline{MR}$ being high on the rising edge of the clock. The first output appears in CAS latency number of clock cycles after the issuance of the Burst Read command. The burst length, burst sequence and latency from the Burst Read command are determined by the mode register, which is already programmed. Burst read can be initiated on any column address of the active row. The output goes into high-impedance at the end of the burst, unless a new burst read is initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read.

Sector Erase

Before a word/double word can be reprogrammed, it must be erased. The erased state of the memory bits is a logical “1”. The AT49LD3200(B) is organized into eight uniform four megabit sectors (SA0 - SA7) that can be individually erased. The Sector Erase command is a synchronous six-bus cycle operation (refer to the Command Definition table and Program Cycle and Erase Cycle waveforms). The erase code consists of 6-byte (DQ8 - DQ31 are Don’t Care inputs for the command) load commands to specific address locations with a specific data pattern. The sector address and 30H data input are latched in the sixth cycle. The sector erase starts at the following rising edge of CLK after the sixth cycle. The erase operation is internally controlled; it will automatically time to completion.

Any commands written to the device during the erase cycle will be ignored. The maximum time needed to erase one sector is t_{EC}.

Word/Double Word Programming

Once a sector is erased, it is programmed (to a logical “0”) on a word-by-word/double-word-by-double-word basis. Programming is accomplished via the internal device command register and is synchronous four-bus cycle operation (refer to the Command Definition table and Program Cycle and Erase Cycle waveforms). The programming operation starts at the following rising edge of CLK after the fourth cycle. The device will automatically generate the required internal program pulses.

Any commands written to the device during the embedded programming cycle will be ignored. Please note that a data “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s. Programming is completed after the specified t_{PGM} cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

Product Identification

The product identification mode identifies the device and manufacturer as Atmel. This mode can be used by an on-board controller or external programmer to identify the correct programming algorithm for the Atmel product.

$\overline{\text{DATA}}$ Polling

The AT49LD3200(B) features $\overline{\text{DATA}}$ polling to indicate the end of a program or sector erase cycle. $\overline{\text{DATA}}$ polling may begin at any time during the program or sector erase cycle.

During a program cycle, an attempted read of the last word/double word loaded will result in the complement of the loaded data in DQ7. Once the program cycle has completed, true valid data can be read on all outputs and the next cycle may begin.

During a sector erase operation, an attempt to read the device will give a “0” on DQ7. Once the sector erase cycle has completed, logical “1” data can be read on all outputs from the device.

Hardware Data Protection

Hardware features protect against inadvertent programming or erasure to the AT49LD3200(B) in the following way: V_{CC} sense: if V_{CC} is below 2.3V (typical), the program or erase function is inhibited; but if V_{CC} dips below 2.3V during program or erase cycle, the respective function will be interrupted and the data at the location being programmed may be corrupted.

Continuity Test Mode

The AT49LD3200(B) has built-in circuitries to make input and output pin continuity check simple and easy. This mode can be activated via the internal device command register and is a synchronous five-bus cycle operation (refer to the Command Definition Table and Continuity Test Mode Entry Waveforms). After the bus cycle operation, keep DQM high (V_{IH}) and allow 5 µsec for circuit setup time or until data is no longer asserted at DQ0 - DQ7, whichever takes longer. This will keep DQ0 - DQ7 from contention since data is asserted at DQ0 - DQ7 during the mode entry sequence. Then DQM can be asserted low (V_{IL}) to enable DQ0 - DQ7 for test. Once in this asynchronous mode, input pins are virtually tied to output pins internally forming input - output pin pairs. The output pin of the pair will follow the logic state of the input pin of the pair (refer to the Input - Output Pin Pairs table). To exit the mode, A_0, A_2 and A_{II} are asserted high (V_{IH}) and A_1, A_{10} and A_{12} are asserted low (V_{IL}), allow 5 µsec for circuit recovery time before returning the device for normal operation.

Input - Output Pin Pairs

Input	Output
$\overline{MR}$	DQ0, DQ16
$\overline{RAS}$	DQ1, DQ17
$\overline{CAS}$	DQ2
DQM	DQ18
$\overline{CS}$	DQ3
$\overline{WORD}$	DQ19
A12	DQ4
A11	DQ20
A10	DQ5
A0	DQ21
A1	DQ6, DQ22
A2	DQ7, DQ23
A3	DQ8, DQ24
A4	DQ9, DQ25
A5	DQ10
A6	DQ26
A7	DQ11
A8	DQ27
A9	DQ12
CKE	DQ28
CLK	DQ13, DQ29
$\overline{WE}$	DQ14, DQ30
VPP	DQ15, DQ31

Asynchronous Boot Block

The AT49LD3200B will automatically activate the Asynchronous Boot Block after power-up and the AT49LD3200 can activate the Asynchronous Boot Block through the Mode Register Set. The size of the boot block is 8K x 16 bits with addresses A_0 ~ A_{12} and outputs DQ_0 ~ DQ_{15}. The contents of the boot block are accessed asynchronously, meaning the data at outputs will change according to the address inputs after t_{ACC}, without any external clocking signals.

Programs and erases are performed using the synchronous bus cycle operation (refer to Command Definitions table and Program Cycle and Erase Cycle waveforms) after the boot block is activated either through power-up or Mode Register Set. Programming of the boot block is set up for x16 mode.

This Asynchronous Boot Block has a lockout feature that prevents programming or erasing of data in this boot block once the feature has been enabled. This feature does not have to be activated; the boot block's usage as a protected region is optional to the user. Once this feature is enabled, the data in the boot block can no longer be erased or programmed when input levels of 3.6V or less are used. To activate the lockout feature,

Boot Block Lockout command, which is a synchronous five-bus cycle operation, must be performed (refer to Command Definitions table and Program Cycle Waveforms).

A software method is available to determine if programming or erasing of the boot block is locked out. Issue Boot Block Lockout Verify command and observe DQ_0 ~ DQ_7. If the data show 00H/02H, the boot block can be programmed or erased; if the data show 01H/03H, the lockout feature has been enabled and the boot block cannot be programmed or erased. The Boot Block Lockout Verify Exit command should be used to return to standard operation (refer to Command Definition table and Boot Block Lockout Verify Waveforms).

The user can override the boot block lockout by taking the $\overline{MR}$ pin to 12 volts after the boot block is activated. When the $\overline{MR}$ pin is brought back to TTL levels, the boot block lockout feature is again active.

Command Definition in Hex[1]

Command Sequence	Bus Cycles	1st Bus Cycle			2nd Bus Cycle			3rd Bus Cycle			4th Bus Cycle			5th Bus Cycle			6th Bus Cycle		
		RA	CA	Data	RA	CA	Data	RA	CA	Data	RA	CA	Data	RA	CA	Data	RA	CA	Data
Word/ Double Word Program	4	AA	55	AA	55	2A	55	AA	55	A0	RA	CA	D_{IN}						
Sector Erase	6	AA	55	AA	55	2A	55	AA	55	80	AA	55	AA	55	2A	55	SA[2]	X	30
Continuity Test Mode Entry	5	AA	55	AA	55	2A	55	AA	55	80	AA	55	AA	AA	55	70			
Boot Block Lockout	5	AA	55	AA	55	2A	55	AA	55	80	AA	55	AA	AA	55	40			
Boot Block Lockout Verify	5	AA	55	AA	55	2A	55	AA	55	80	AA	55	AA	AA	55	90			
Boot Block Lockout Verify Exit	5	AA	55	AA	55	2A	55	AA	55	80	AA	55	AA	AA	55	F0			

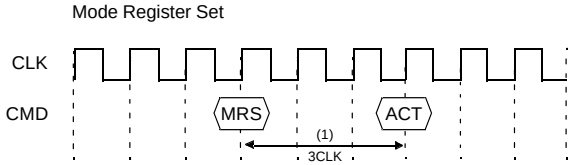
Notes:
1. The DATA FORMAT in each bus cycle is as follows: DQ31 - DQ8 (Don't Care); DQ7 - DQ0 (Hex).
2. SA = Sector Addresses: Any word/double word address within a sector can be used to designate the sector address. See Sector Address Mapping table below.
3. Allow minimum 200 ns after Boot Block Lockout Verify command and before Read.
4. Allow minimum 10 µs after Boot Block Lockout Verify Exit command for the device to return to standard operation.

Sector Address Mapping

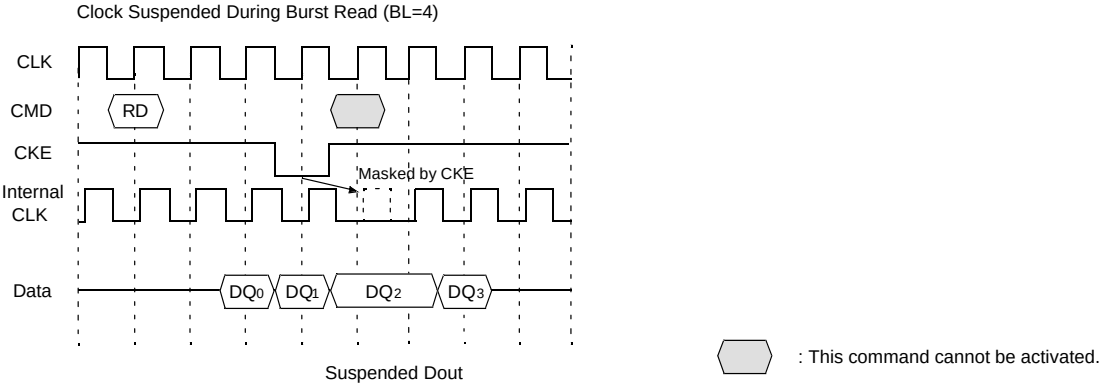
Sector	Size (Word/Double Word)	x16 Address Range		x32 Address Range	
		CA_{7-0}	RA_{12-0}	CA_{6-0}	RA_{12-0}
SA0	256K/128K	X	00XX 03XX	X	00XX 03XX
SA1	256K/128K	X	04XX 07XX	X	04XX 07XX
SA2	256K/128K	X	08XX 0BXX	X	08XX 0BXX
SA3	256K/128K	X	0CXX 0FXX	X	0CXX 0FXX
SA4	256K/128K	X	10XX 13XX	X	10XX 13XX
SA5	256K/128K	X	14XX 17XX	X	14XX 17XX
SA6	256K/128K	X	18XX 1BXX	X	18XX 1BXX
SA7	256K/128K	X	1CXX 1FXX	X	1CXX 1FXX

Basic Feature and Function Descriptions

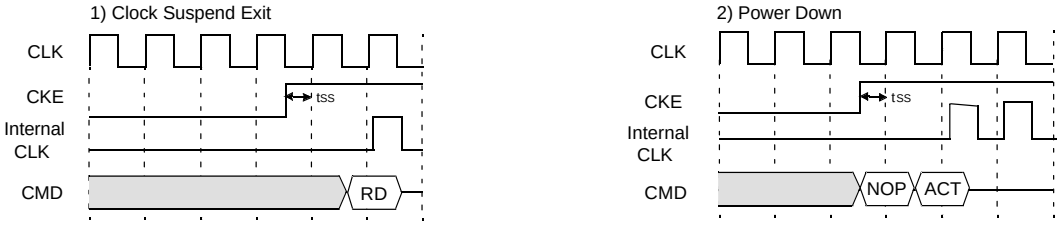
MRS



Clock Suspend



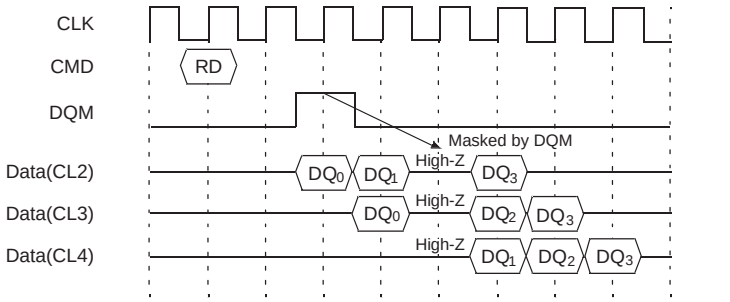
Clock Suspend Exit and Power-down Exit



Note: After Mode Register Set command is completed, no new commands can be issued for 3 clock cycles, and $\overline{MR}$ or $\overline{CS}$ should be fixed “H” within a minimum of 3 clock cycles.

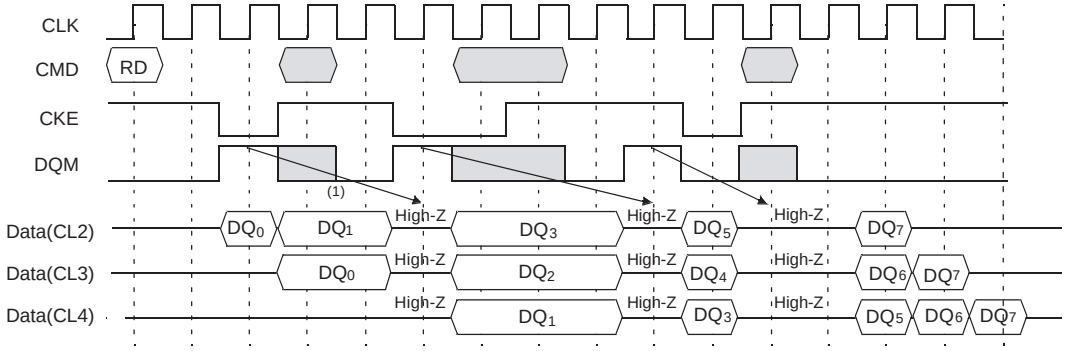
DQM Operation

1) Read Mask (BL=4)



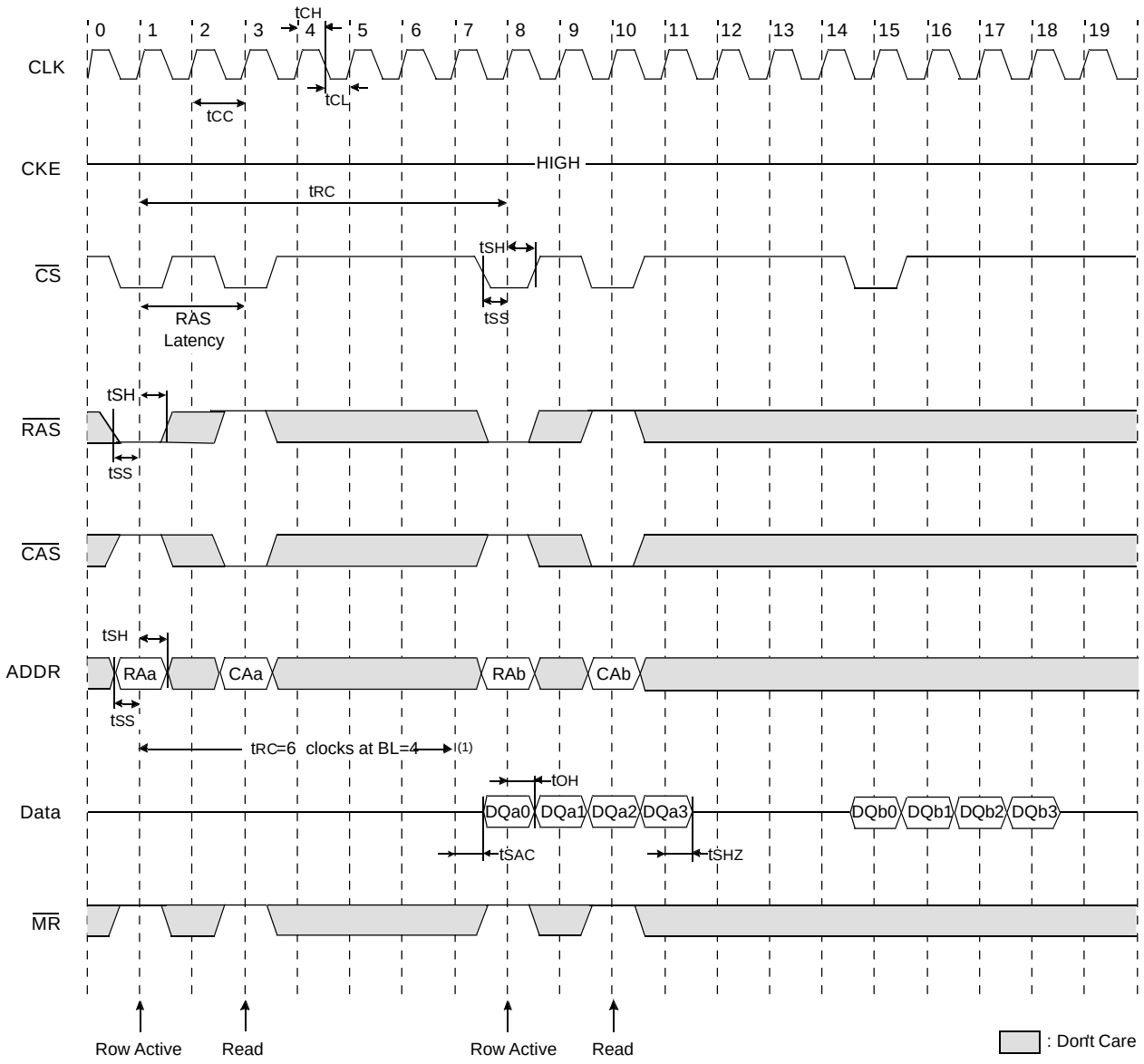
DQM to Data-out Mask = 2CLKs

2) DQM with Clock Suspended (BL=8)



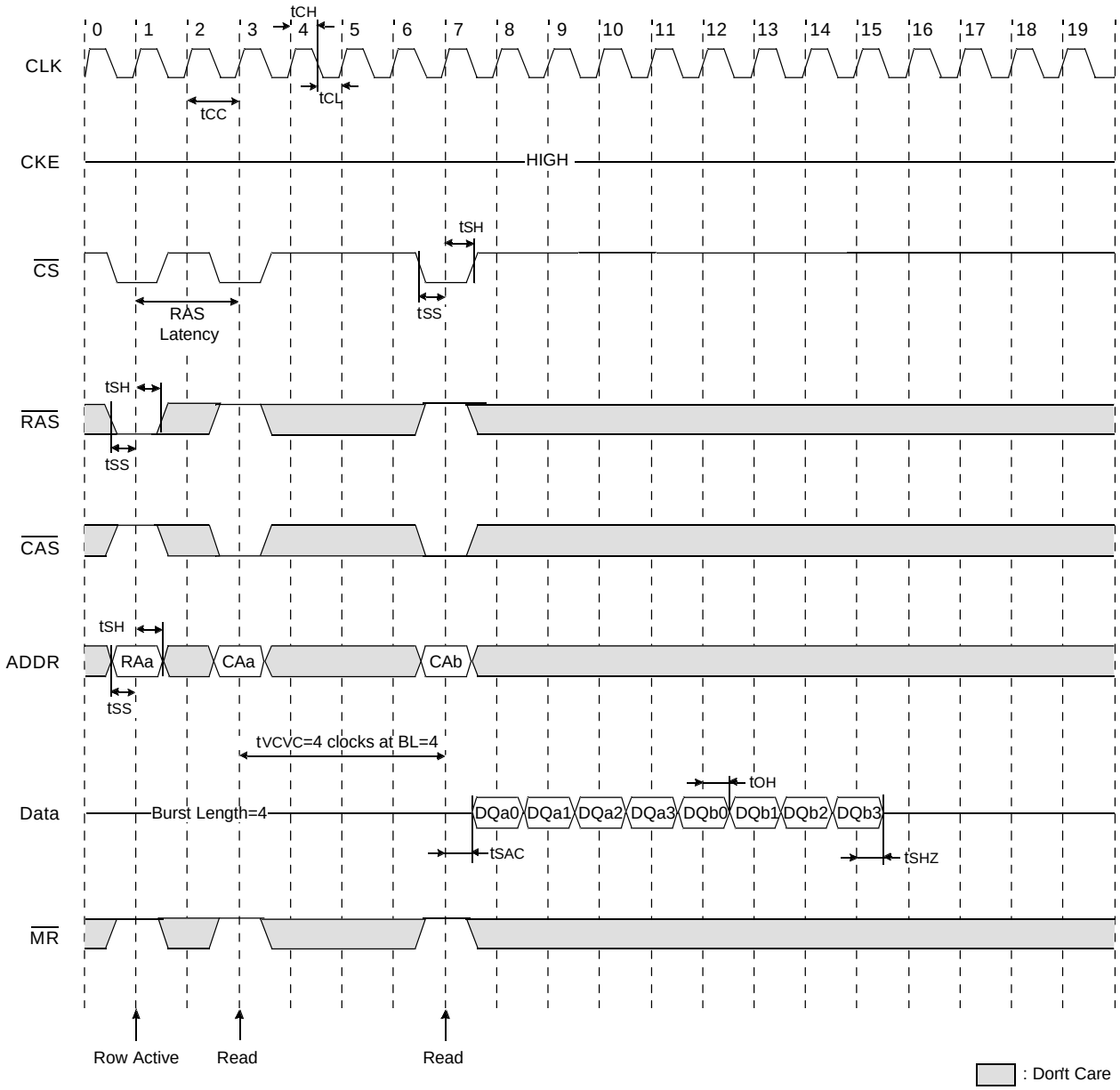
Note: DQM makes data out high-Z after 2 CLKs, which should be masked by CKE “L”.

Read Cycle I: Normal @RAS Latency = 2, CAS Latency = 5, Burst Length = 4



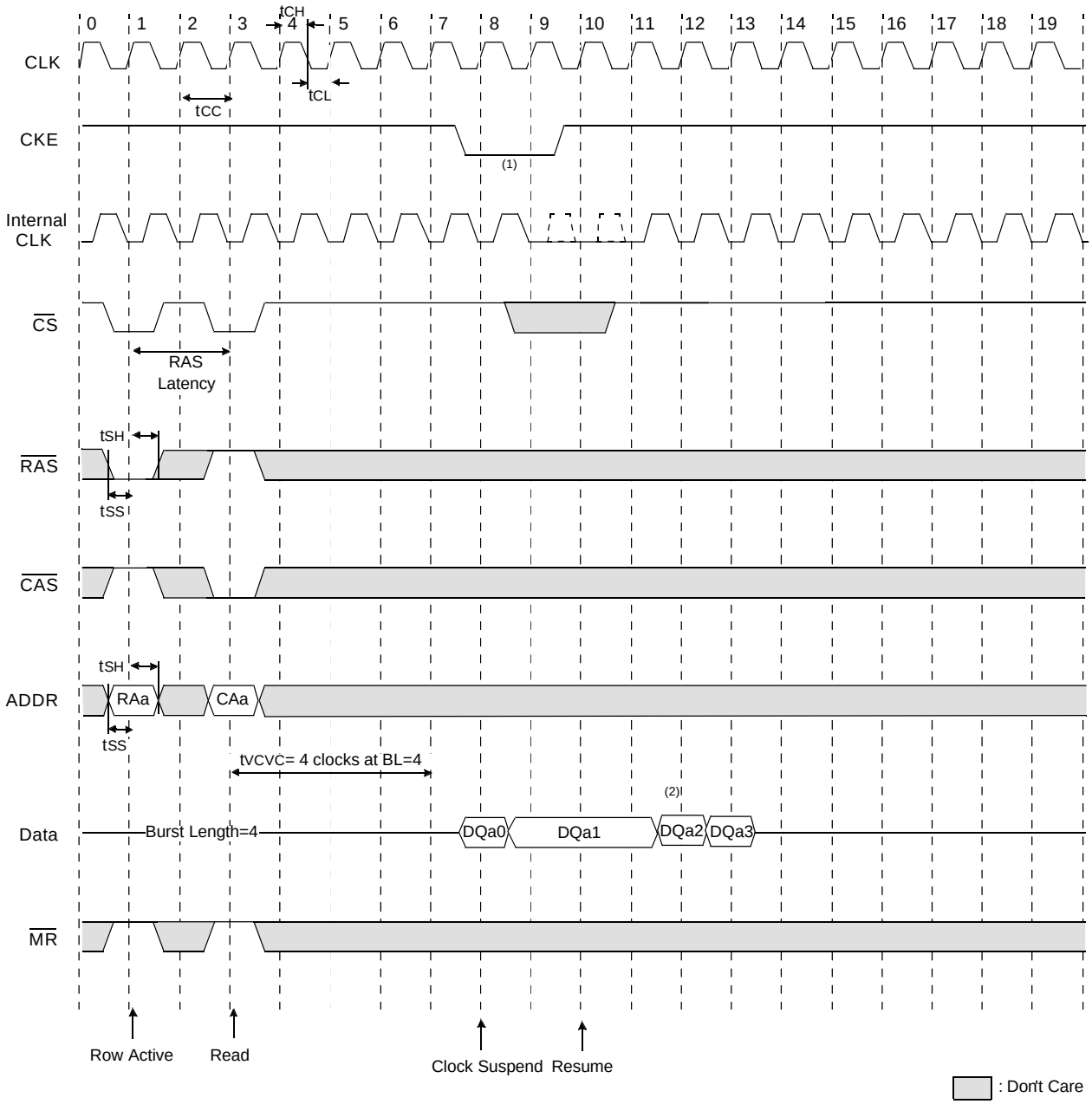
Note: When the burst length is 4 at 66 MHz, t_{RC} is equal to 6 clock cycles.

Read Cycle II: Consecutive Column Access @RAS Latency = 2, CAS Latency = 5, Burst Length = 4



Note: When column access is initiated beyond t_{VCVC}, at BL = 4, CA_a access read is completed, CA_b access read begins.

Read Cycle III: Clock Suspend @RAS Latency = 2, CAS Latency = 5, Burst Length = 4

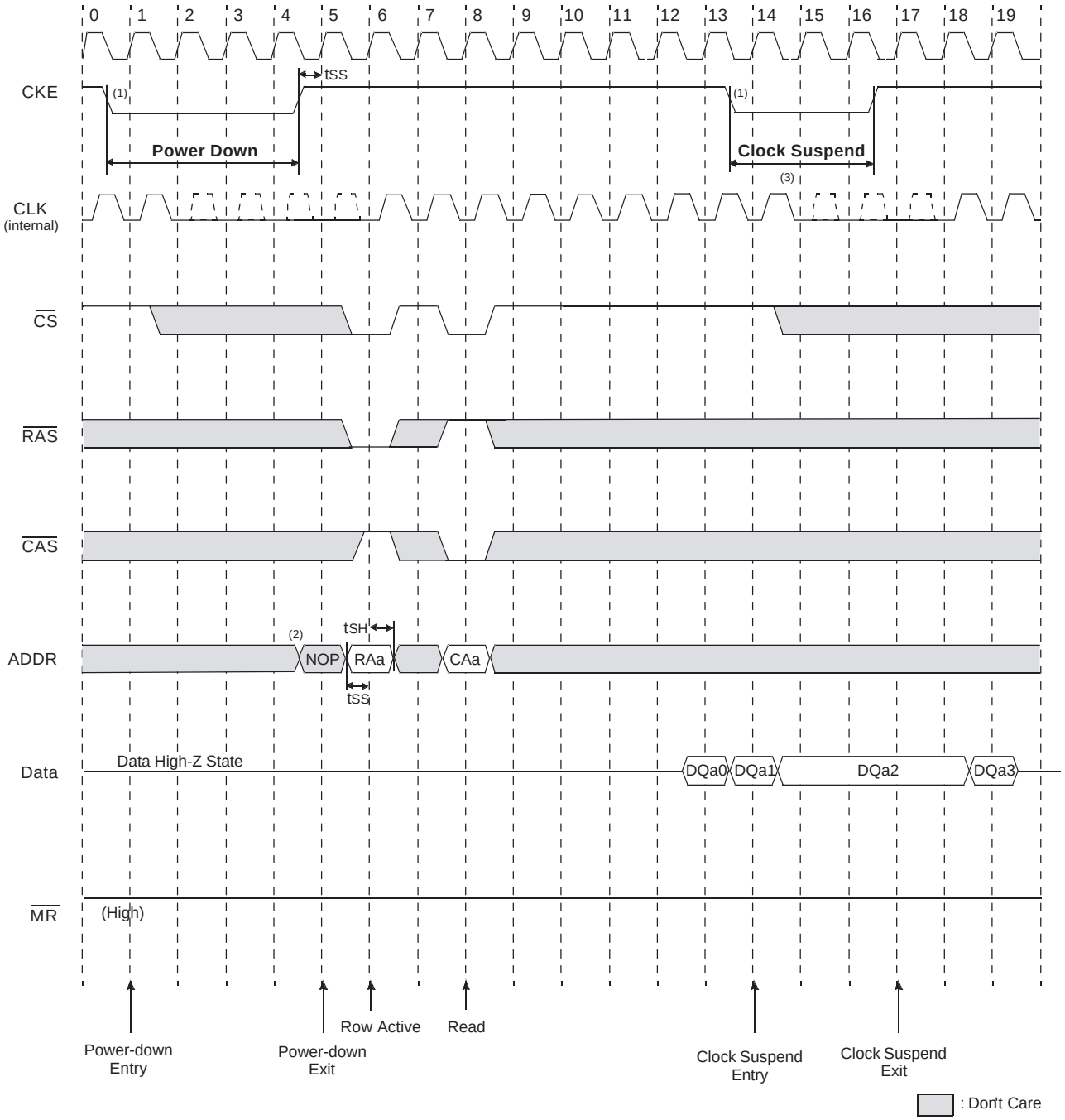


Notes: 1. From next clock after CKE goes low, clock suspension begins.
2. For clock suspension, data output state is held and maintained.

Read Interrupted by Precharge Command and Burst Read Stop Cycle @Burst Length = 8

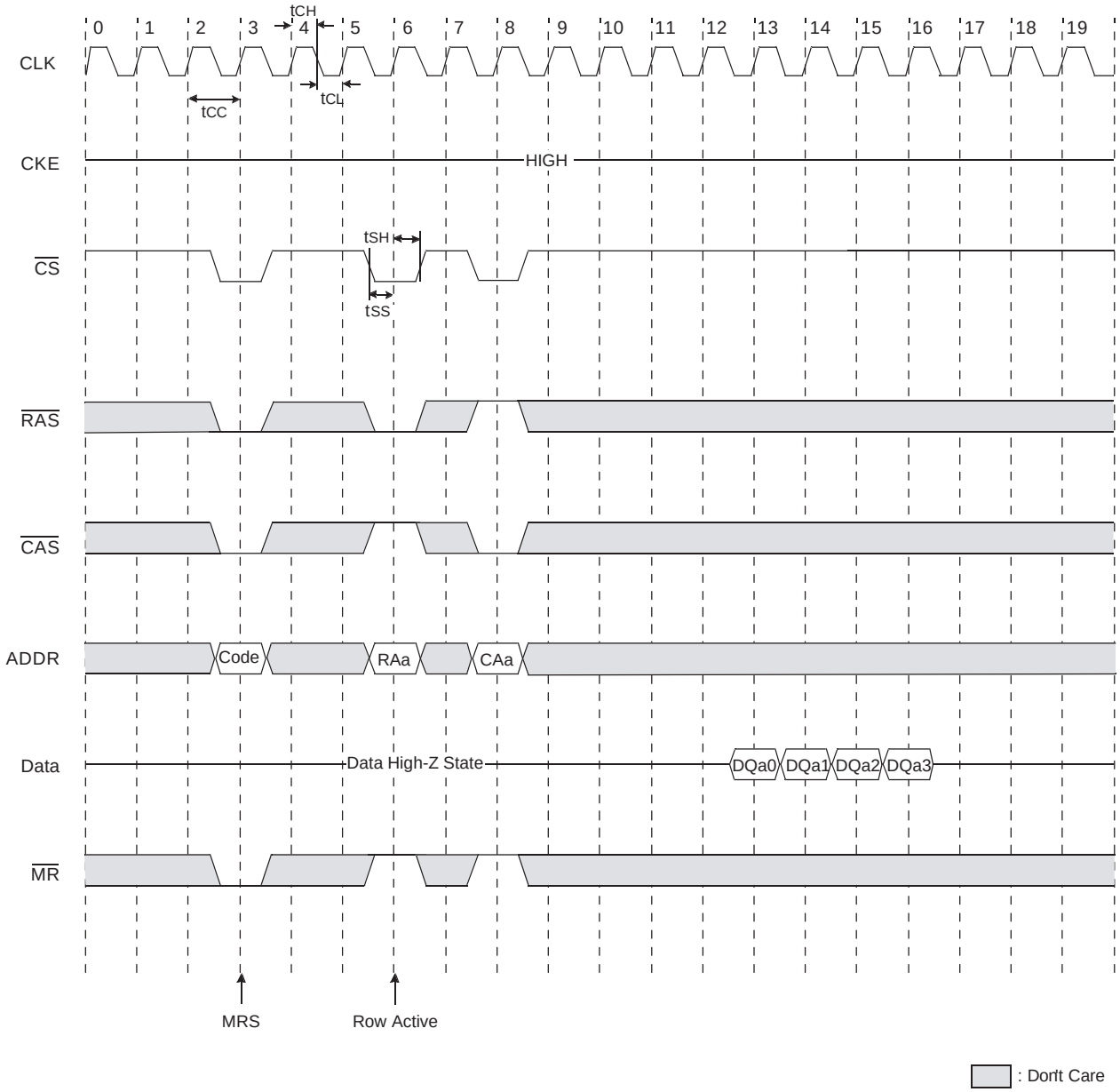
Notes: 1. The Burst Stop command is valid at every page burst length. The data bus goes to high-Z after the CAS latency from the Burst Stop command is issued.
2. The interval between Read command (column address presented) and Burst Stop command is 1 cycle (min).

Power-down and Clock Suspend Cycle: @RAS Latency = 2, CAS Latency = 5, Burst Length = 4



Notes:
1. From next clock after CKE goes low, clock suspend and power-down begins.
2. After power-down exit, NOP should be issued and new command can be issued after 1 clock.
3. Clock suspend is in active standby mode.

Mode Register Set: @RAS Latency = 2, CAS Latency = 5, Burst Length = 4



Notes: 1. After the Mode Register Set is completed, no new commands can be issued for 3 CLK cycles.

2. After power-up, necessarily Mode Register Set should be completed at least one time and $\overline{CS}$ or $\overline{MR}$ must be fixed “H” within 3 clock cycles, and when user wants to change Mode Register Set, user must exit from power-down mode and start Mode Register Set before chip enters normal operation mode.

Detailed Functional Truth Table

Current State	Input Signal						Next State Operation
	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{MR}$	Add.	
After Power-up[1]	L	X	X	X	X	X	Power-down
	H	L	L	H	H	RA	Row Active; latch RA
	H	L	L	L	L	Code	Mode Register Set
Row Active	H	L	L	H	H	RA	If consecutive row access is issued within t_{RC} (min.) without $\overline{CAS}$ enabling, only the final RA is valid.
	H	L	H	L	H	CA	Begin READ; latch CA
	H	L	L	L	L	Code	Illegal[1]
	L	X	X	X	X	X	Clock Suspend
READ	H	L	L	H	H	RA	Row Access in Read State, within the t_{RC}, previous read is ignored and new row is activated. Beyond the t_{RC}, previous read is completed and new read begins.
	H	L	H	L	H	CA	Consecutive Column Access, within the t_{VCVC}, only the final CA is valid and the previous burst read is ignored. Beyond the t_{VCVC}, the previous read is completed and new read begins.
	H	L	L	H	L	X	NOP (after Burst Read)/Read Interrupt
	H	L	H	H	L	X	NOP (after Burst Read)/Read Interrupt
	H	L	L	L	L	Code	Illegal[1]
	L	X	X	X	X	X	Clock Suspend/Power-down
Any State	L	L	L	L	H	X	Low Power Consumption Mode
Any State	H	L	H	H	H	X	NOP
Any State	H	L	L	L	H	X	Illegal
	H	L	H	L	L	CA	Illegal

Note: 1. After the power-up, when user wants to change MR Set, user must exit from power-down mode and start MR Set before chip enters normal operation mode.

Technical Notes

Frequency vs. AC Parameter Relationship Table[1]

≤100 MHz

Burst Length	RAS Latency	CAS Latency	t_{RC} (min)	t_{VCVC} (min)
4	2	6	7	5[2]
		7	8	6
8	2	6	11	9[2]
		7	12	10

≤75 MHz

Burst Length	RAS Latency	CAS Latency	t_{RC} (min)	t_{VCVC} (min)
4	2	5	6	4[2]
		6	7	5
8	2	5	10	8[2]
		6	11	9

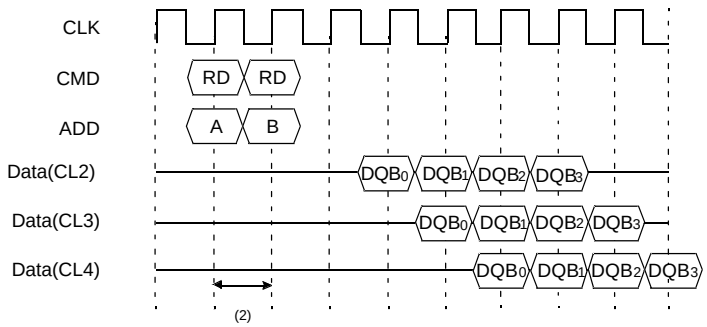
≤50 MHz

Burst Length	RAS Latency	CAS Latency	t_{RC} (min)	t_{VCVC} (min)
4	1	4	4[2]	3/4[2]
		5	5	4[2]
		6	6	5
8	1	4	8[2]	7/8[2]
		5	9	8[2]
		6	10	9

Notes:
1. Above tables are not specifications values, but rather the actual number of clock cycles. There are no gapless operations for CAS latency 7 and 8.
2. Minimum clocks for gapless operation.
3. t_{RC} (max) = t_{VCVC} (max) = 50 µs. If t_{RC} (max) or t_{VCVC} (max) has been reached, a new “ACTIVE” command is necessary for new access.

$\overline{\text{CAS}}$ Interrupt

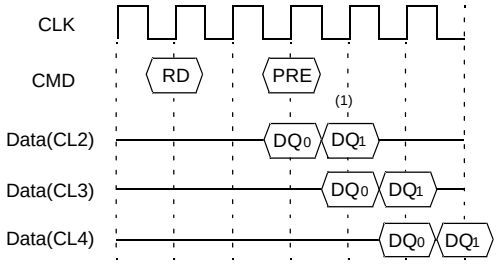
Read interrupted by Read (BL=4) (1)

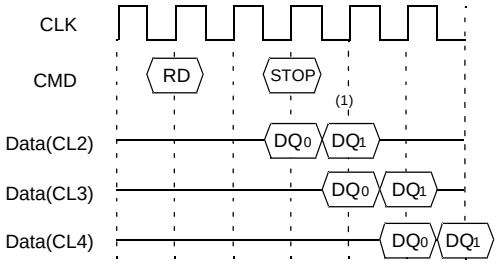


Notes: 1. By "Interrupt", it is meant to stop Burst Read by external command before the end of burst. By "$\overline{\text{CAS}}$ Interrupt", to stop Burst Read by $\overline{\text{CAS}}$ access.
2. $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay (=1 CLK).

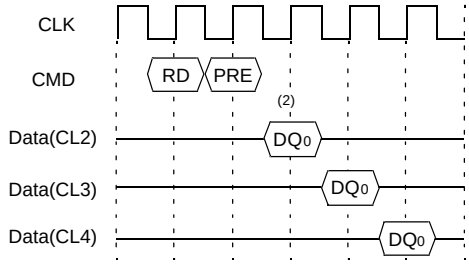
Read Interrupt Operation by Issuing the Precharge of Burst Stop Command

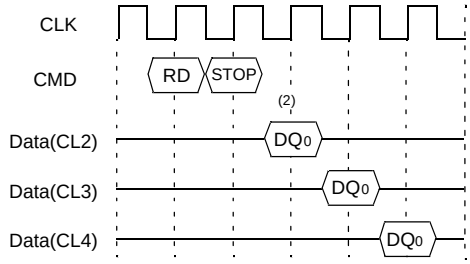
CASE I) Issued read Interrupt command during burst read operation period.





CASE II) Issued read Interrupt command between read command and data out.

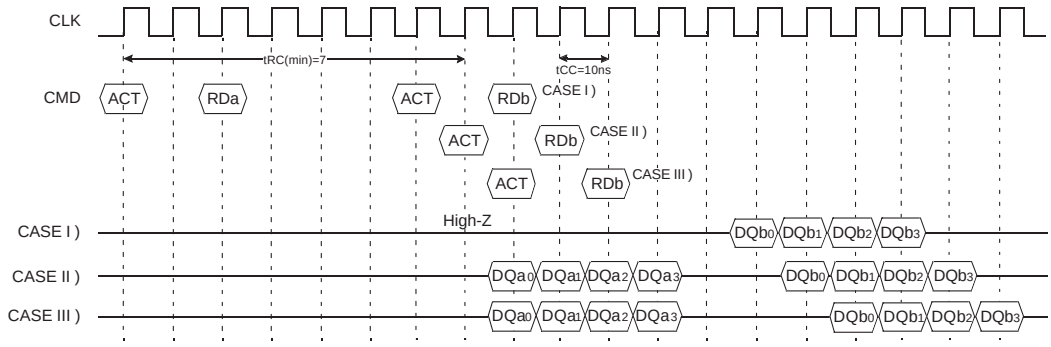




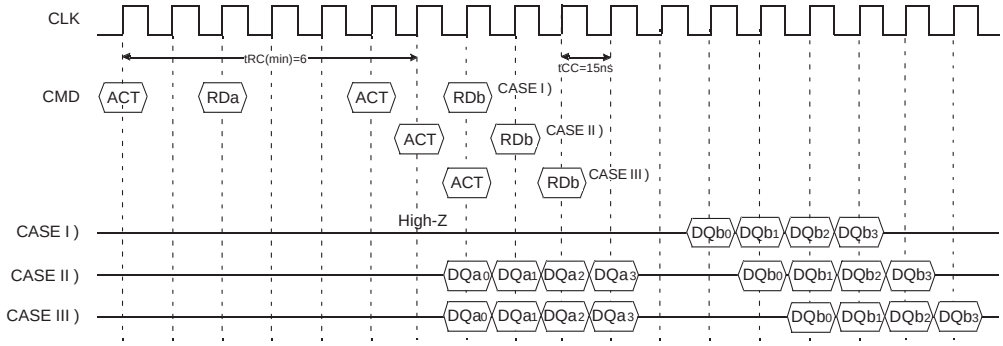
Notes: 1. The data bus goes to high-Z after CAS latency from the Burst Stop (or precharge) command.
2. Valid output data will last up to CL-1 clock cycle from PRE command.

Read Cycle Depending on t_{RC}

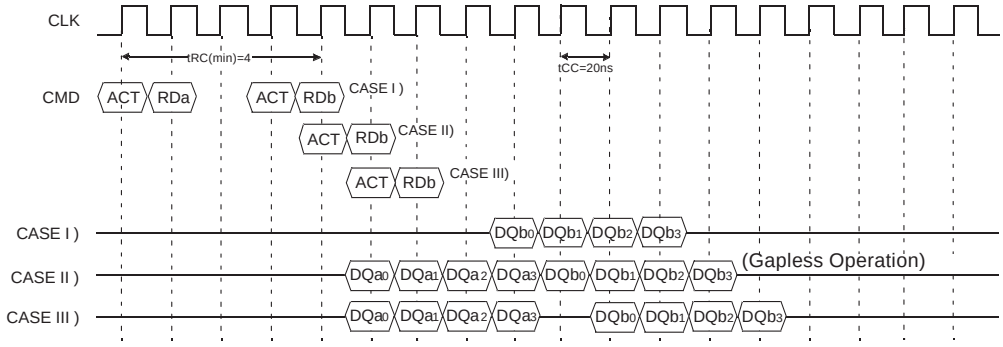
@RL = 2, CL = 6, BL = 4; 100 MHz



@RL = 2, CL = 5, BL = 4; 75 MHz

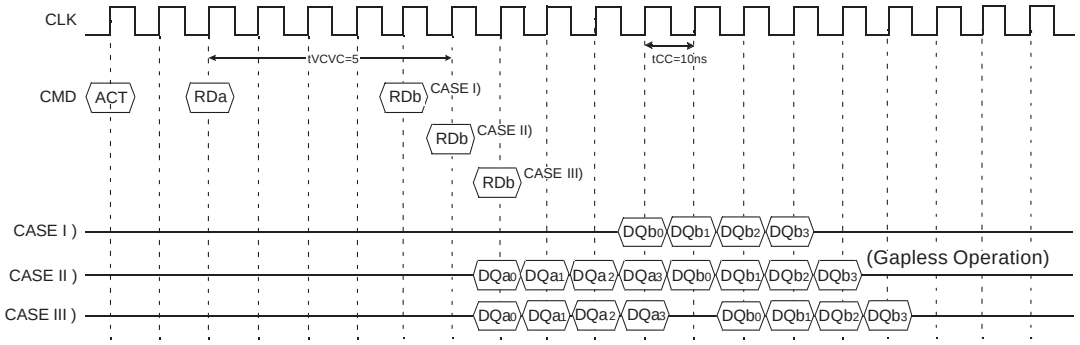


@RL = 1, CL = 4, BL = 4; 50 MHz

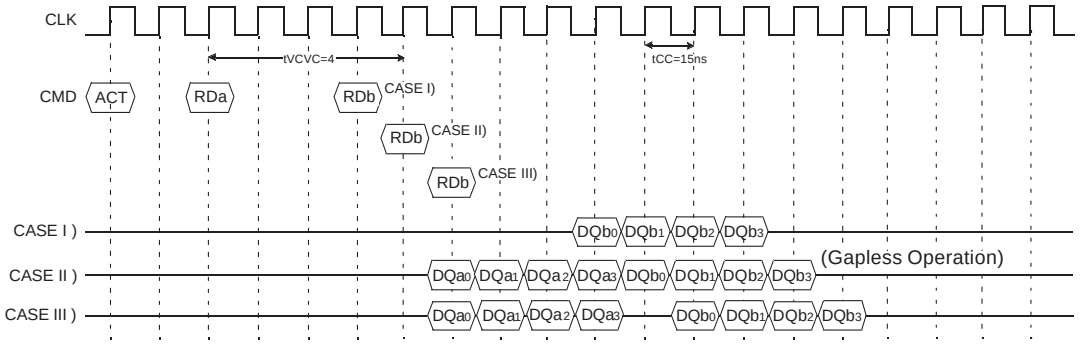


Read Cycle Depending on t_{VCVC}

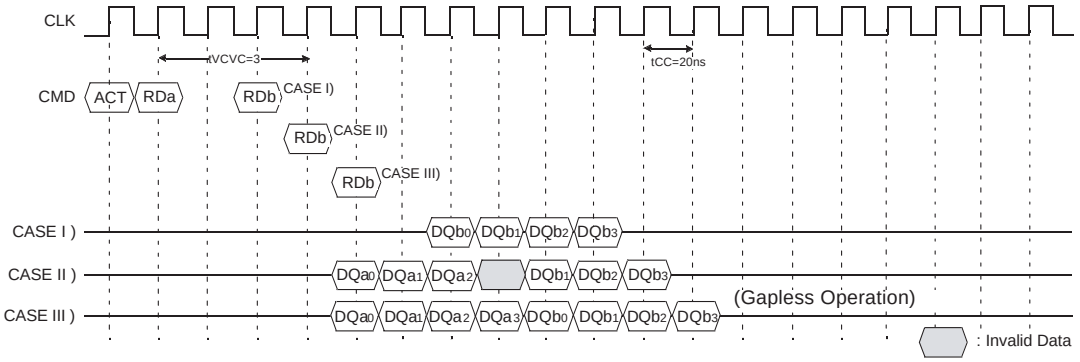
@RL = 2, CL = 6, BL = 4; 100 MHz



@RL = 2, CL = 5, BL = 4; 75 MHz



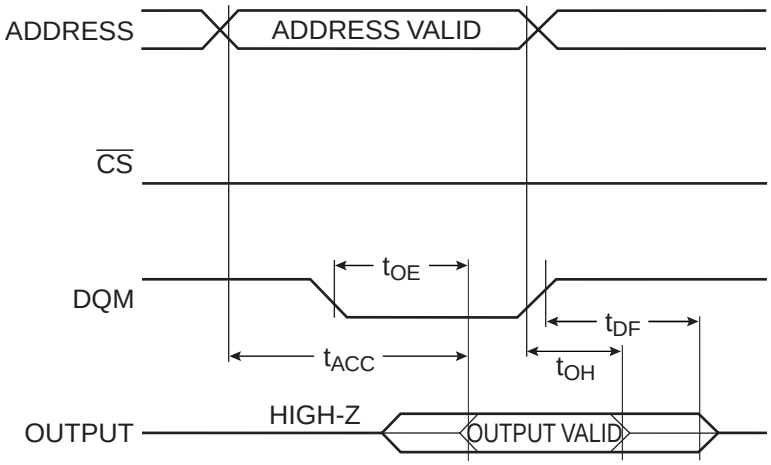
@RL = 1, CL = 4, BL = 4; 50 MHz



AC Characteristics for Boot Block Read Operation

Symbol	Parameter	Condition	Min	Max	Units
t_{ACC}	Address to Output Delay	$\overline{CS}$ = DQM = V_{IL}		170	ns
t_{OE}	DQM to Output Delay	$\overline{CS}$ = V_{IL}		60	ns
t_{DF}	DQM High to Output Float			40	ns
t_{OH}	Output Hold from Address		0		ns

AC Waveforms for Boot Block Read Operation



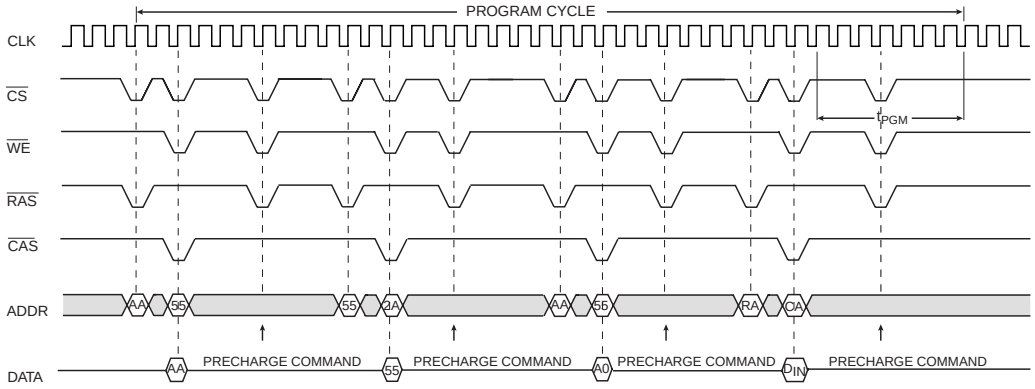
3-volt Program and Erase Cycle Characteristics

Symbol	Parameter	Typ	Max	Units
t_{PGM}	Word/Double Word Programming Time	50	600	µs
t_{EC}	Sector/Boot Block Erase Cycle Time		2.0/300	seconds/ms
t_{BBL}	Boot Block Lockout Enable Time		10	ms
I_{CC2}	V_{CC} Current during Program and Erase Cycle		150	mA

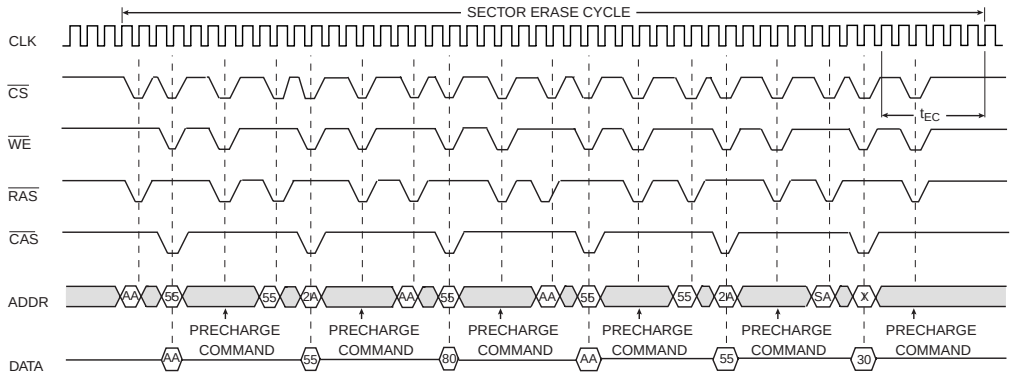
High-speed 12-volt Program and Erase Cycle Characteristics

Symbol	Parameter	Typ	Max	Units
t_{PGM}	Word/Double Word Programming Time	15	200	µs
t_{EC}	Sector/Boot Block Erase Cycle Time		1.2/200	seconds/ms
I_{CC3}	V_{CC} Current During Program and Erase Cycle		75	mA
I_{PP3}	V_{PP} Current During Program and Erase Cycle		75	mA

Program Cycle Waveforms

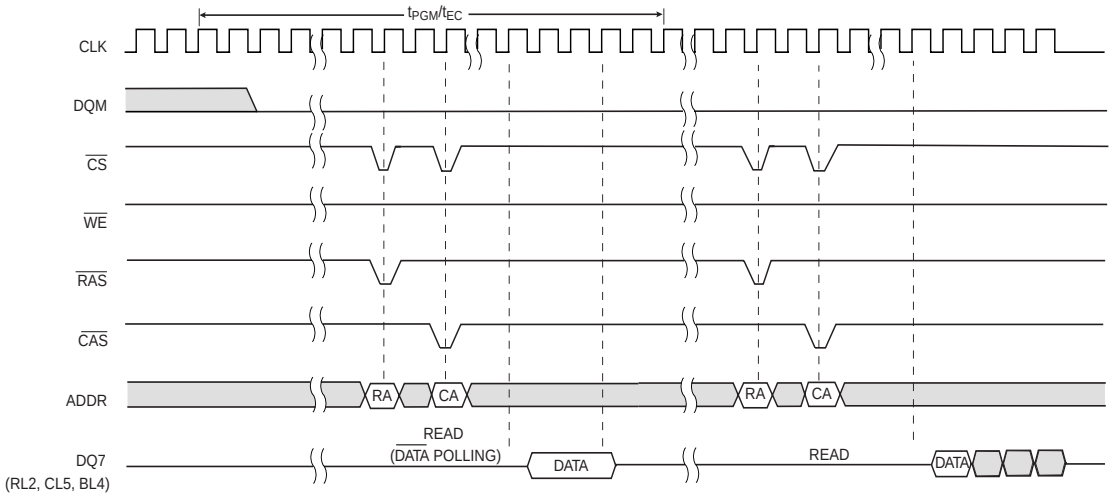


Sector Erase Cycle Waveforms



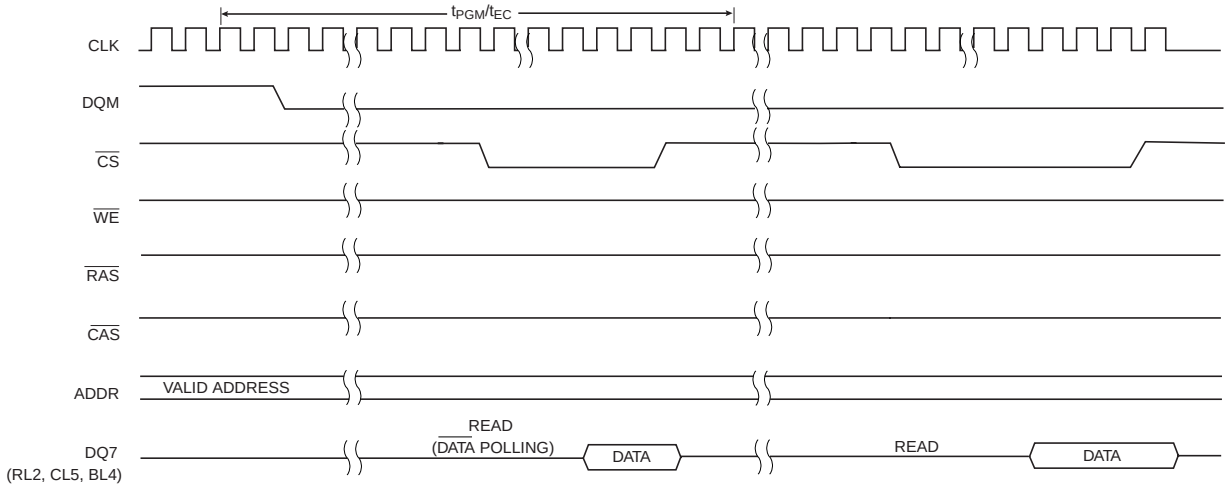
Notes:
1. The Precharge command is optional. A Precharge command ($\overline{CS}$, $\overline{RAS}$, $\overline{MR}$ = L) during Program and Sector Erase cycles ($\overline{WE}$ = L) will be treated as NOP, and the number of clock cycles between the bus cycle and the Precharge command or vice versa should be “Don’t Care”.
2. For boot block programming, RA = CA = A_0 ~ A_{12} and be held valid throughout program cycle; DQM should be held “H” during the four-bus cycle command operation.
3. For boot block erasing, SA = X; DQM should be held “H” during the six-bus cycle command operation.

$\overline{\text{Data}}$ Polling Waveforms



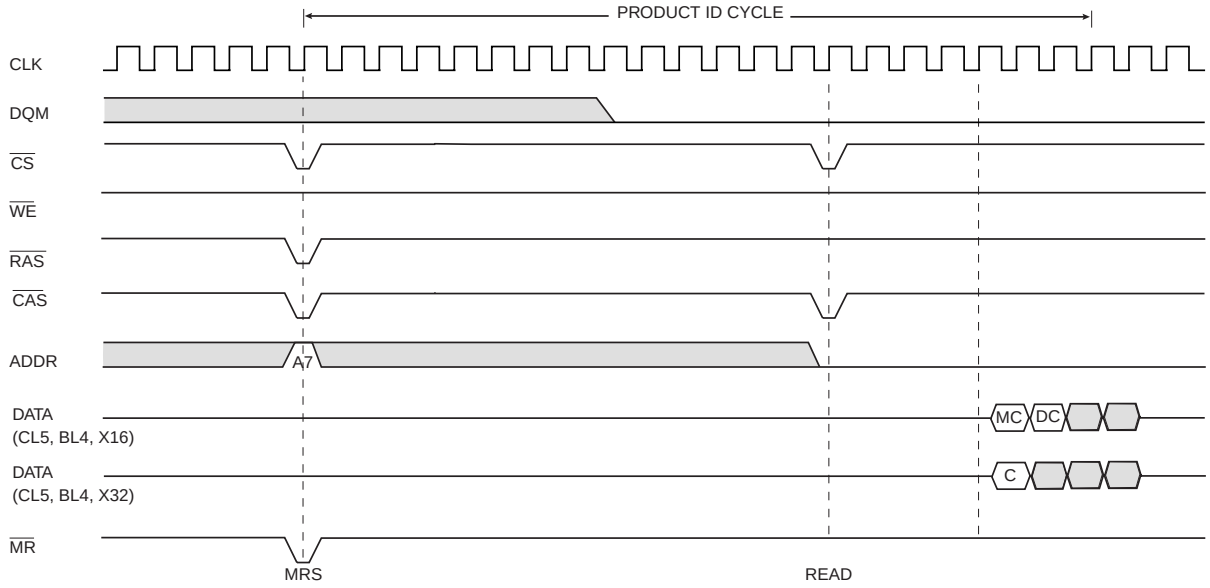
Note: During Program cycle, DATA = complement of loaded DQ7.
After Program cycle, DATA = same state as loaded DQ7.
During Sector Erase cycle, DATA = “0”; after Sector Erase cycle, DATA = “1”.

$\overline{\text{Data}}$ Polling Waveforms for Boot Block



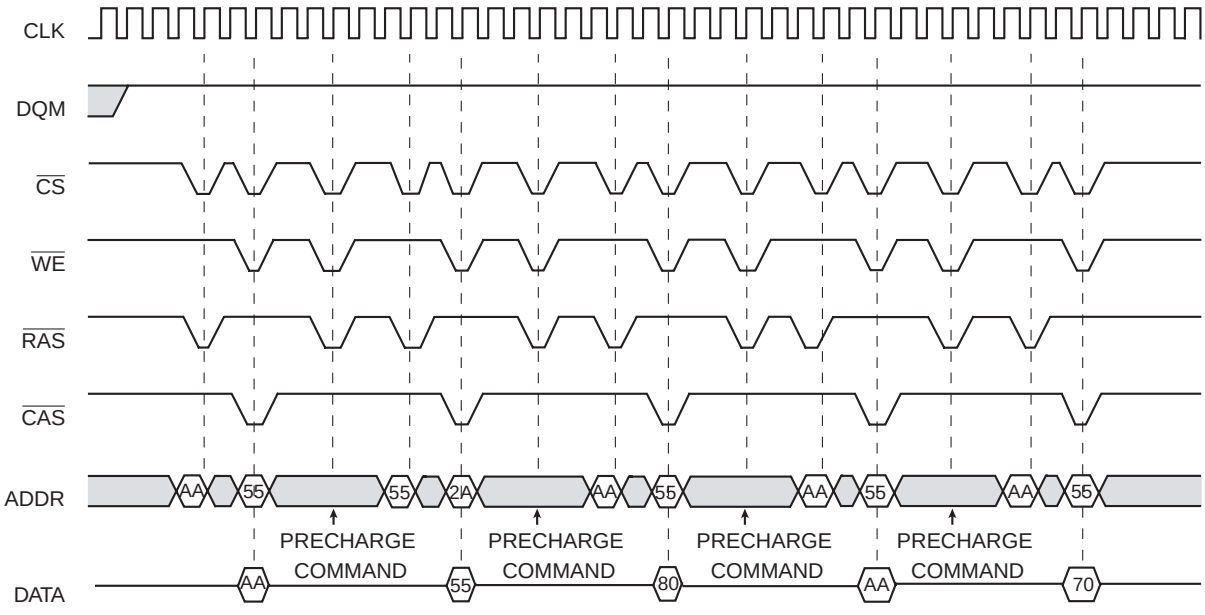
Note: During Program cycle, DATA = complement of loaded DQ7.
After Program cycle, DATA = same state as loaded DQ7.
During Sector Erase cycle, DATA = “0”; after Sector Erase cycle, DATA = “1”.

Product ID Cycle Waveforms

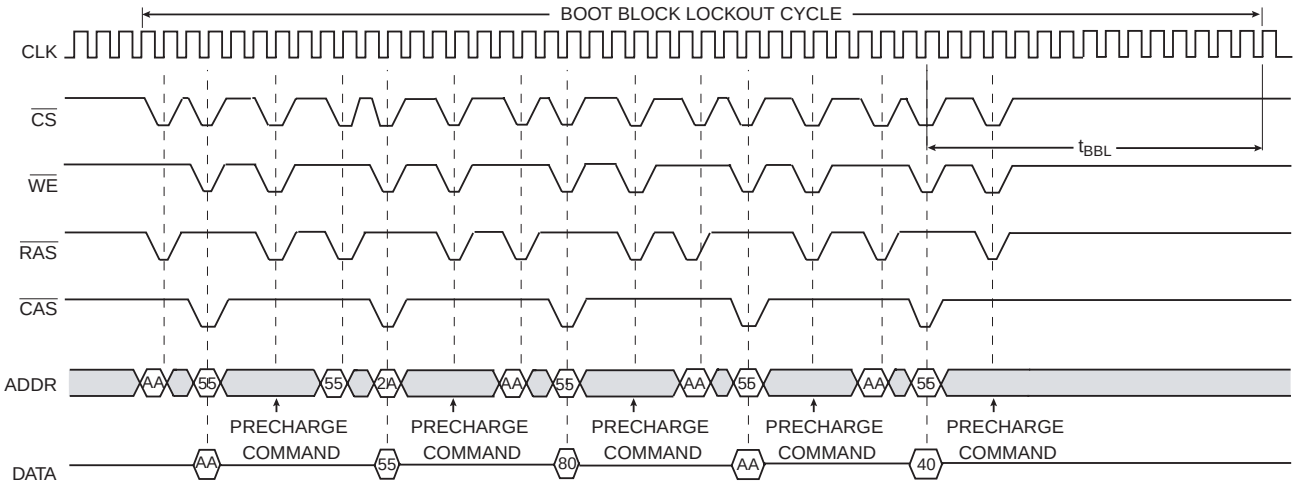


Note: For x16 Mode, Manufacturer Code, MC = 001F(HEX), Device Code, DC = 32C2 (HEX).
For x32 Mode, Code, C = 32C2001F (HEX).

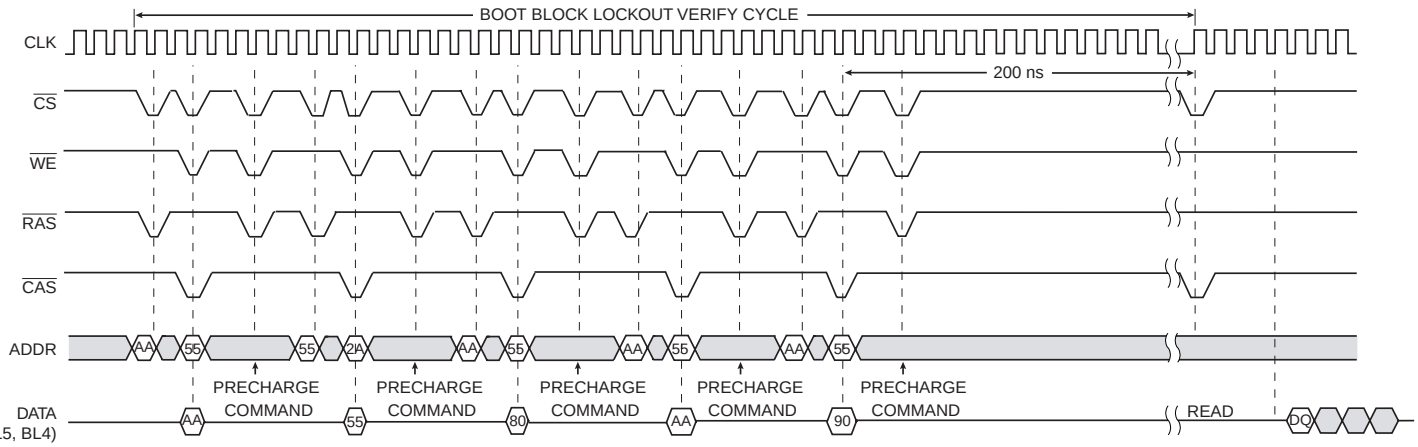
Continuity Test Mode Entry Waveforms



Boot Block Lockout Cycle Waveforms

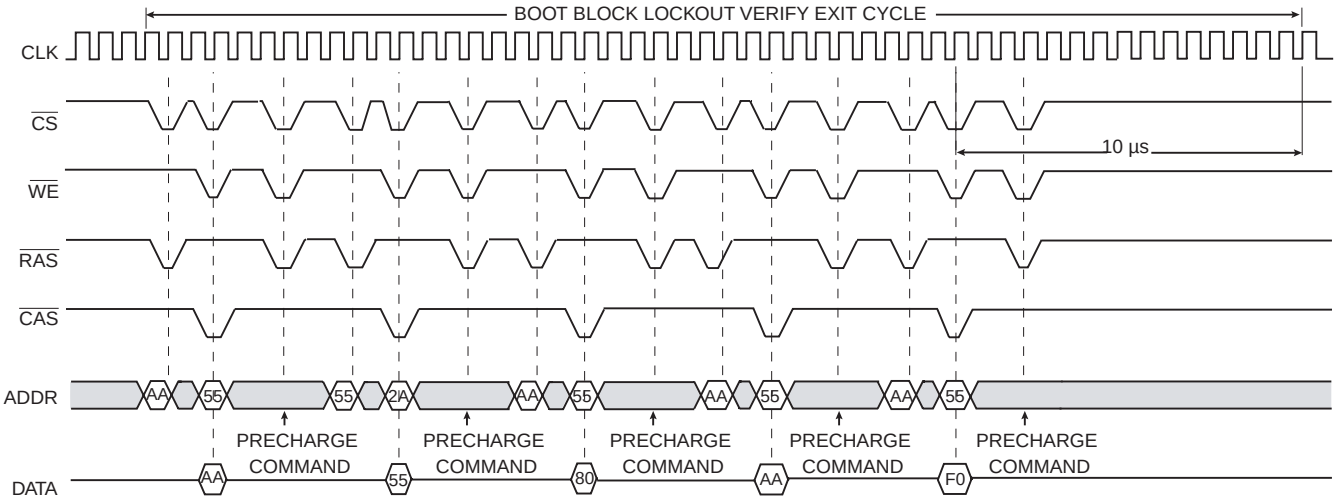


Boot Block Lockout Verify Cycle Waveforms



Note: DQ = XX00 (Hex) implies Boot Block not activated and Lockout not enabled.
DQ = XX01 (Hex) implies Boot Block not activated and Lockout enabled.
DQ = XX02 (Hex) implies Boot Block activated and Lockout not enabled.
DQ = XX03 (Hex) implies Boot Block activated and Lockout enabled.

Boot Block Lockout Verify Exit Cycle Waveforms



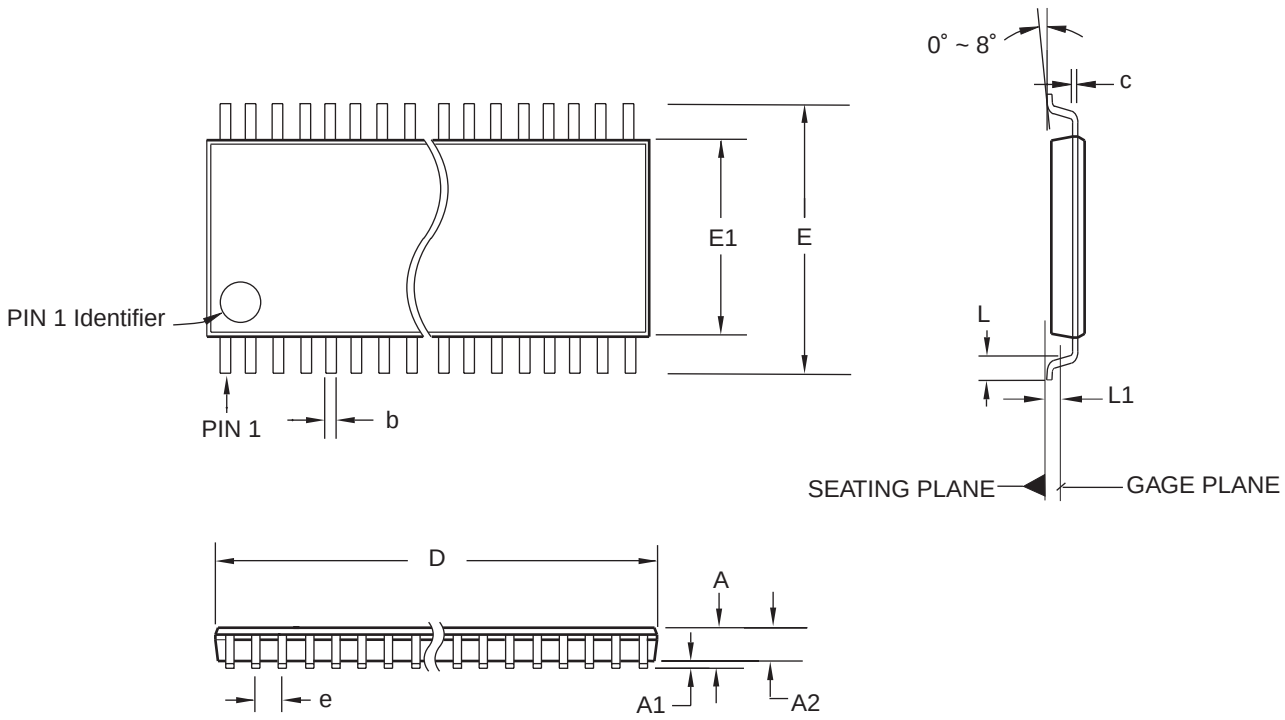
Ordering Information

Max Freq (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	150	0.05	AT49LD3200-10TC	86T	Commercial (0° to 70°C)
	150	0.05	AT49LD3200-10TI	86T	Industrial (-40° to 85°C)
75	150	0.05	AT49LD3200-13TC	86T	Commercial (0° to 70°C)
	150	0.05	AT49LD3200-13TI	86T	Industrial (-40° to 85°C)
50	150	0.05	AT49LD3200-20TC	86T	Commercial (0° to 70°C)
	150	0.05	AT49LD3200-20TI	86T	Industrial (-40° to 85°C)

Package Type	
86T	86-lead, Thin Small Outline Package (TSOP Type II)

Packaging Information

86T – TSOP Type II



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	22.12	22.22	22.32	Note 2
E	11.56	11.76	11.96	
E1	10.06	10.16	10.26	Note 2
L	0.40	0.50	0.60	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.12	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation EC.
2. Dimensions D and E1 do not include mold protrusion. Allowable protrusion on E1 is 0.25 mm per side and on D is 0.15 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**86T,** 86-lead (10.16 mm Body Width) Thin Small Outline Package (TSOP Type ll)	86T	B

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
USA
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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