

AZ12010

Multiply by 16, 32 Phase-Locked Loop Clock Generator

FEATURES

- Differential Inputs/Outputs for External Voltage Controlled SAW Oscillator
- Optional Internal Crystal Oscillator Driver
- Internal Edge-Matching Phase/Frequency Detector
- Internal Charge-Pump/Integrator Amplifier
- RF Bipolar Design for Low Phase Noise
- Available in a 3x3 mm MLP Package

PACKAGE AVAILABILITY

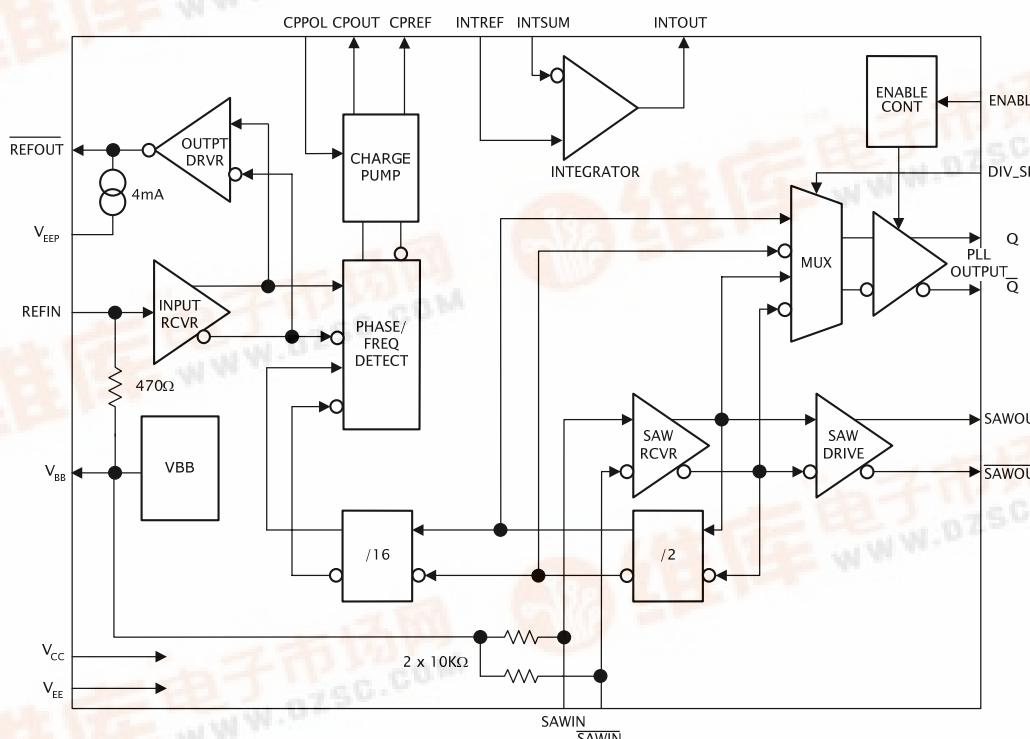
| PACKAGE | PART NO. | MARKING | NOTES |
|--|------------|--------------------------|-------|
| MLP 16 (3x3) | AZ12010AL | AZ12010A <Date Code> | 1,2 |
| MLP 16 (3x3) RoHS Compliant / Lead (Pb) Free | AZ12010AL+ | AZ12010A+ <Date Code> | 1,2 |
| MLP 16 (3x3) | AZ12010BL | AZ12010B <Date Code> | 1,2 |
| MLP 16 (3x3) RoHS Compliant / Lead (Pb) Free | AZ12010BL+ | AZ12010B+ <Date Code> | 1,2 |
| DIE | AZ12010XP | N/A | 3 |

1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts)
Tape & Reel.

2 Date code format: "YY" for year followed by "WW" for week.

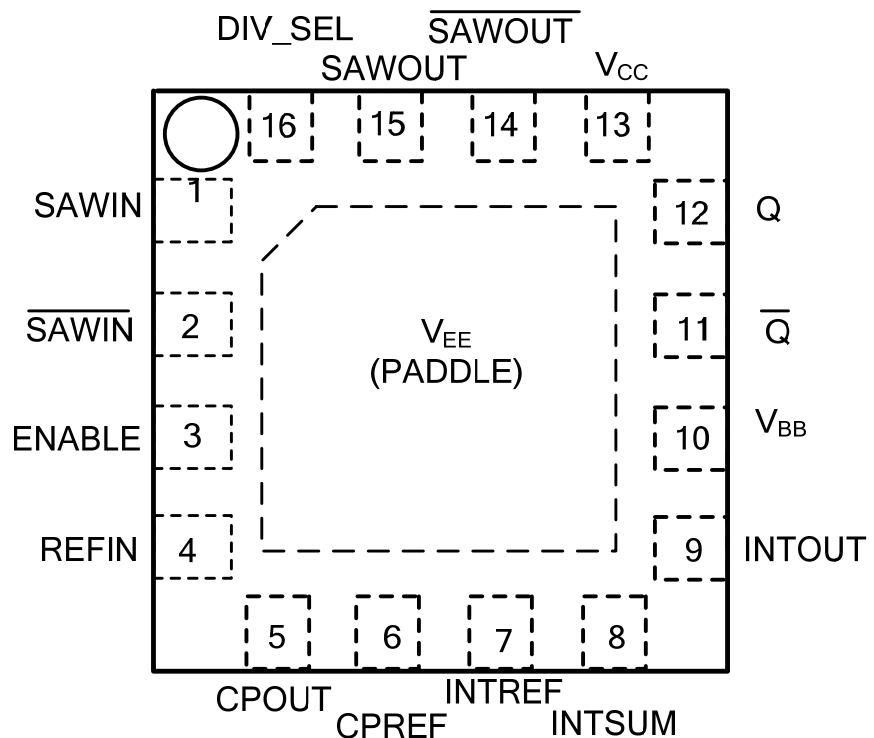
3 Waffle Pack

DESCRIPTION



The AZ12010 contains all of the functional elements necessary to implement a Phase-Locked Loop for clock multiplication at frequencies up to 800 MHz. A fixed 32 times multiplication allows the use of low cost crystals or a low frequency reference signal. The output can be divided by two for 16 times net multiplication. The VCSO is differentially or single-ended driven using the chip CML SAW outputs. The dynamic properties of the PLL are under the control of the user through selection of the desired external components.

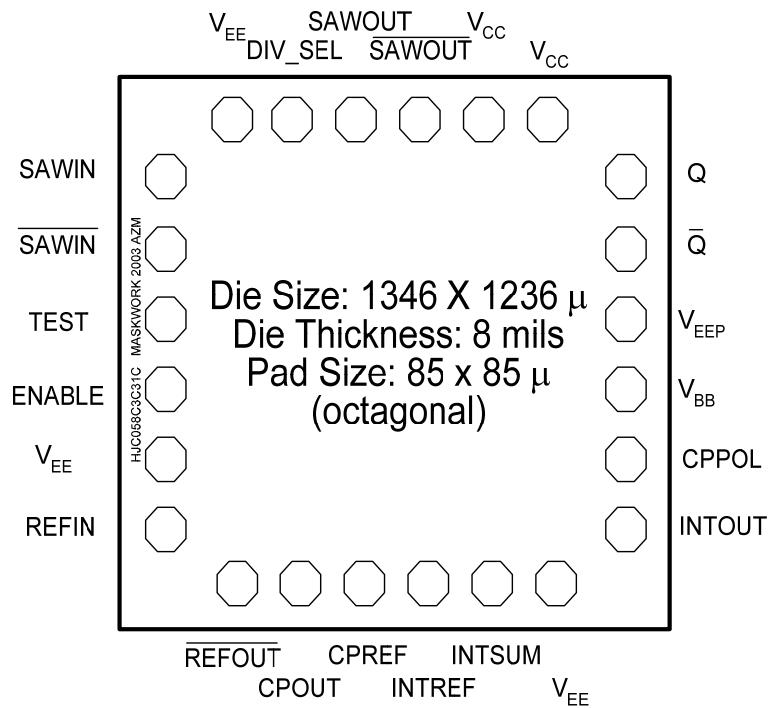
AZ12010



3X3 MLP 16 PACKAGE

AZM12010A: CPPOL pulled High
AZM12010B: CPPOL pulled Low

AZ12010



DIE MAP

Pad Center Locations

| Signal Name | X coordinate (μ) | Y coordinate (μ) |
|-------------|------------------------|------------------------|
| SAWIN | -522.0 | 372.3 |
| SAWIN | -522.0 | 220.3 |
| TEST | -522.0 | 68.3 |
| ENABLE | -522.0 | -83.7 |
| V_{EE} | -522.0 | -235.7 |
| REFIN | -522.0 | -387.7 |
| REFOUT | -365.0 | -515.8 |
| CPOUT | -213.0 | -515.8 |
| CPREF | -61.0 | -515.8 |
| INTREF | 91.0 | -515.8 |
| INTSUM | 243.0 | -515.8 |
| V_{EE} | 395.0 | -515.8 |
| INTOUT | 552.0 | -387.7 |
| CPPOL | 552.0 | -235.7 |
| V_{BB} | 552.0 | -83.7 |
| V_{EEP} | 552.0 | 68.3 |
| \bar{Q} | 552.0 | 220.3 |
| Q | 552.0 | 372.3 |
| V_{CC} | 395.0 | 509.9 |
| V_{CC} | 243.0 | 509.9 |
| SAWOUT | 91.0 | 509.9 |
| SAWOUT | -61.0 | 509.9 |
| DIV_SEL | -219.0 | 509.9 |
| V_{EE} | -377.0 | 509.9 |

AZ12010

AZ12010 FUNCTIONAL PIN/PAD DESCRIPTIONS

| Name | Functional Description | Logic Level |
|-----------|---|------------------|
| REFIN | Reference Frequency Input This pin/pad includes an on-chip $470\ \Omega$ pull down resistor to V_{BB} . The input from the reference circuit should be AC coupled. | |
| REFOUT | Reference Frequency Output This pin is an inverted and amplified version of the signal on the REFIN pin. The gain from REFIN to REFOUT is approximately 20. If V_{EEP} is connected to V_{EE} , a 4 ma on-chip current source is provided for the output. REFOUT is not available on the packaged versions (AZ12010A, AZ12010B). | PECL |
| CPREF | Charge Pump Reference Output The pin/pad voltage is nominally 1.2 volts below V_{CC} . | |
| CPOUT | Charge Pump Output The charge pump output voltage is $V_{CPREF} \pm 0.3V$ during a phase correction pulse. When there is no correction pulse the output goes high impedance. | |
| CPPOL | Charge Pump Polarity When this pin/pad is pulled high the PLL operates with a VCSO circuit exhibiting negative pulling slope (the VCSO frequency goes down when the control voltage goes up). When this pin/pad is pulled low (AZM12010B) the PLL operates with a VCSO circuit exhibiting positive pulling slope (the VCSO frequency goes up when the control voltage goes up). If the pin/pad is left open (AZM12010A), an internal pullup resistor selects negative pulling slope mode. | LVC MOS LVTTL |
| INTREF | Integrator Reference Input This pin/pad should be connected to CPREF through a bias current cancellation network | |
| INTSUM | Integrator Summing Junction This pin/pad is the summing junction for the integrator amplifier | |
| INTOUT | Integrator Output | |
| SAWIN | SAW Amplifier Inputs If only one input is used (Single-ended VCSO), the unused input should be bypassed with a capacitor to V_{BB} . | |
| SAWOUT | SAW Amplifier Outputs These are open collector outputs for driving the VCSO device. Operating at nominally 9 ma, external pullup resistors must be connected between these pins/pads and V_{CC} . If only one output is used, the other output should be connected to V_{CC} through a 50Ω resistor. | CML (Analog) |
| ENABLE | PLL Output Enable The Q and \bar{Q} outputs are enabled when this pin/pad is pulled high. When this pin/pad is low, the Q output is high, and the \bar{Q} output is low. If the pin/pad is left open, an internal pullup resistor enables the outputs. | LVC MOS LVTTL |
| DIV_SEL | Divide Select When this pin/pad is high, the Q and \bar{Q} outputs are divided by one from the SAW device. When it is low, the Q and \bar{Q} outputs are divided by two from the SAW device. If the pin/pad is left open, an internal pullup resistor selects the divide by one mode. | LVC MOS LVTTL |
| Q | Clock Output These pin/pads are the main clock output. When ENABLE is low, the outputs are disabled with Q high and \bar{Q} low. | PECL |
| V_{BB} | Reference Voltage Output This pin/pad is used to bias the REFIN signal. It must be bypassed externally to the V_{EE} pins/pads with a $0.01\ \mu F$ capacitor. | |
| V_{EEP} | REFOUT Current Source If V_{EEP} is connected to V_{EE} , a 4 ma on-chip current source is provided for the REFOUT output. V_{EEP} is not available on the packaged versions (AZ12010A, AZ12010B). | |
| V_{CC} | Positive Supply +3.0 to +3.6 V | |
| V_{EE} | Negative Supply Ground | |

AZ12010

Absolute Maximum Ratings are those values beyond which device life may be impaired.

| Symbol | Characteristic | Rating | | | Unit |
|------------------|--|-------------|--|--|------|
| V _{CC} | Power Supply (V _{EE} = GND) | 0 to +6.0 | | | Vdc |
| V _I | Input Voltage (V _{EE} = GND) | 0 to +6.0 | | | Vdc |
| I _{OUT} | PECL Output Current — Continuous — Surge | 50 100 | | | mA |
| T _A | Operating Temperature Range | -40 to +85 | | | °C |
| T _{STG} | Storage Temperature Range | -65 to +150 | | | °C |

AZ12010 DC CHARACTERISTICS (V_{CC} = +3.0 to +3.6 V, V_{EE} = GND)

| Symbol | Characteristic | -40°C | | 0°C | | 25°C | | | 85°C | | Unit |
|------------------------------------|--|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|------|
| | | Min | Max | Min | Max | Min | Typ | Max | Min | Max | |
| V _{BB} | Reference Voltage | V _{CC} -1.38 | V _{CC} -1.26 | V _{CC} -1.38 | V _{CC} -1.26 | V _{CC} -1.38 | V _{CC} -1.31 | V _{CC} -1.26 | V _{CC} -1.38 | V _{CC} -1.26 | V |
| R _{REF} | REFIN Pull-Down resistor to V _{BB} | | | | | | 470 | | | | Ω |
| R _{SAW} | SAWIN, SAWIN Pull-Down resistor to V _{BB} | | | | | | 10K | | | | Ω |
| V _{HCTL} | High level integrator output | V _{CC} -1.0 | | V _{CC} -1.0 | | V _{CC} -1.0 | | | V _{CC} -1.0 | | V |
| V _{LCTL} | Low level integrator output | | 0.5 | | 0.5 | | | 0.5 | | 0.5 | V |
| V _{OH} | Output HIGH Voltage ¹ Q, \bar{Q} | V _{CC} -1085 | V _{CC} -880 | V _{CC} -1025 | V _{CC} -880 | V _{CC} -1025 | V _{CC} -955 | V _{CC} -880 | V _{CC} -1025 | V _{CC} -880 | mV |
| V _{OH} | Output HIGH Voltage ² SAWOUT, \bar{SAWOUT} | V _{CC} -10 | V _{CC} | V _{CC} -10 | V _{CC} | V _{CC} -10 | | V _{CC} | V _{CC} -10 | V _{CC} | mV |
| V _{OL} | Output LOW Voltage ¹ Q, \bar{Q} | V _{CC} -1830 | V _{CC} -1555 | V _{CC} -1810 | V _{CC} -1620 | V _{CC} -1810 | V _{CC} -1705 | V _{CC} -1620 | V _{CC} -1810 | V _{CC} -1620 | mV |
| V _{OL} | Output LOW Voltage ² SAWOUT, \bar{SAWOUT} | V _{CC} -349 | V _{CC} -481 | V _{CC} -365 | V _{CC} -516 | V _{CC} -392 | V _{CC} -449 | V _{CC} -557 | V _{CC} -465 | V _{CC} -661 | mV |
| V _{IH} | Input HIGH Voltage, LVCMOS/LVTTL EN, DIV_SEL | 2.2 | V _{CC} | 2.2 | V _{CC} | 2.2 | | V _{CC} | 2.2 | V _{CC} | V |
| V _{IL} | Input LOW Voltage, LVCMOS/LVTTL EN, DIV_SEL | 0.0 | 0.8 | 0.0 | 0.8 | 0.0 | | 0.8 | 0.0 | 0.8 | V |
| I _{CC} (I _{EE}) | Power Supply Current | | 65 | | 65 | 45 | 54 | 65 | | 65 | mA |

1. Load is 50Ω to V_{CC}-2V
2. Load is 50Ω to V_{CC}

AZ12010 AC CHARACTERISTICS (V_{CC} = +3.0 to +3.6 V, V_{EE} = GND)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|---------------------------------|--|-------|------|-----|------|------|------|------|-----|------|-----------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| A _{PD} | Phase Detector Gain | | | | | 20.3 | | | | | radians/V |
| f _{VCO} | External VSCO frequency | | | 800 | | | 800 | | | 800 | MHz |
| t _r / t _f | Output Rise & Fall Times (20% - 80%) Q, \bar{Q} | | | | | 120 | | | | | ps |
| a _V | SAW Amplifier and Driver Gain at 622.08 MHz ¹ | 18 | 24.5 | 28 | 15.5 | 21 | 24.5 | 13.5 | 19 | 22.5 | dB |

1. Single Ended Input and Output, Driven from 50Ω backmatched source, Load 50Ω to V_{CC}.

AZ12010

Loop Filter Design

The combination of the phase detector, amplifier, VCO and divider form a second-order phase-locked loop. Proper selection of the loop components is important to obtain stable, low jitter operation.

The loop bandwidth (or natural frequency, ω_n) and damping factor (ζ) are the two major driving forces that define the loop's response to a disturbance. The value of ζ is typically 0.7 to ensure the fastest step response consistent with no ringing. However in many oscillator application ζ may be 3 or higher to provide further phase noise reduction. ω_n is chosen as a compromise between settling time, VCO jitter and reference feedthrough. These values can be computed by the following equations:

$$\omega_n = \frac{1}{N} \sqrt{\frac{K_\phi K_{VCO}}{\tau_1}}$$

$$\zeta = \frac{\tau_2 \omega_n}{2}$$

$$\tau_1 = R_1 C_1$$

$$\tau_2 = R_2 C_1$$

K_ϕ = Phase Detector Gain (20.3 radians/V)

K_{VCO} = VCO Gain (radians/sec/volt)

N = Frequency Divisor value (32)

The component definitions are shown in the figure below. R3 should be equal to R1 to minimize integrator offsets.

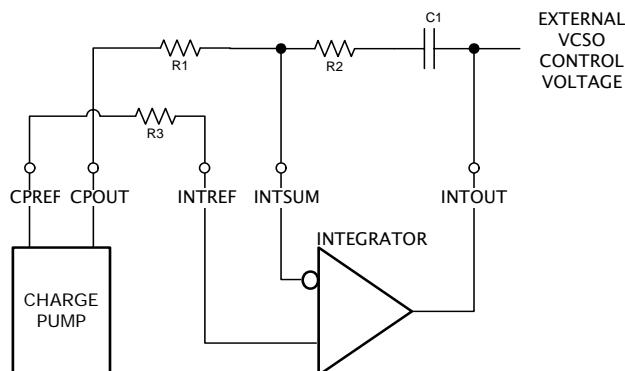


Figure 1 Charge Pump and Integrator

AZ12010

Application Circuit

A typical application circuit is shown in Figure 2.

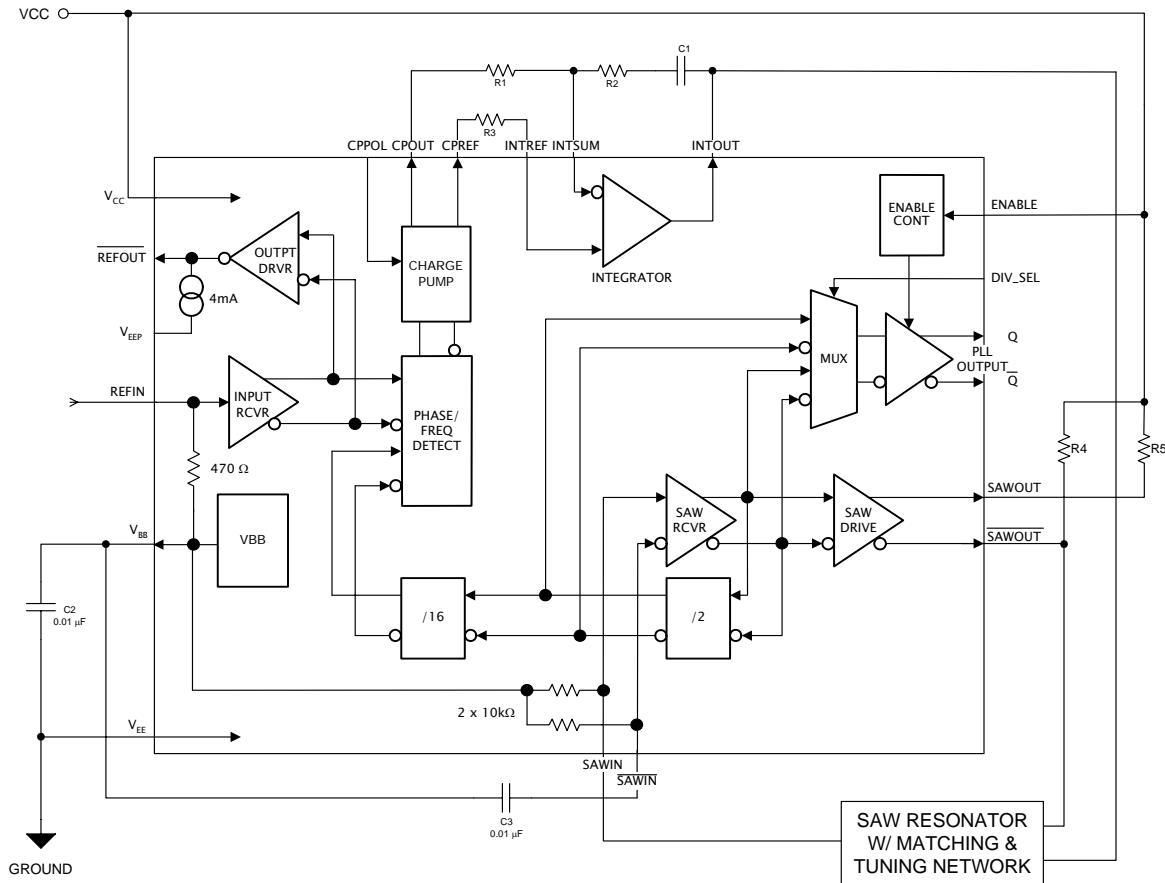
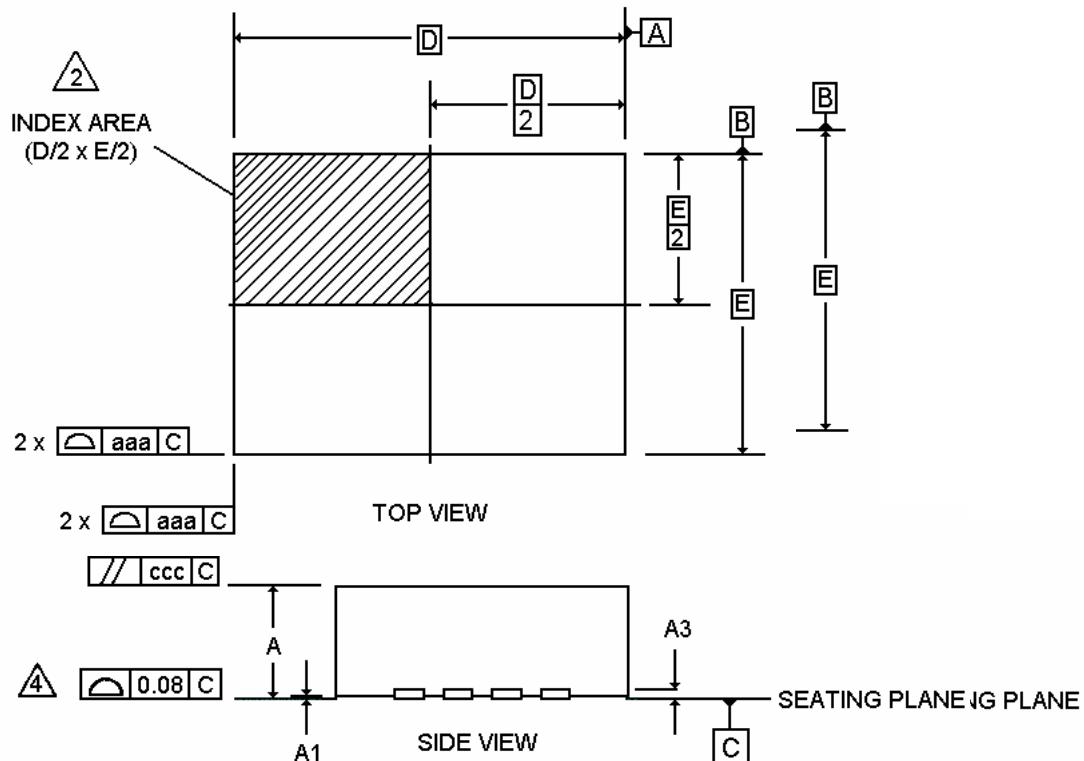


Figure 2. Typical Application, Always Enabled and Divide by One for Output

AZ12010

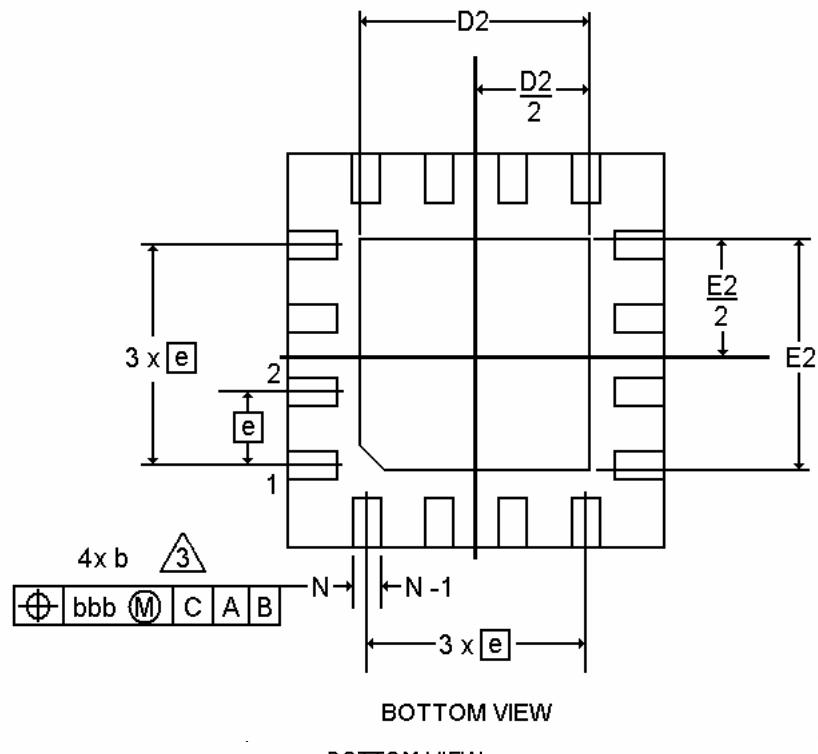
**PACKAGE DIAGRAM
MLP 16**



NOTES

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
3. DIMENSION b APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM PAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 0.80 | 1.10 |
| A1 | 0.00 | 0.05 |
| A3 | 0.25 REF | |
| b | 0.225 | 0.275 |
| D | 2.90 | 3.10 |
| D2 | 1.65 | 1.95 |
| E | 2.90 | 3.10 |
| E2 | 1.65 | 1.95 |
| e | 0.50 BSC | |
| L | 0.35 | 0.45 |
| aaa | 0.25 | |
| bbb | 0.10 | |
| ccc | 0.10 | |



AZ12010

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