Data Book

AU9720

USB to Serial Bridge Controller

Technical Reference Manual

Product Specification

Official Release

Revision 1.05W

Public

Apr 2005

Data Sheet Status

Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

Revision History

Date	Revision	Description
Apr. 2005	1.05W	Removed the schematics. Please contact our sales if you need it.

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1.0. Introduction

1.1. Description

The **AU9720** operates as a bridge between one USB port and one standard RS232 Serial port. The two large on-chip buffers have been pre-configured to accommodate the data flow between two different buses. The USB bulk-type data is adopted for maximum data transfer, which could be up to 6M bits/sec. Automatic handshake is supported at the Serial port. With these, a much higher baud rate can be achieved compared to the system uses legacy UART controller.

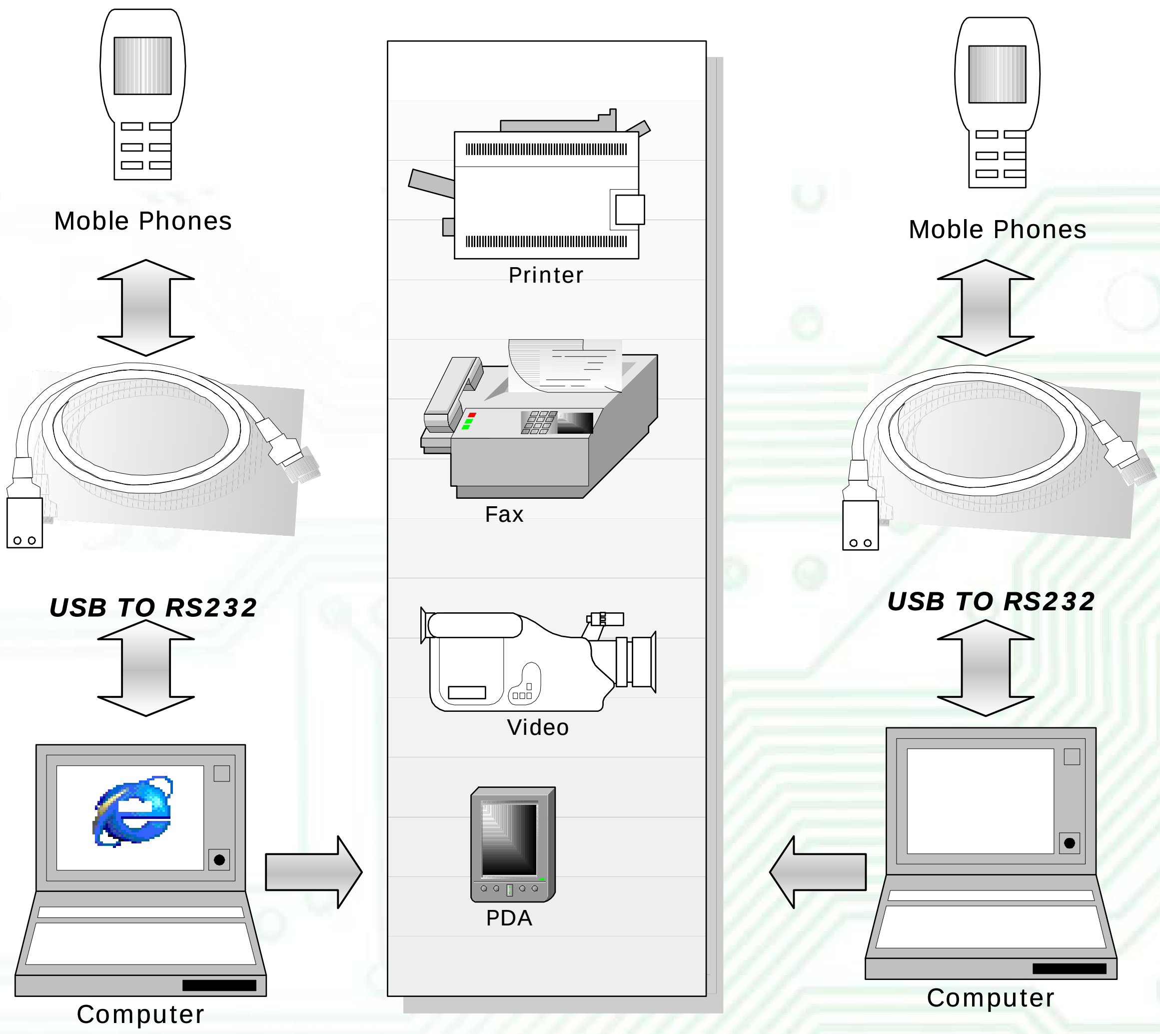
This device is also compliant with USB power management and remote wakeup scheme. Only minimum required power is consumed from the host during Suspend. By integrating all the function in a 28-SSOP package, this chip is suitable to be embedded inside a data cable. With such cables, users can connect between a PC host and any device with RS232 interface.

1.2. Features

- Support USB Specification v1.1 and USB CDC v1.1
- Support the RS232 Serial interface
- Support automatic handshake mode
- Support automatic hardware flow control with CTS/RTS
- Support automatic software flow control with XON/XOFF
- Support Remote wake-up and power management
- 384/128 bytes buffer each for upstream and downstream data flow
- Support default ROM or external EEPROM for device configuration
- On chip USB transceiver
- Crystal oscillator running at 12MHz
- Support Windows 98/SE, ME, 2000, XP, Windows CE3.0, CE.NET, Linux, and Mac OS
- 28 Pins SSOP Lead-Free package

2.0. Application Diagram

The following diagram shows several typical applications using AU9720. By connecting the USB connector to a desktop or notebook PC through AU9720, which is implemented as a bus-powered, a programmable speed could be gained to transfer data between PC and mobile phones with much higher baud rate speed than what normal UART devices could offer.



3.0. Pin Assignment

The AU9720 is packaged in 28pin SSOP Lead-Free. The following figure shows signal name for each pin and the table in the following page describes each pin in details.

Figure 3.1 Pin Assignment Diagram

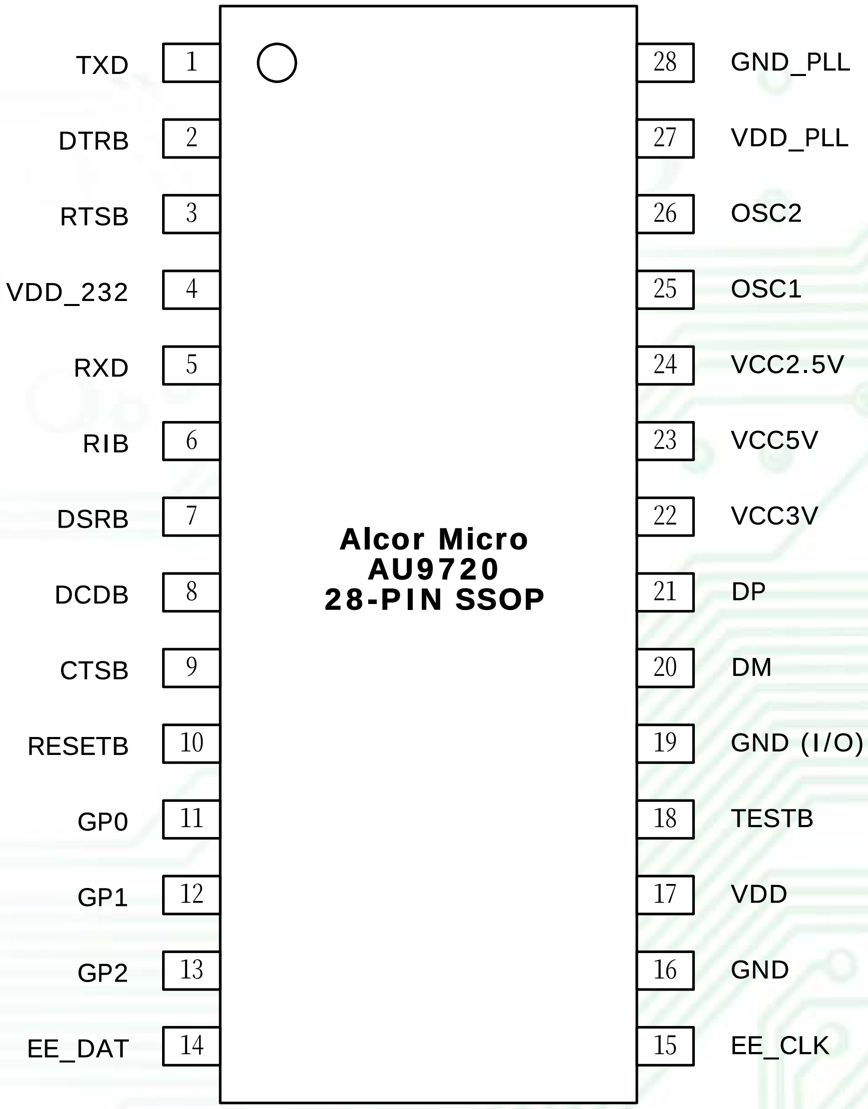


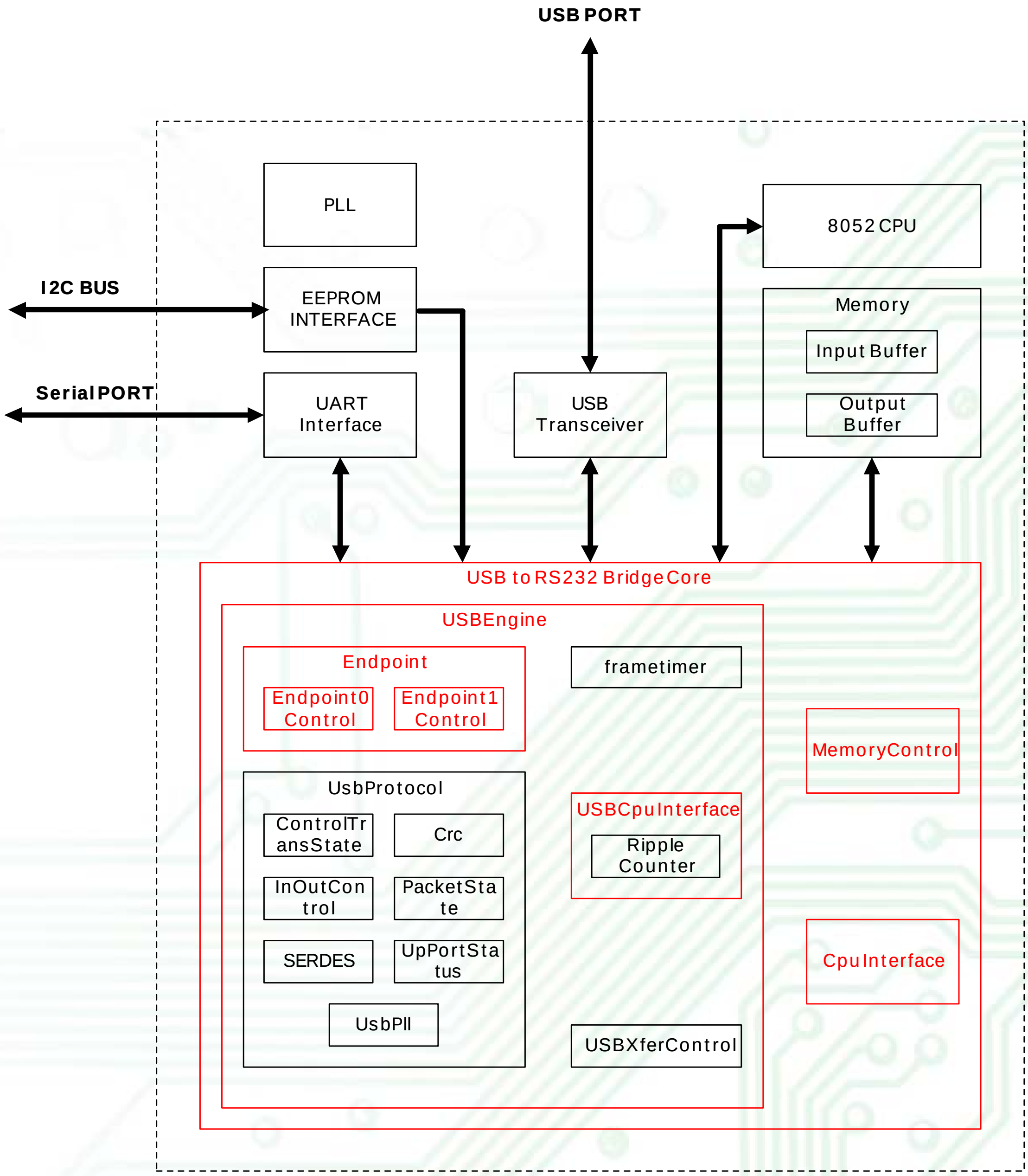
Table 3.1 Pin Assignments

Pin#	Pin Name	I/O	Description
1	TXD	O	Data Output to serial port
2	DTRB	O	Low: Data Terminal Ready (serial port)
3	RTSB	O	Low: Request To Send; (serial port)
4	VDD_232	PWR	VDD for RS-232 (Input)
5	RXD	I	Data Input from serial port
6	RIB	I	Low: Ring Indicator (Serial Port)
7	DSRB	I	Low: Data Set Ready (Serial port)
8	DCDB	I	Low: Data Carrier Detect (serial port)
9	CTSB	I	Low: Clear to send (serial port)
10	RESETB	I	System reset
11	GP0	I/O	Reserved for System Output use
12	GP1	I/O	High (connect with external 47K resistor) for USB Heavy Load (500mA); Low (connect with external 220K resistor) for USB Light Load (100mA)
13	GP2	I/O	Shutdown Transceiver under Suspend mode
14	EE_DAT	I/O	External EEPROM data signal
15	EE_CLK	I/O	External EEPROM clock
16	GND	PWR	Ground
17	VDD	PWR	Power input (3.3V)
18	TESTB	I	Reserved
19	GND (I/O)	PWR	I/O Ground
20	DM	I/O	USB DMINUS signal
21	DP	I/O	USB DPLUS Signal
22	VCC3V	PWR	3.3v power output
23	VCC5V	PWR	5v power input
24	VCC2.5V	PWR	2.5v power output
25	OSC1	I	Crystal oscillator input
26	OSC2	O	Crystal oscillator output
27	VDD_PLL	PWR	3.3V input power for PLL
28	GND_PLL	PWR	Ground for PLL

4.0. System Architecture and Reference Design

4.1. Block Diagram

Figure 4.1 AU9720 USB to Serial Bridge controller Block Diagram



5.0. Electrical Characteristics

5.1 Recommended Operating Conditions

Table 5.1 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	4.75	5	5.25	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	0		85	^oC
T_{STG}	Storage Temperature	-40		125	^oC

5.2 General DC Characteristics

Table 5.2 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input low current	no pull-up or pull-down	-1		1	μA
I_{IH}	Input high current	no pull-up or pull-down	-1		1	μA
I_{OZ}	Tri-state leakage current		-10		10	μA
C_{IN}	Input capacitance			5		ρF
C_{OUT}	Output capacitance			5		ρF
C_{BID}	Bi-directional buffer capacitance			5		ρF

5.3 DC Electrical Characteristics for 3.3 volts operation

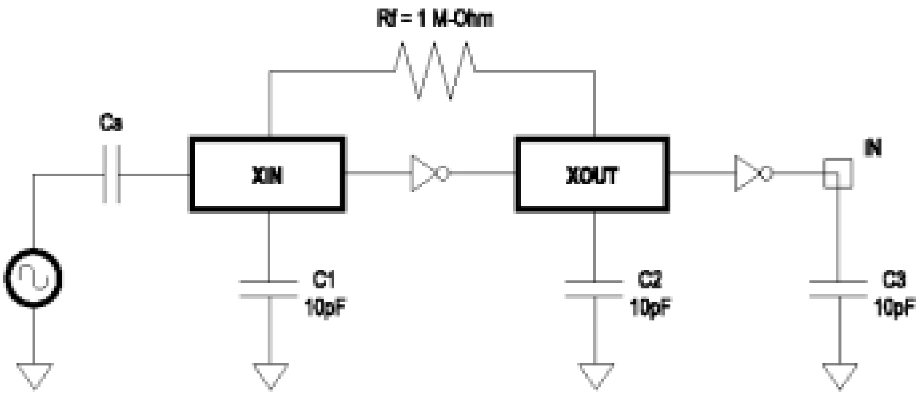
Table 5.3 DC Electrical Characteristics for 3.3 volts operation

SYMBO	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	CMOS			0.9	V
V_{IH}	Input Hight Voltage	CMOS	2.3			V
V_{OL}	Output low voltage	I_{OL}=4mA, 16mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=4mA,16mA	2.4			V
R_I	Input Pull-up/down resistance	Vil=0_V or Vih=V_{CC}		10K/200K		KΩ

5.4 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.

Figure 5.1 Crystal Oscillator Circuit Setup for Characterization



5.5 ESD Test Results

Test Description: ESD Testing was performed on a Zapmaster system using the Human-Body-Model (HBM) and Machine-Model (MM), according to MIL-STD 883 and EIAJ IC-121 respectively.

- Human-Body-Model stresses devices by sudden application of a high voltage supplied by a 100pF capacitor through 1.5k-ohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200pF capacitor through very low (0 ohm) resistance.

Test circuit & condition

- Zap Interval: 1 second
- Number of Zaps: 3 positive and 3 negative at room temperature
- Criteria: I-V Curve Tracing

Table 5.4 ESD Data

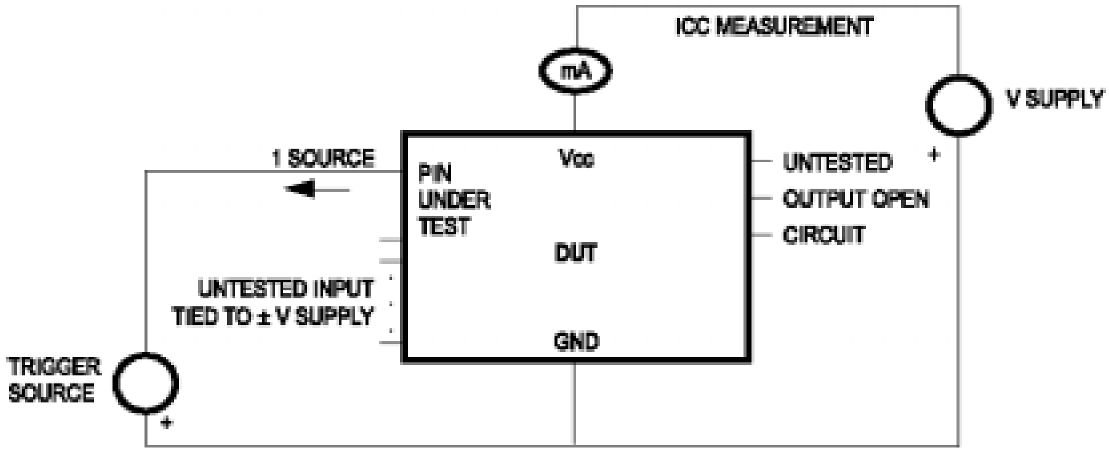
Model	Mode	S/S	Target	Results
HBM	Vdd, Vss, I/C	15	6000V	PASS
MM	Vdd, Vss, I/C	15	200V	PASS

5.6 Latch-Up Test Results

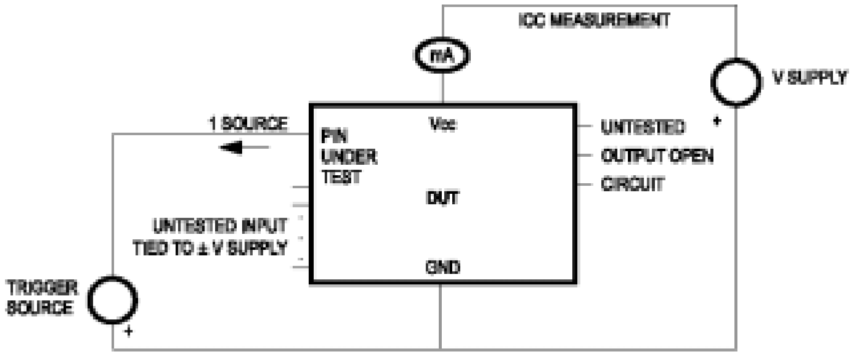
Test Description: Latch-Up testing was performed at room ambience using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss, to which 5Volts and ground were biased respectively. Testing was started at 5.0V (Positive) or 0V (Negative), and the DUT was biased for 0.5 seconds.
If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=00mA, Icc=100mA), then the voltage was increased by 0.1Volts and the pin was tested again.
This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

Notes:
1. DUT: The device under test.
2. PUT: The pin under test.

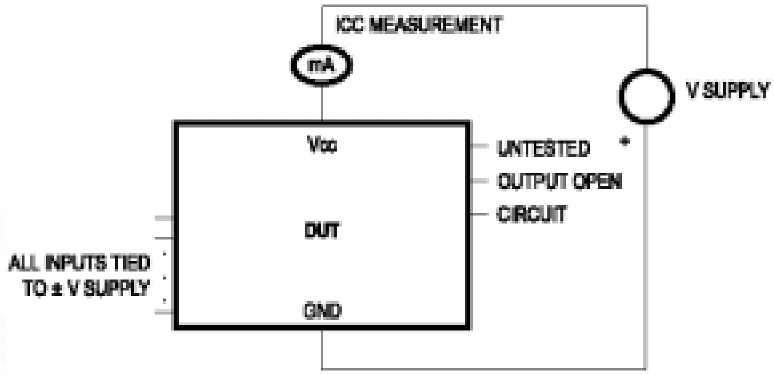
Figure 5.2 Latch-Up Test Results



Test Circuit: Positive Input/Output Overvoltage/Overcurrent



Test Circuit: Negative Input/Output Overvoltage/Overcurrent



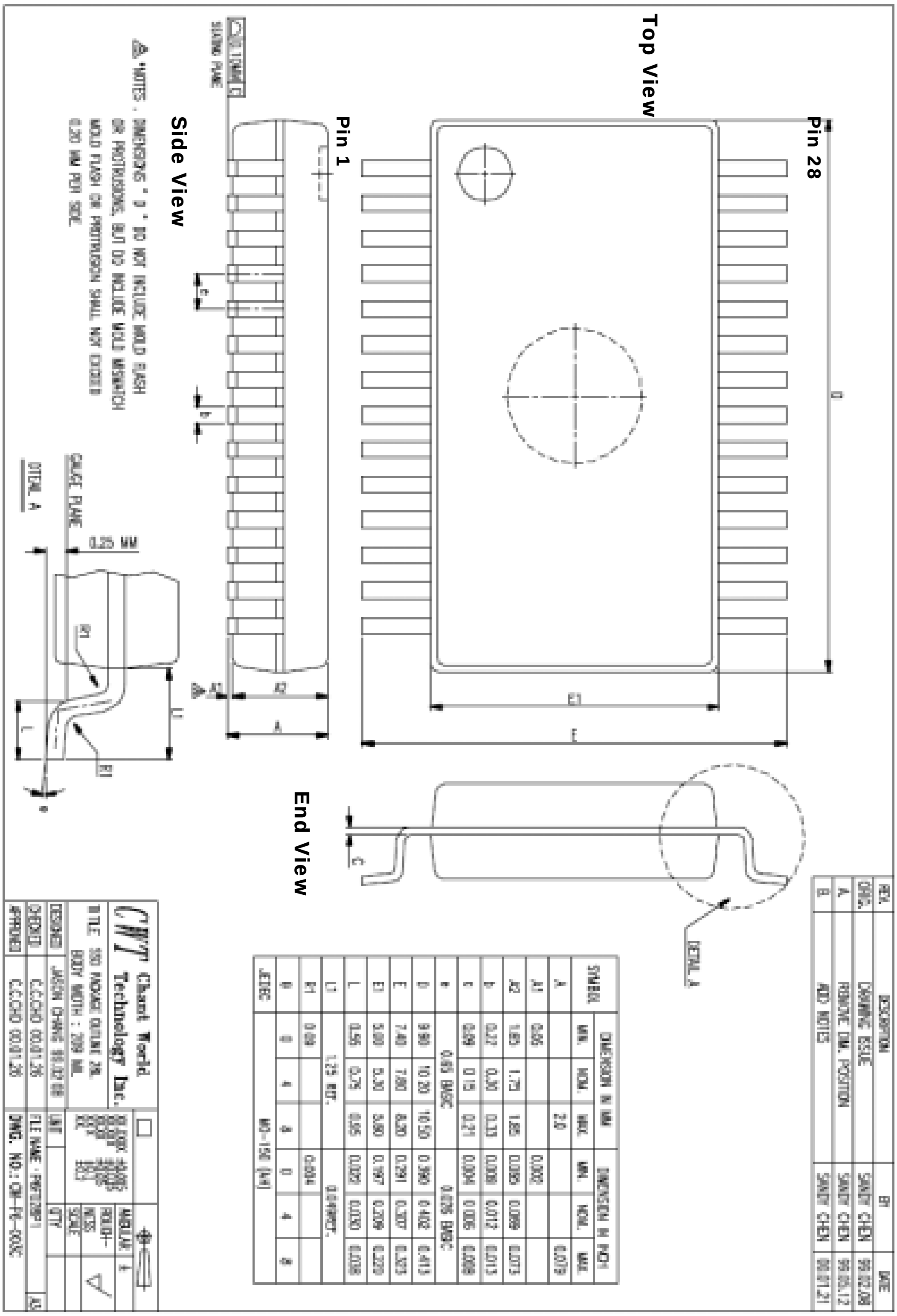
Supply Overvoltage Test

Table 5.5 Latch–Up Data

Mode		Voltage (V)/Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0	5	Pass
Current	+	200	5	Pass
	-	200	5	Pass
Vdd - Vxx		9.0	5	Pass

6.0 Mechanical Information

Figure 6.1 Mechanical Information Diagram



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About Alcor Micro, Corp

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California.

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