



查询42671-00供应商

Peregrine Semiconductor

捷多邦, 专业PCB打样工厂, 24小时加急出货

# Preliminary Specification PE42671 DIE

## SP7T UltraCMOS™ 2.75 V Switch 100 – 3000 MHz, +68 dBm IIP3

Figure 1. Functional Diagram

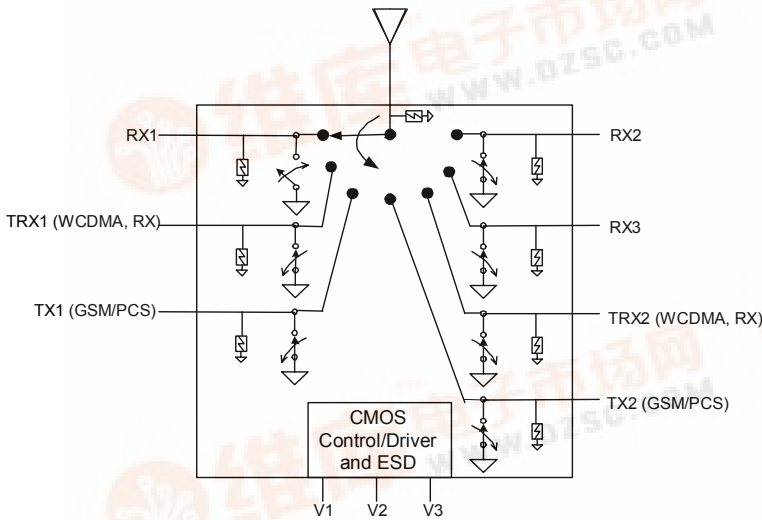
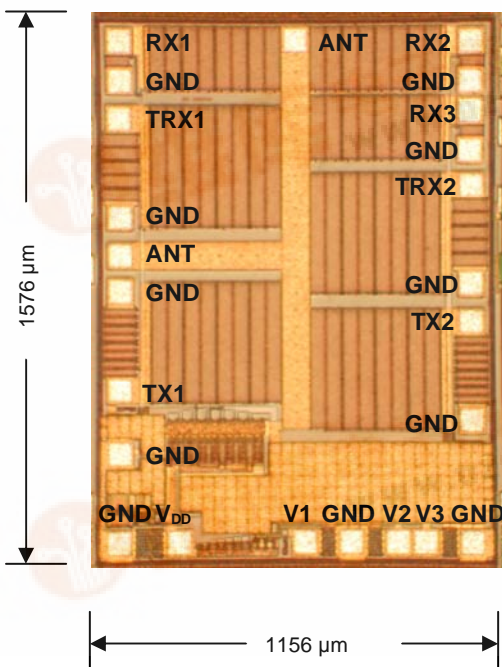


Figure 2. Die Top View\*



### Features

- 2 TX, 2 TRX, 3 RX ports
- Three pin CMOS logic control with integral decoder/driver
- Exceptional harmonic performance:  $2f_o = -83$  dBc and  $3f_o = -78$  dBc
- Low TX insertion loss: 0.65 dB at 900 MHz, 0.75 dB at 1900 MHz
- TX – RX Isolation of 47 dB at 900 MHz, 40 dB at 1900 MHz
- 1500 V HBM ESD tolerance all ports
- +68 dBm IIP3 @ 50 Ω
- -111 dBm IMD3
- No blocking capacitors required

### Product Description

The PE42671 is a HaRP™-enhanced SP7T RF Switch developed on the UltraCMOS™ process technology. It addresses the specific design needs of the Quad-Band GSM Handset Antenna Switch Module Market for use in GSM/PCS/EDGE/WCDMA handsets. The switch is comprised of two transmit ports that can be used for GSM/PCS/EDGE, two transmit/receive ports (TRX1 and TRX2) that can be used for either WCDMA or as receive ports, and three symmetric receive ports. On-chip CMOS decode logic facilitates three-pin low voltage CMOS control, while high ESD tolerance of 1500 V at all ports, no blocking capacitor requirements, and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ruggedness.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.



**Table 1. Target Electrical Specifications @ 25 °C, V<sub>DD</sub> = 2.75 V**

Parameter	Condition	Typ	Units
Insertion loss <sup>1</sup>	TX - ANT (850 / 900)	0.65	dB
	TX - ANT (1800 / 1900)	0.75	dB
	TRX - ANT ( 850 WCDMA )	0.6	dB
	TRX - ANT ( 2100 WCDMA )	0.75	dB
	RX - ANT (850 / 900)	0.95	dB
	RX - ANT (1800 / 1900)	1.0	dB
Return Loss	Port under test in on state (850 / 900) (1800 / 1900 / 2100)	20	dB
		15	dB
Isolation	TX - RX (850 / 900)	47	dB
	TX - RX (1800 / 1900)	40	dB
	TX - TX (850 / 900)	33	dB
	TX - TX (1800 / 1900)	27	dB
	TX - TRX (850 / 900)	36	dB
	TX - TRX (1800 / 1900)	29	dB
	TRX - RX ( 850 WCDMA ) TRX - RX (2100 WCDMA)	40 31	dB dB
2nd Harmonic	TX 850 / 900 MHz, +35 dBm output power, 50 Ω	-83	dBc
	TX 1800 / 1900 MHz, +33 dBm output power, 50 Ω	-82	dBc
3rd Harmonic	TX 850 / 900 MHz, +35 dBm output power, 50 Ω	-78	dBc
	TX 1800 / 1900 MHz, +33 dBm output power, 50 Ω	-78	dBc
WCDMA 2100 IMD3	TRX1 / TRX2: Measured at 2.14 GHz at ANT port, input +20 dBm CW signal at 1.95 GHz and -15 dBm CW signal at 1.76 GHz	-111	dBm
WCDMA 2100 IIP3	TRX1 / TRX2: Measured at 2.14 GHz at ANT port, input +20 dBm CW signal at 1.95 GHz and -15 dBm CW signal at 1.76 GHz	+68	dBm

Note: 1. Insertion loss specified with optimal impedance matching.

**Table 2. Operating Ranges**

Parameter	Symbol	Min	Typ	Max	Units
Temperature range	T <sub>OP</sub>	-40		+85	°C
V <sub>DD</sub> Supply Voltage	V <sub>DD</sub>	2.65	2.75	2.85	V
I <sub>DD</sub> Power Supply Current (V <sub>DD</sub> = 2.75 V)	I <sub>DD</sub>		13	50	μA
TX input power <sup>2</sup> (VSWR ≤ 3:1) 824-915 MHz	P <sub>IN</sub>			+35	dBm
TX input power <sup>2</sup> (VSWR ≤ 3:1) 1710-1910 MHz				+33	
TRX input power (VSWR ≤ 3:1) 824 - 2170 MHz				+31	
RX input power <sup>2</sup> (VSWR =1:1)	P <sub>IN</sub>			+20	dBm
Control Voltage High	V <sub>IH</sub>	1.4			V
Control Voltage Low	V <sub>IL</sub>			0.4	V

Note: 2. Assumes RF input period of 4620 μs and duty cycle of 50%.

**Table 3. Absolute Maximum Ratings**

Symbol	Parameter/Conditions	Min	Max	Units
V <sub>DD</sub>	Power supply voltage	-0.3	4.0	V
V <sub>I</sub>	Voltage on any input	-0.3	V <sub>DD</sub> + 0.3	V
T <sub>ST</sub>	Storage temperature range	-65	+150	°C
P <sub>IN</sub> (50 Ω)	TX input power (50 Ω) <sup>3,4</sup> 824-915 MHz		+38	dBm
	TX input power (50 Ω) <sup>3,4</sup> 1710-1910 MHz		+36	
	TRX input power (50 Ω) 824 - 2170 MHz		+34	
	RX input power (50 Ω) <sup>3,4</sup>		+23	
P <sub>IN</sub> (∞:1)	TX input power (VSWR = (∞:1) <sup>3,4</sup> 824-915 MHz		+35	dBm
	TX input power (VSWR = (∞:1) <sup>3,4</sup> 1710-1910 MHz		+33	
	TRX input power (VSWR = (∞:1) 824 - 2170 MHz		+31	
V <sub>ESD</sub>	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		1500	V

Note: 3. Assumes RF input period of 4620 μs and duty cycle of 50%.

4. V<sub>DD</sub> within operating range specified in Table 2.

Part performance is not guaranteed under these conditions. Exposure to absolute maximum conditions for extended periods of time may adversely affect reliability. Stresses in excess of absolute maximum ratings may cause permanent damage.

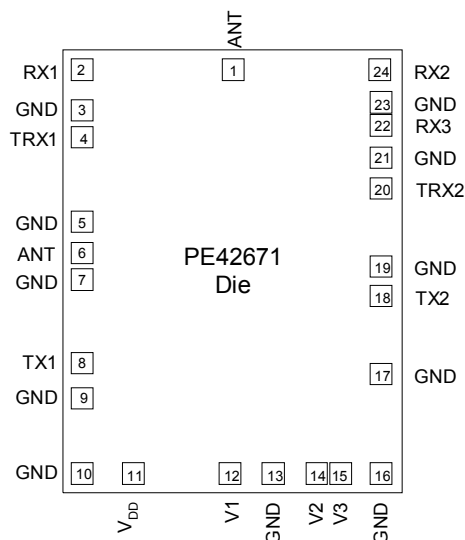
**Table 4. Pin Descriptions**

Pin No.	Pin Name	Description
1	ANT	RF Common – Antenna Redundant ANT pins for flexible bonding
2	RX1 <sup>6</sup>	RF I/O – RX1
3	GND <sup>5</sup>	Ground
4	TRX1 <sup>6</sup>	RF I/O – TRX1
5	GND <sup>5</sup>	Ground
6	ANT	RF Common – Antenna Redundant ANT pins for flexible bonding
7	GND <sup>5</sup>	Ground
8	TX1 <sup>6</sup>	RF I/O - TX1
9	GND <sup>5</sup>	Ground
10	GND <sup>5</sup>	Ground
11	V <sub>DD</sub>	Supply
12	V1	Switch control input, CMOS logic level
13	GND <sup>5</sup>	Ground
14	V2	Switch control input, CMOS logic level
15	V3	Switch control input, CMOS logic level
16	GND <sup>5</sup>	Ground
17	GND <sup>5</sup>	Ground
18	TX2 <sup>6</sup>	RF I/O – TX2
19	GND <sup>5</sup>	Ground
20	TRX2 <sup>6</sup>	RF I/O – TRX2
21	GND <sup>5</sup>	Ground
22	RX3 <sup>6</sup>	RF I/O – RX3
23	GND <sup>5</sup>	Ground
24	RX2 <sup>6</sup>	RF I/O – RX2

Notes: 5. Bond wires should be physically short and connected to ground plane for best performance.

6. Blocking capacitors needed only when non-zero DC voltage present.

**Figure 3. Pad Configuration (Top View)**



**Table 5. Truth Table**

Path	V3	V2	V1
TX1 - ANT	0	0	0
TX2 - ANT	0	0	1
TRX1 - ANT	0	1	0
TRX2 - ANT	1	1	0
RX1 - ANT	0	1	1
RX2 - ANT	1	0	0
RX3 - ANT	1	0	1

**Electrostatic Discharge (ESD) Precautions**

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

**Latch-Up Avoidance**

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

**Table 6. Ordering Information**

Order Code	Description	Package	Shipping Method
42671-90	PE42671-DIE-D	Film Frame	Wafer (Gross Die / Wafer Quantity)
42671-99	PE42671-DIE-400G	Waffle Pack	400 Dice / Waffle Pack
42671-00	PE42671-DIE-1H	Evaluation Kit	1/ box

## Sales Offices

### *The Americas*

#### **Peregrine Semiconductor Corporation**

9450 Carroll Park Drive  
San Diego, CA 92121  
Tel: 858-731-9400  
Fax: 858-731-9499

### *Europe*

#### **Peregrine Semiconductor Europe**

Bâtiment Maine  
13-15 rue des Quatre Vents  
F-92380 Garches, France  
Tel: +33-1-47-41-91-73  
Fax : +33-1-47-41-91-73

#### **Space and Defense Products**

##### **Americas:**

Tel: 858-731-9453

##### **Europe, Asia Pacific:**

180 Rue Jean de Guiramand  
13852 Aix-En-Provence Cedex 3, France  
Tel: +33(0) 4 4239 3361  
Fax: +33(0) 4 4239 7227

### *North Asia Pacific*

#### **Peregrine Semiconductor K.K.**

Teikoku Hotel Tower 10B-6  
1-1-1 Uchisaiwai-cho, Chiyoda-ku  
Tokyo 100-0011 Japan  
Tel: +81-3-3502-5211  
Fax: +81-3-3502-5213

#### **Peregrine Semiconductor, Korea**

#B-2402, Kolon Tripolis, #210  
Geumgok-dong, Bundang-gu, Seongnam-si  
Gyeonggi-do, 463-480 S. Korea  
Tel: +82-31-728-4300  
Fax: +82-31-728-4305

### *South Asia Pacific*

#### **Peregrine Semiconductor, China**

Shanghai, 200040, P.R. China  
Tel: +86-21-5836-8276  
Fax: +86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: [www.psemi.com](http://www.psemi.com)

## Data Sheet Identification

### **Advance Information**

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### **Preliminary Specification**

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

### **Product Specification**

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS and HaRP are trademarks of Peregrine Semiconductor Corp.