Features

- 32-Mbit Flash and 4-Mbit/8-Mbit PSRAM
- Single 66-ball (8 mm x 10 mm x 1.2 mm) CBGA Package
- 2.7V to 3.3V Operating Voltage

Flash

- 32-megabit (2M x 16)
- 2.7V to 3.3V Read/Write
- Access Time – 70 ns
- Sector Erase Architecture
  - Sixty-three 32K Word Sectors with Individual Write Lockout
  - Eight 4K Word Sectors with Individual Write Lockout
- Fast Word Program Time – 15 µs
- Suspend/Resume Feature for Erase and Program
  - Supports Reading and Programming from Any Sector by Suspending Erase of a Different Sector
  - Supports Reading Any Word by Suspending Programming of Any Other Word
- Low-power Operation
  - 12 mA Active
  - 13 µA Standby
- $\overline{\text{Data}}$ Polling, Toggle Bit, Ready/$\overline{\text{Busy}}$ for End of Program Detection
- $\overline{\text{VPP}}$ Pin for Write Protection and Accelerated Program/Erase Operations
- $\overline{\text{RESET}}$ Input for Device Initialization
- Sector Lockdown Support
- Top or Bottom Boot Block Configuration Available
- 128-bit Protection Register
- Minimum 100,000 Erase Cycles

PSRAM

- 8-megabit (512K x 16)
- 2.7V to 3.3V V_{CC}
- 70 ns Access Time
- Extended Temperature Range
- ISB0 < 10 µA when Deep Power-Down

Device Number	Flash Boot Location	Flash Plane Configuration	PSRAM Configuration
AT52BC3221A	Bottom	32M (2M x 16)	8M (512K x 16)
AT52BC3221AT	Top	32M (2M x 16)	8M (512K x 16)

32-Mbit Flash + 8-Mbit PSRAM Stack Memory

AT52BC3221A
AT52BC3221AT

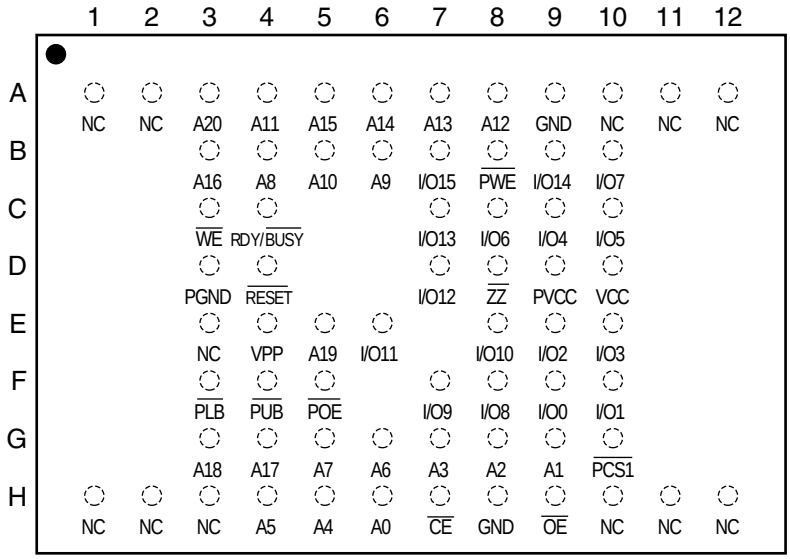
Preliminary

Rev. 3466A–STKD–11/04

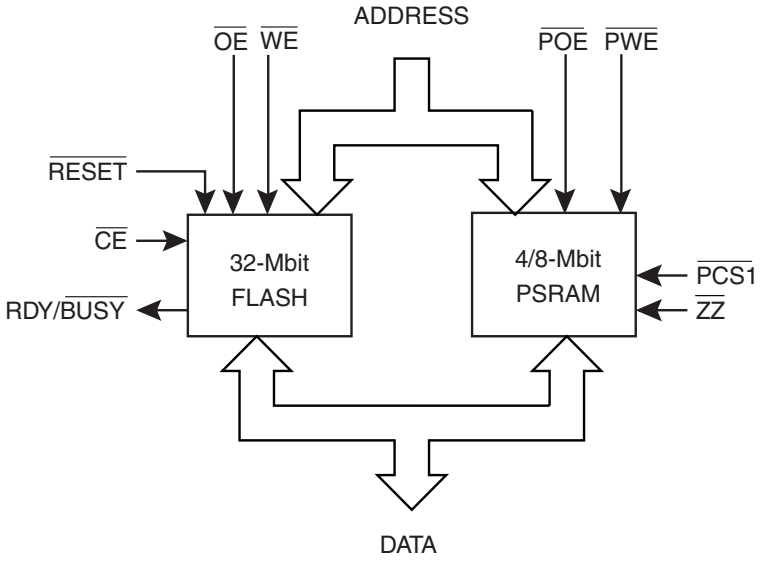
Pin Configuration

Pin Name	Function
A0 - A18, A19 - A20	Common Address Input for 8M PSRAM/Flash, Flash Address Input
$\overline{CE}$	Flash Chip Enable
$\overline{OE}$	Flash Output Enable
$\overline{WE}$	Flash Write Enable
$\overline{RESET}$	Flash Reset
RDY/$\overline{BUSY}$	Flash READY/$\overline{BUSY}$ Output
VPP	Flash Power Supply for Accelerated Program/Erase Operations
VCC	Flash Power
GND	Flash Ground
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect
$\overline{PLB}$	PSRAM Lower Byte
$\overline{PUB}$	PSRAM Upper Byte
PVCC	PSRAM Power
PGND	PSRAM Ground
$\overline{PCS1}$	PSRAM Chip Select 1
$\overline{ZZ}$	Low Power Modes
$\overline{PWE}$	PSRAM Write Enable
$\overline{POE}$	PSRAM Output Enable

CBGA (Top View)



Block Diagram



Description

The AT52BC3221A(T) combines a 32-megabit Flash (2M x 16) and an 8-megabit PSRAM (organized as 512K x 16) in a stacked 66-ball CBGA package. The stacked modules operate at 2.7V to 3.3V in the extended temperature range.

Absolute Maximum Ratings

Temperature under Bias	-25°C to +85°C
Storage Temperature	-55°C to +150°C
All Input Voltages except V_{PP} (including NC Pins) with Respect to Ground	-0.2V to V_{CC} +0.3V
Voltage on V_{PP} with Respect to Ground	-0.2V to + 6.25V
All Output Voltages with Respect to Ground	-0.2V to V_{CC} +0.3V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

Operating Temperature (Case)	-25°C - 85°C
V_{CC} Power Supply	2.7V to 3.3V

32-megabit Flash Memory Description

The 32-megabit Flash is a a 2.7-volt memory organized as 2,097,152 words of 16 bits each. The memory is divided into 71 sectors for erase operations. The device has $\overline{CE}$ and $\overline{OE}$ control signals to avoid any bus contention. This device can be read or reprogrammed using a single power supply, making it ideally suited for in-system programming.

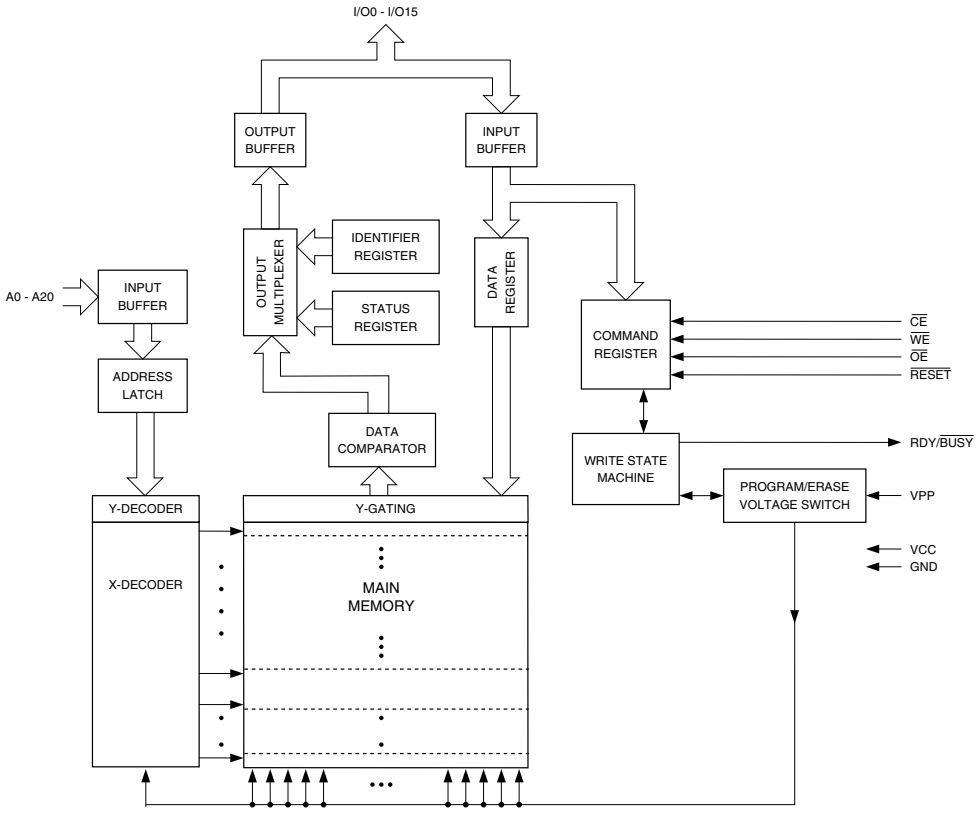
The device powers on in the read mode. Command sequences are used to place the device in other operation modes such as program and erase. The device has the capability to protect the data in any sector (see “Sector Lockdown” section).

To increase the flexibility of the device, it contains an Erase Suspend and Program Suspend feature. This feature will put the erase or program on hold for any amount of time and let the user read data from or program data to any of the remaining sectors within the memory. The end of a program or an erase cycle is detected by the READY/$\overline{BUSY}$ pin, $\overline{Data}$ Polling or by the toggle bit.

The VPP pin provides data protection. When the V_{PP} input is below 0.4V, the program and erase functions are inhibited. When V_{PP} is at 0.9V or above, normal program and erase operations can be performed.

A six-byte command (Enter Single Pulse Program Mode) sequence to remove the requirement of entering the three-byte program sequence is offered to further improve programming time. After entering the six-byte code, only single pulses on the write control lines are required for writing into the device. This mode (Single Pulse Word Program) is exited by powering down the device, or by pulsing the $\overline{RESET}$ pin low for a minimum of 500 ns and then bringing it back to V_{CC}. Erase, Erase Suspend/Resume and Program Suspend/Resume commands will not work while in this mode; if entered they will result in data being programmed into the device. It is not recommended that the six-byte code reside in the software of the final product but only exist in external programming code.

Block Diagram



Device Operation

READ: The 32-Mbit Flash memory is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on, it will be reset to the read or standby mode, depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the "Command Definition in Hex" table on page 12 (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the read or standby mode, depending upon the state of the control inputs.

ERASURE: Before a word can be reprogrammed, it must be erased. The erased state of memory bits is a logical "1". The entire device can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase command.

CHIP ERASE: The entire device can be erased at one time by using the six-byte chip erase software code. After the chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time to erase the chip is t_{EC}.

If the sector lockdown has been enabled, the chip erase will not erase the data in the sector that has been locked out; it will erase only the unprotected sectors. After the chip erase, the device will return to the read or standby mode.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into 71 sectors (SA0 - SA70) that can be individually erased. The Sector Erase command is a six-bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H data input command is latched on the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. The maximum time to erase a sector is t_{SEC}. When the sector programming lockdown feature is not enabled, the sector will erase (from the same Sector Erase command). An attempt to erase a sector that has been protected will result in the operation terminating immediately.

WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logical "0") on a word-by-word basis. Programming is accomplished via the internal device command register and is a four-bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after the specified t_{BP} cycle time. The $\overline{Data}$ Polling feature or the Toggle Bit feature may be used to indicate the end of a program cycle. If the erase/program status bit is a "1", the device was not able to verify that the erase or program operation was performed successfully.

VPP PIN: The circuitry of the 32-Mbit Flash is designed so that the device cannot be programmed or erased if the V_{PP} voltage is less that 0.4V. When V_{PP} is at 0.9V or above, normal program and erase operations can be performed. The VPP pin cannot be left floating.

PROGRAM/ERASE STATUS: The device provides several bits to determine the status of a program or erase operation: I/O2, I/O3, I/O5, I/O6 and I/O7. The "Status Bit Table" on page 11 and the following four sections describe the function of these bits. To provide greater flexibility for system designers, the device contains a programmable configuration register. The configuration register allows the user to specify the status bit operation. The configuration register can be set to one of two different values, "00" or "01". If the configuration register is set to "00", the part will automatically return to the read mode after a successful program or erase operation. If the configuration register is set to a "01", a Product ID Exit command must be given after a successful program or erase operation before the part will return to the read mode. It is important to note that whether the configuration register is set to a "00" or to a "01", any unsuccessful program or erase operation requires using the Product ID Exit command to return the device to read mode. The default value (after power-up) for the configuration register is "00". Using the four-bus cycle Set Configuration Register command as shown in the "Command Definition in Hex" table on page 12, the value of the configuration register can be changed. Voltages applied to the $\overline{\text{RESET}}$ pin will not alter the value of the configuration register. The value of the configuration register will affect the operation of the I/O7 status bit as described below.

$\overline{\text{DATA}}$ POLLING: The device features $\overline{\text{Data}}$ Polling to indicate the end of a program cycle. If the status configuration register is set to a "00", during a program cycle an attempted read of the last word loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a "0" on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{\text{Data}}$ Polling may begin at any time during the program cycle. Please see "Status Bit Table" on page 11 for more details.

If the status bit configuration register is set to a "01", the I/O7 status bit will be low while the device is actively programming or erasing data. I/O7 will go high when the device has completed a program or erase operation. Once I/O7 has gone high, status information on the other pins can be checked.

The $\overline{\text{Data}}$ Polling status bit must be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 1 and 2 on page 9.

TOGGLE BIT: In addition to $\overline{\text{Data}}$ Polling the device provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the memory will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle. Please see "Status Bit Table" on page 11 for more details.

The toggle bit status bit should be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 3 and 4 on page 10.

ERASE/PROGRAM STATUS BIT: The device offers a status bit on I/O5, which indicates whether the program or erase operation has exceeded a specified internal pulse count limit. If the status bit is a "1", the device is unable to verify that an erase or a word program operation has been successfully performed. If a program (Sector Erase) command is issued to a protected sector, the protected sector will not be programmed (erased). The device will go to a status read mode and the I/O5 status bit will be set high, indicating the program (erase) operation did not complete as requested. Once the erase/program status bit has been set to a "1", the system must write the Product ID Exit command to return to the read mode. The

erase/program status bit is a “0” while the erase or program operation is still in progress. Please see “Status Bit Table” on page 11 for more details.

V_{PP} STATUS BIT: The device provides a status bit on I/O3, which provides information regarding the voltage level of the VPP pin. During a program or erase operation, if the voltage on the VPP pin is not high enough to perform the desired operation successfully, the I/O3 status bit will be a “1”. Once the V_{PP} status bit has been set to a “1”, the system must write the Product ID Exit command to return to the read mode. On the other hand, if the voltage level is high enough to perform a program or erase operation successfully, the V_{PP} status bit will output a “0”. Please see “Status Bit Table” on page 11 for more details.

SECTOR LOCKDOWN: Each sector has a programming lockdown feature. This feature prevents programming of data in the designated sectors once the feature has been enabled. These sectors can contain secure code that is used to bring up the system. Enabling the lockdown feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; any sector’s usage as a write-protected region is optional to the user.

At power-up or reset, all sectors are unlocked. To activate the lockdown for a specific sector, the six-bus cycle Sector Lockdown command must be issued. Once a sector has been locked down, the contents of the sector is read-only and cannot be erased or programmed.

SECTOR LOCKDOWN DETECTION: A software method is available to determine if programming of a sector is locked down. When the device is in the software product identification mode (see “Software Product Identification Entry/Exit” sections on page 24), a read from address location 00002H within a sector will show if programming the sector is locked down. If the data on I/O0 is low, the sector can be programmed; if the data on I/O0 is high, the program lockdown feature has been enabled and the sector cannot be programmed. The software product identification exit code should be used to return to standard operation.

SECTOR LOCKDOWN OVERRIDE: The only way to unlock a sector that is locked down is through reset or power-up cycles. After power-up or reset, the content of a sector that is locked down can be erased and reprogrammed.

ERASE SUSPEND/ERASE RESUME: The Erase Suspend command allows the system to interrupt a sector or chip erase operation and then program or read data from a different sector within the memory. After the Erase Suspend command is given, the device requires a maximum time of 15 µs to suspend the erase operation. After the erase operation has been suspended, the system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one-bus cycle command. The device also supports an erase suspend during a complete chip erase. While the chip erase is suspended, the user can read from any sector within the memory that is protected. The command sequence for a chip erase suspend and a sector erase suspend are the same.

PROGRAM SUSPEND/PROGRAM RESUME: The Program Suspend command allows the system to interrupt a programming operation and then read data from a different word within the memory. After the Program Suspend command is given, the device requires a maximum of 20 µs to suspend the programming operation. After the programming operation has been suspended, the system can then read data from any other word within the device that is not contained in the sector in which the programming operation was suspended. An address is not required during the program suspend operation. To resume the programming operation, the system must write the Program Resume command. The program suspend and resume are one-bus cycle commands. The command sequence for the erase suspend and program suspend are the same, and the command sequence for the erase resume and program resume are the same.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see "Operating Modes" on page 17 (for hardware operation) or "Software Product Identification Entry/Exit" sections on page 24. The manufacturer and device codes are the same for both modes.

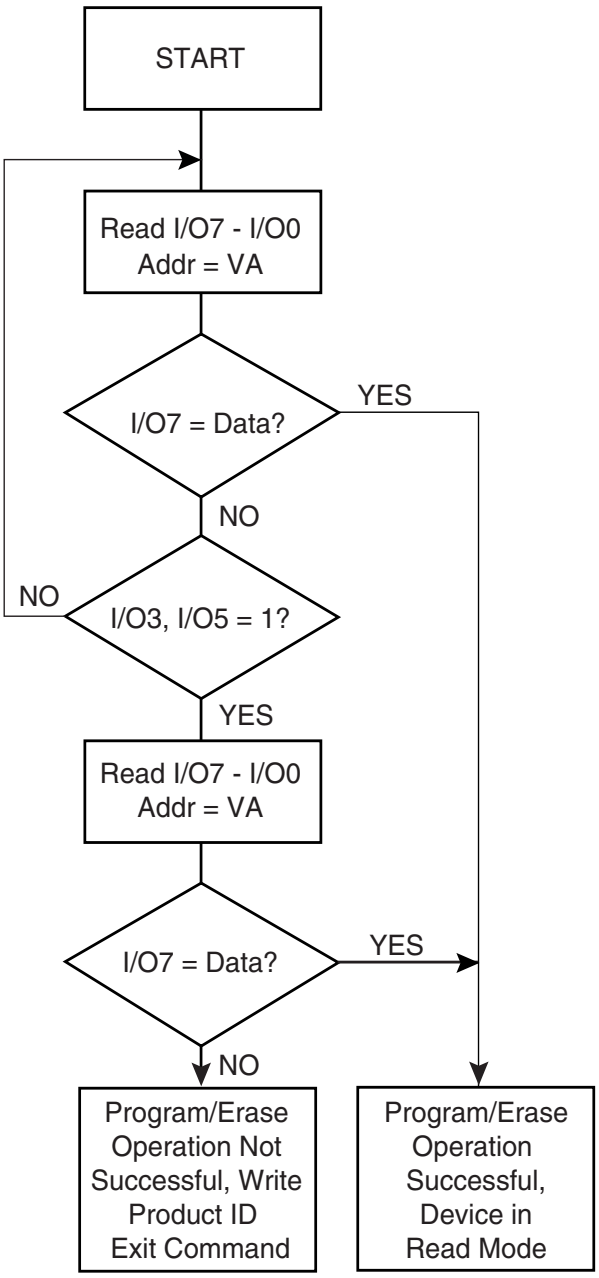
128-BIT PROTECTION REGISTER: The device contains a 128-bit register that can be used for security purposes in system design. The protection register is divided into two 64-bit blocks. The two blocks are designated as block A and block B. The data in block A is non-changeable and is programmed at the factory with a unique number. The data in block B is programmed by the user and can be locked out such that data in the block cannot be reprogrammed. To program block B in the protection register, the four-bus cycle Program Protection Register command must be used as shown in the "Command Definition in Hex" table on page 12. To lock out block B, the four-bus cycle Lock Protection Register command must be used as shown in the "Command Definition in Hex" table. Data bit D1 must be zero during the fourth bus cycle. All other data bits during the fourth bus cycle are don't cares. To determine whether block B is locked out, the Product ID Entry command is given followed by a read operation from address 80H. If data bit D1 is zero, block B is locked. If data bit D1 is one, block B can be reprogrammed. Please see the "Protection Register Addressing Table" on page 12 for the address locations in the protection register. To read the protection register, the Product ID Entry command is given followed by a normal read operation from an address within the protection register. After determining whether block B is protected or not, or reading the protection register, the Product ID Exit command must be given prior to performing any other operation.

RDY/$\overline{\text{BUSY}}$: For the 32-Mbit Flash memory, an open-drain READY/$\overline{\text{BUSY}}$ output pin provides another method of detecting the end of a program or erase operation. RDY/$\overline{\text{BUSY}}$ is actively pulled low during the internal program and erase cycles and is released at the completion of the cycle. The open-drain connection allows for OR-tying of several devices to the same RDY/$\overline{\text{BUSY}}$ line. Please see "Status Bit Table" on page 11 for more details.

HARDWARE DATA PROTECTION: The Hardware Data Protection feature protects against inadvertent programs to the device in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power-on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (d) Program inhibit: V_{PP} is less than V_{ILPP}. (e) V_{PP} power-on delay: once V_{PP} has reached 1.65V, program and erase operations are inhibited for 100 ns.

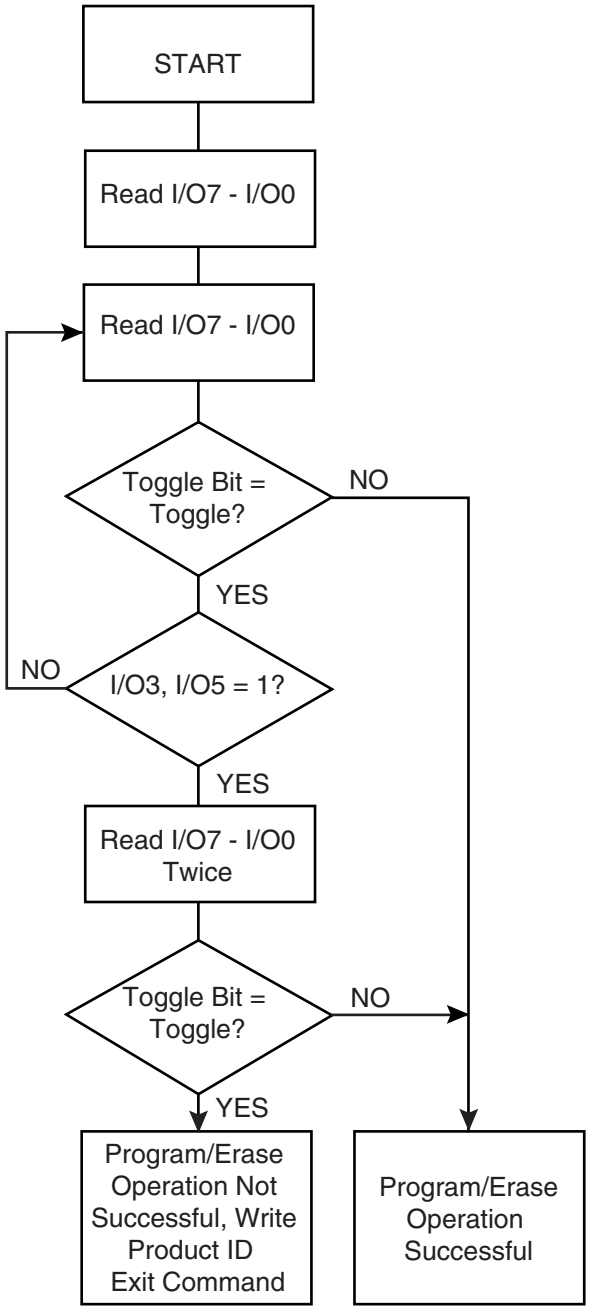
INPUT LEVELS: While operating with a 2.7V to 3.3V power supply, the address inputs and control inputs ($\overline{\text{OE}}$, $\overline{\text{CE}}$ and $\overline{\text{WE}}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CC} + 0.3V.

Figure 1. $\overline{\text{Data}}$ Polling Algorithm
(Configuration Register = 00)



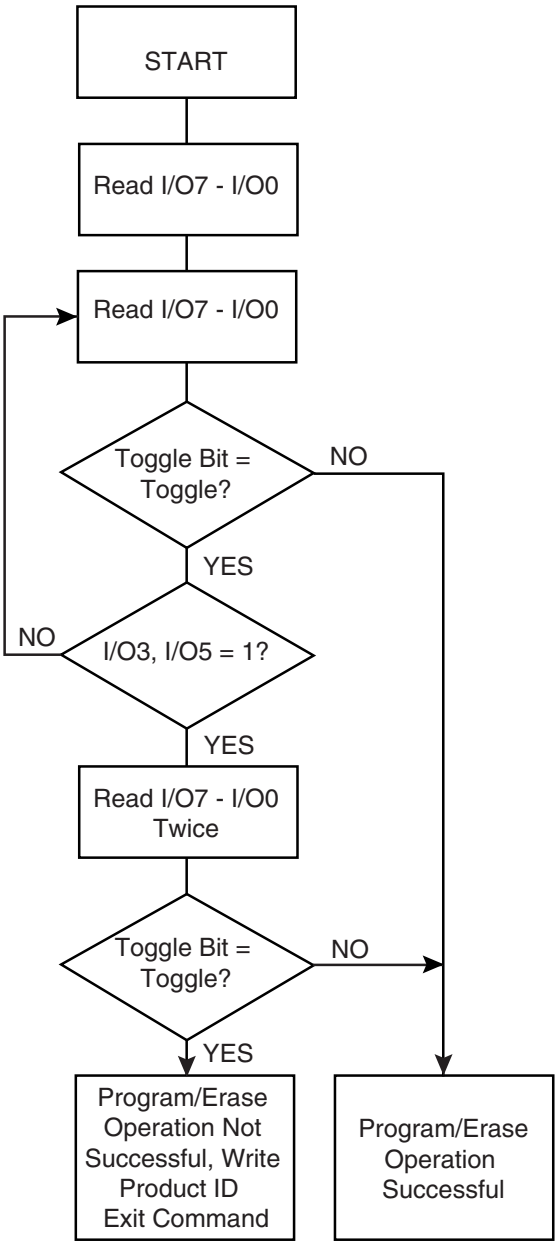
Notes: 1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
2. I/O7 should be rechecked even if I/O5 = "1" because I/O7 may change simultaneously with I/O5.

Figure 2. $\overline{\text{Data}}$ Polling Algorithm
(Configuration Register = 01)



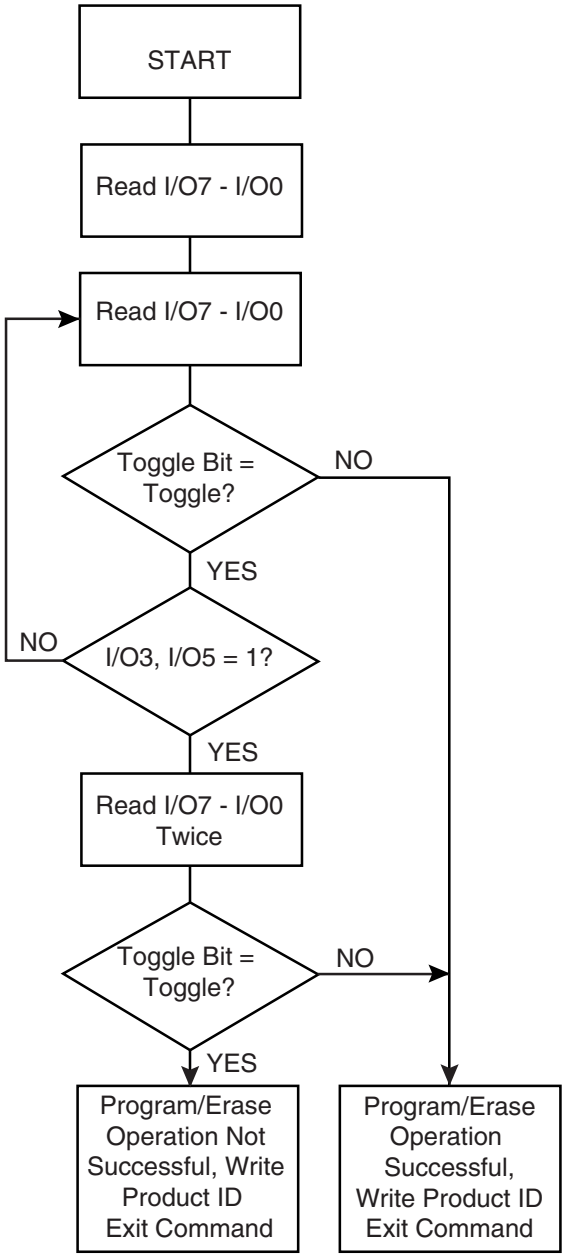
Note: 1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.

Figure 3. Toggle Bit Algorithm (Configuration Register = 00)



Note: 1. The system should recheck the toggle bit even if I/O5 = "1" because the toggle bit may stop toggling as I/O5 changes to "1".

Figure 4. Toggle Bit Algorithm (Configuration Register = 01)



Note: 1. The system should recheck the toggle bit even if I/O5 = "1" because the toggle bit may stop toggling as I/O5 changes to "1".

Status Bit Table

	Status Bit						
	I/O7	I/O7	I/O6	I/O5[1]	I/O3[2]	I/O2	RDY/$\overline{\text{BUSY}}$
Configuration Register	**00**	**01**	**00/01**	**00/01**	**00/01**	**00/01**	**00/01**
Programming	$\overline{\text{I/O7}}$	0	TOGGLE	0	0	1	0
Erasing	0	0	TOGGLE	0	0	TOGGLE	0
Erase Suspended & Read Erasing Sector	1	1	1	0	0	TOGGLE	1
Erase Suspended & Read Non-erasing Sector	DATA	DATA	DATA	DATA	DATA	DATA	1
Erase Suspended & Program Non-erasing Sector	$\overline{\text{I/O7}}$	0	TOGGLE	0	0	TOGGLE	0

Notes: 1. I/O5 switches to a “1” when a program or an erase operation has exceeded the maximum time limits or when a program or sector erase operation is performed on a protected sector.
2. I/O3 switches to a “1” when the V_{PP} level is not high enough to successfully perform program and erase operations.

Command Definition in Hex[1]

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	555	AA	AAA[2]	55	555	80	555	AA	AAA	55	555	10
Sector Erase	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA[3][4]	30
Word Program	4	555	AA	AAA	55	555	A0	Addr	D_{IN}				
Enter Single Pulse Program Mode	6	555	AA	AAA	55	555	80	555	AA	AAA	55	555	A0
Single Pulse Word Program	1	Addr	D_{IN}										
Sector Lockdown	6	555	AA	AAA[2]	55	555	80	555	AA	AAA	55	SA[3][4]	60
Erase/Program Suspend	1	XXX	B0										
Erase/Program Resume	1	XXX	30										
Product ID Entry	3	555	AA	AAA	55	555	90						
Product ID Exit[5]	3	555	AA	AAA	55	555	F0[8]						
Product ID Exit[5]	1	XXX	F0[8]										
Program Protection Register	4	555	AA	AAA	55	555	C0	Addr	D_{IN}				
Lock Protection Register - Block B	4	555	AA	AAA	55	555	C0	80	X0				
Status of Block B Protection	4	555	AA	AAA	55	555	90	80	D_{OUT}[6]				
Set Configuration Register	4	555	AA	AAA	55	555	D0	XXX	00/01[7]				

Notes:
1. The DATA FORMAT shown for each bus cycle is as follows; I/O7 - I/O0 (Hex). In word operation I/O15 - I/O8 are don't care. The ADDRESS FORMAT shown for each bus cycle is as follows: A11 - A0 (Hex). Address A20 through A11 are don't care in the word mode.
2. Since A11 is a Don't Care, AAA can be replaced with 2AA.
3. SA = sector address. Any word address within a sector can be used to designate the sector address (see pages 15-17 for details).
4. Once a sector is in the lockdown mode, data in the protected sector cannot be changed unless the chip is reset or power cycled.
5. Either one of the Product ID Exit commands can be used.
6. If data bit D1 is "0", block B is locked. If data bit D1 is "1", block B can be reprogrammed.
7. The default state (after power-up) of the configuration register is "00".
8. Bytes of data other than F0 may be used to exit the Product ID mode. However, it is recommended that F0 be used.

Protection Register Addressing Table

Word	Use	Block	A7	A6	A5	A4	A3	A2	A1	A0
0	Factory	A	1	0	0	0	0	0	0	1
1	Factory	A	1	0	0	0	0	0	1	0
2	Factory	A	1	0	0	0	0	0	1	1
3	Factory	A	1	0	0	0	0	1	0	0
4	User	B	1	0	0	0	0	1	0	1
5	User	B	1	0	0	0	0	1	1	0
6	User	B	1	0	0	0	0	1	1	1
7	User	B	1	0	0	0	1	0	0	0

Note: All address lines not specified in the above table must be "0" when accessing the protection register, i.e., A20 - A8 = 0.

Bottom Boot – Sector Address Table

Sector	x16 Address Range (A20 - A0)
SA0	00000 - 00FFF
SA1	01000 - 01FFF
SA2	02000 - 02FFF
SA3	03000 - 03FFF
SA4	04000 - 04FFF
SA5	05000 - 05FFF
SA6	06000 - 06FFF
SA7	07000 - 07FFF
SA8	08000 - 0FFFF
SA9	10000 - 17FFF
SA10	18000 - 1FFFF
SA11	20000 - 27FFF
SA12	28000 - 2FFFF
SA13	30000 - 37FFF
SA14	38000 - 3FFFF
SA15	40000 - 47FFF
SA16	48000 - 4FFFF
SA17	50000 - 57FFF
SA18	58000 - 5FFFF
SA19	60000 - 67FFF
SA20	68000 - 6FFFF
SA21	70000 - 77FFF
SA22	78000 - 7FFFF
SA23	80000 - 87FFF
SA24	88000 - 8FFFF
SA25	90000 - 97FFF
SA26	98000 - 9FFFF
SA27	A0000 - A7FFF
SA28	A8000 - AFFFF
SA29	B0000 - B7FFF
SA30	B8000 - BFFFF
SA31	C0000 - C7FFF
SA32	C8000 - CFFFF
SA33	D0000 - D7FFF
SA34	D8000 - DFFFF
SA35	E0000 - E7FFF
SA36	E8000 - EFFFF

Bottom Boot – Sector Address Table (Continued)

Sector	x16 Address Range (A20 - A0)
SA37	F0000 - F7FFF
SA38	F8000 - FFFFF
SA39	100000 - 107FFF
SA40	108000 - 10FFFF
SA41	110000 - 117FFF
SA42	118000 - 11FFFF
SA43	120000 - 127FFF
SA44	128000 - 12FFFF
SA45	130000 - 137FFF
SA46	138000 - 13FFFF
SA47	140000 - 147FFF
SA48	148000 - 14FFFF
SA49	150000 - 157FFF
SA50	158000 - 15FFFF
SA51	160000 - 167FFF
SA52	168000 - 16FFFF
SA53	170000 - 177FFF
SA54	178000 - 17FFFF
SA55	180000 - 187FFF
SA56	188000 - 18FFFF
SA57	190000 - 197FFF
SA58	198000 - 19FFFF
SA59	1A0000 - 1A7FFF
SA60	1A8000 - 1AFFFF
SA61	1B0000 - 1B7FFF
SA62	1B8000 - 1BFFFF
SA63	1C0000 - 1C7FFF
SA64	1C8000 - 1CFFFF
SA65	1D0000 - 1D7FFF
SA66	1D8000 - 1DFFFF
SA67	1E0000 - 1E7FFF
SA68	1E8000 - 1EFFFF
SA69	1F0000 -1F7FFF
SA70	1F8000 - 1FFFF

Top Boot – Sector Address Table

Sector	x16 Address Range (A20 - A0)
SA0	00000 - 07FFF
SA1	08000 - 0FFFF
SA2	10000 - 17FFF
SA3	18000 - 1FFFF
SA4	20000 - 27FFF
SA5	28000 - 2FFFF
SA6	30000 - 37FFF
SA7	38000 - 3FFFF
SA8	40000 - 47FFF
SA9	48000 - 4FFFF
SA10	50000 - 57FFF
SA11	58000 - 5FFFF
SA12	60000 - 67FFF
SA13	68000 - 6FFFF
SA14	70000 - 77FFF
SA15	78000 - 7FFFF
SA16	80000 - 87FFF
SA17	88000 - 8FFFF
SA18	90000 - 97FFF
SA19	98000 - 9FFFF
SA20	A0000 - A7FFF
SA21	A8000 - AFFFF
SA22	B0000 - B7FFF
SA23	B8000 - BFFFF
SA24	C0000 - C7FFF
SA25	C8000 - CFFFF
SA26	D0000 - D7FFF
SA27	D8000 - DFFFF
SA28	E0000 - E7FFF
SA29	E8000 - EFFFF
SA30	F0000 - F7FFF
SA31	F8000 - FFFFF
SA32	100000 - 107FFF
SA33	108000 - 10FFFF
SA34	110000 - 117FFF
SA35	118000 - 11FFFF
SA36	120000 - 127FFF

Top Boot – Sector Address Table (Continued)

Sector	x16 Address Range (A20 - A0)
SA37	128000 - 12FFFF
SA38	130000 - 137FFF
SA39	138000 - 13FFFF
SA40	140000 - 147FFF
SA41	148000 - 14FFFF
SA42	150000 - 157FFF
SA43	158000 - 15FFFF
SA44	160000 - 167FFF
SA45	168000 - 16FFFF
SA46	170000 - 177FFF
SA47	178000 - 17FFFF
SA48	180000 - 187FFF
SA49	188000 - 18FFFF
SA50	190000 - 197FFF
SA51	198000 - 19FFFF
SA52	1A0000 - 1A7FFF
SA53	1A8000 - 1AFFFF
SA54	1B0000 - 1B7FFF
SA55	1B8000 - 1BFFFF
SA56	1C0000 - 1C7FFF
SA57	1C8000 - 1CFFFF
SA58	1D0000 - 1D7FFF
SA59	1D8000 - 1DFFFF
SA60	1E0000 - 1E7FFF
SA61	1E8000 - 1EFFFF
SA62	1F0000 - 1F7FFF
SA63	1F8000 - 1F8FFF
SA64	1F9000 - 1F9FFF
SA65	1FA000 - 1FAFFF
SA66	1FB000 - 1FBFFF
SA67	1FC000 - 1FCFFF
SA68	1FD000 - 1FDFFF
SA69	1FE000 - 1FEFFF
SA70	1FF000 - 1FFFFF

DC and AC Operating Range

	32-Mbit Flash
Operating Temperature (Case)	-25°C to 85°C
V_{CC} Power Supply	2.7V to 3.3V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	V_{PP}	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Ai	D_{OUT}
Program/Erase[2]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IHPP}[6]	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X[1]	X	V_{IH}	X	X	High-Z
Program Inhibit	X	X	V_{IH}	V_{IH}	X		
	X	V_{IL}	X	V_{IH}	X		
	X	X	X	V_{IH}	V_{ILPP}[7]		
Output Disable	X	V_{IH}	X	V_{IH}	X		High-Z
Reset	X	X	X	V_{IL}	X	X	High-Z
Product Identification							
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}		A1 - A20 = V_{IL}, A9 = V_H[3], A0 = V_{IL}	Manufacturer Code[4]
						A1 - A20 = V_{IL}, A9 = V_H[3], A0 = V_{IH}	Device Code[4]
Software[5]				V_{IH}		A0 = V_{IL}, A1 - A20 = V_{IL}	Manufacturer Code[4]
						A0 = V_{IH}, A1 - A20 = V_{IL}	Device Code[4]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC programming waveforms on page 22.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 001FH (x16), Device Code: 00C8H (x16)-Bottom Boot; 00C9H (x16)-Top Boot.
5. See details under “Software Product Identification Entry/Exit” on page 24.
6. V_{IHPP} (min) = 0.9V; V_{IHPP} (max) = 3.6V.
7. V_{ILPP} (max) = 0.4V.

DC Characteristics

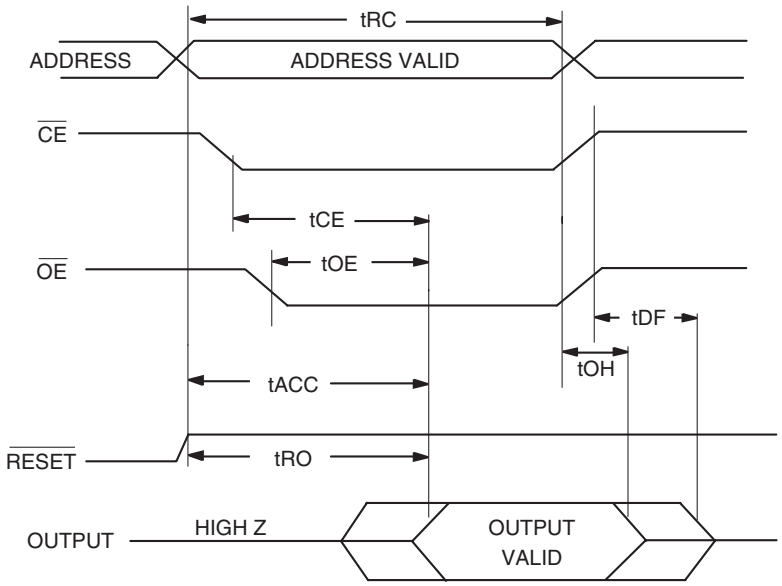
Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		13	25	µA
I_{CC}[1]	V_{CC} Active Read Current	f = 5 MHz; I_{OUT} = 0 mA		12	25	mA
I_{CC1}	V_{CC} Programming Current				45	mA
I_{PP1}	V_{PP} Input Load Current				10	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OL2}	Output Low Voltage	I_{OL} = 1.0 mA			0.20	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA V_{CCQ} < 2.6V I_{OH} = -400 µA $V_{CCQ} \geq$ 2.6V I_{OH} = -400 µA	V_{CCQ} - 0.2 2.4 2.4			V V V
V_{OH2}	Output High Voltage	I_{OH} = -100 µA V_{CCQ} < 2.6V I_{OH} = -100 µA $V_{CCQ} \geq$ 2.6V I_{OH} = -100 µA	V_{CCQ} - 0.1 2.5 2.5			V V V

Note: 1. In the erase mode, I_{CC} is 65 mA.

AC Read Characteristics

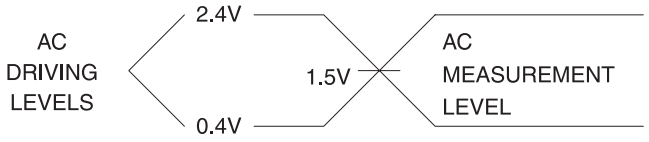
Symbol	Parameter	32-Mbit Flash		Units
		Min	Max	
t_{RC}	Read Cycle Time	70		ns
t_{ACC}	Address to Output Delay		70	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		70	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	40	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns
t_{RO}	$\overline{RESET}$ to Output Delay		100	ns

AC Read Waveforms[1][2][3][4]



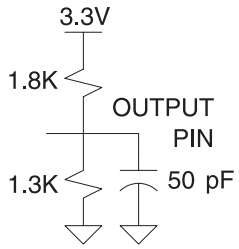
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

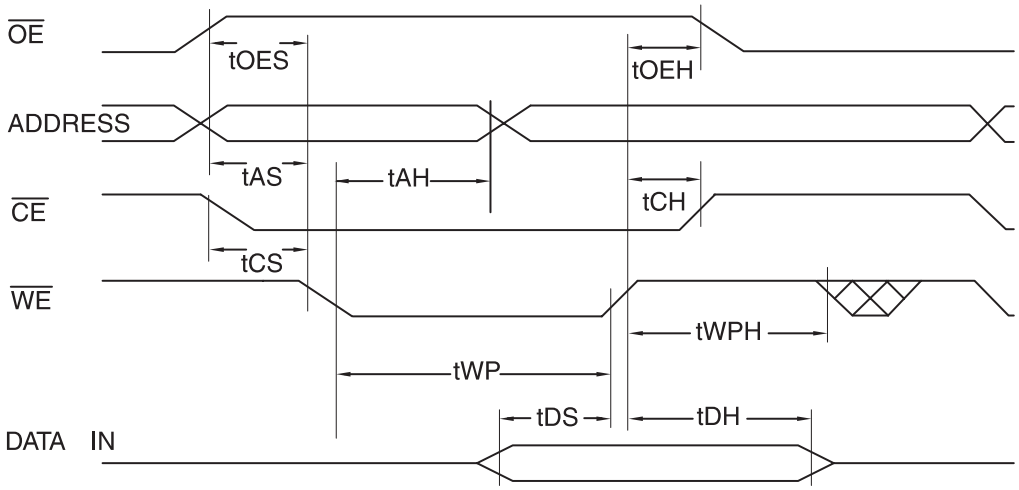
Note: This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

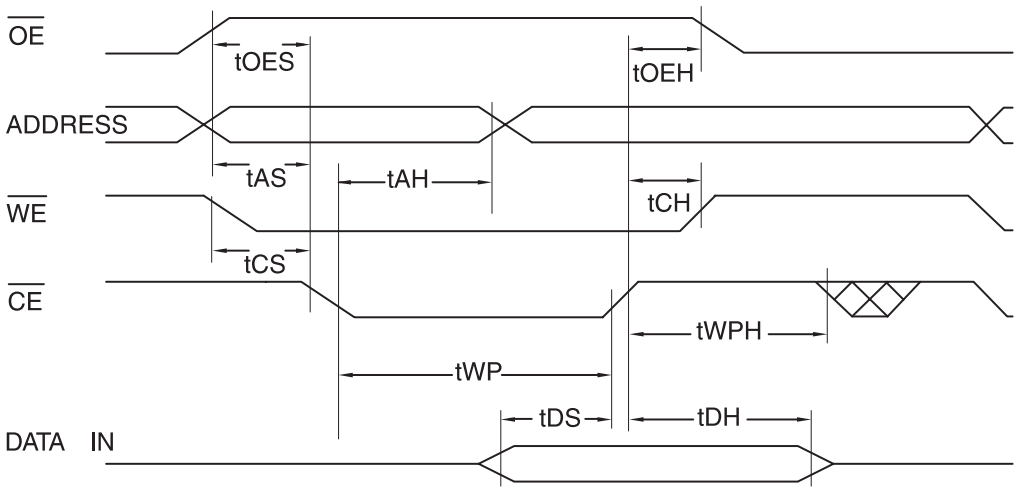
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	0		ns
t_{AH}	Address Hold Time	35		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	35		ns
t_{DS}	Data Setup Time	35		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	35		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled



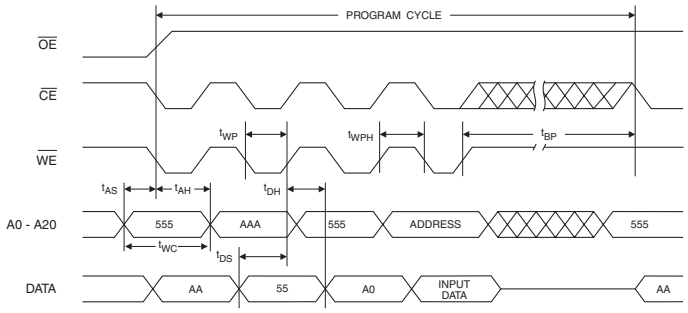
$\overline{CE}$ Controlled



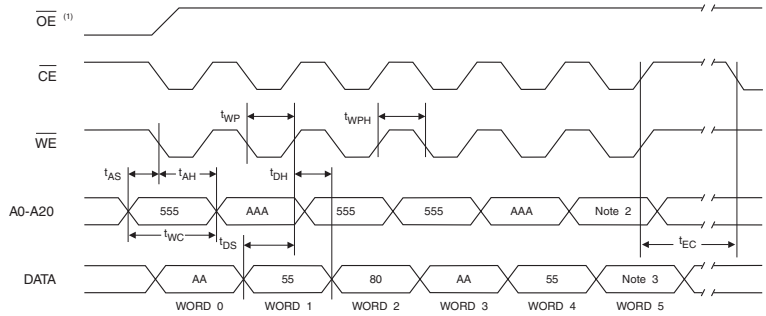
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Word Programming Time		15	150	µs
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	35			ns
t_{DS}	Data Setup Time	35			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	35			ns
t_{WPH}	Write Pulse Width High	35			ns
t_{WC}	Write Cycle Time	70			ns
t_{RP}	$\overline{\text{Reset}}$ Pulse Width	500			ns
t_{EC}	Chip Erase Cycle Time		80	400	seconds
t_{SEC1}	Sector Erase Cycle Time (4K Word Sectors)		0.3	3.0	seconds
t_{SEC2}	Sector Erase Cycle Time (32K Word Sectors)		1.2	5.0	seconds
t_{ES}	Erase Suspend Time			15	µs
t_{PS}	Program Suspend Time			20	µs

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



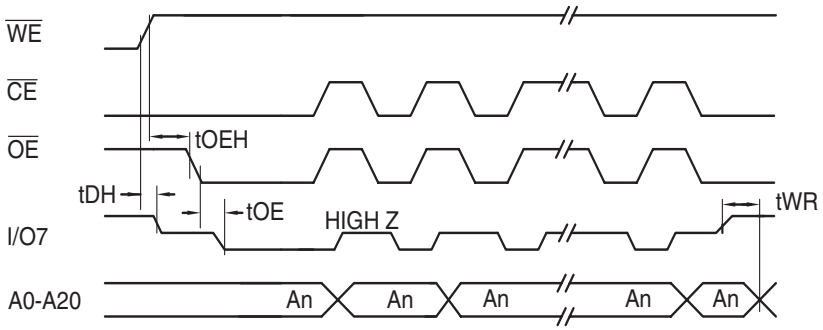
Notes:
1. $\overline{\text{OE}}$ must be high only when $\overline{\text{WE}}$ and $\overline{\text{CE}}$ are both low.
2. For chip erase, the address should be 555. For sector erase, the address depends on what sector is to be erased. (See note 3 under “Command Definitions in Hex” on page 12.)
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

$\overline{\text{Data}}$ Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 19.

$\overline{\text{Data}}$ Polling Waveforms

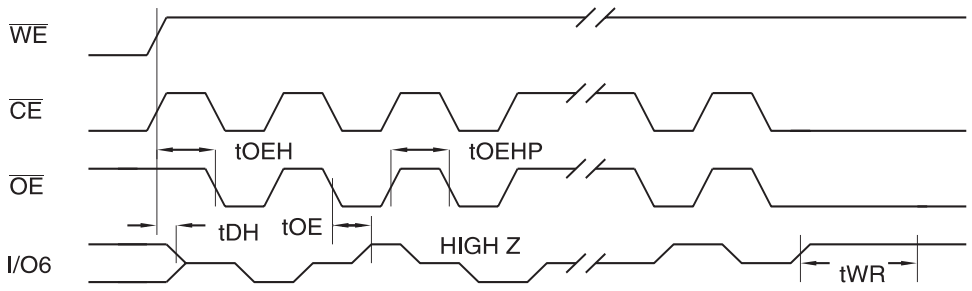


Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	50			ns
t_{WR}	Write Recovery Time	0			ns

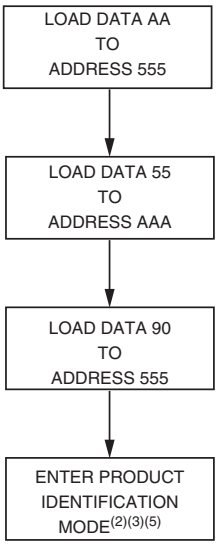
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 19.

Toggle Bit Waveforms(1)(2)(3)

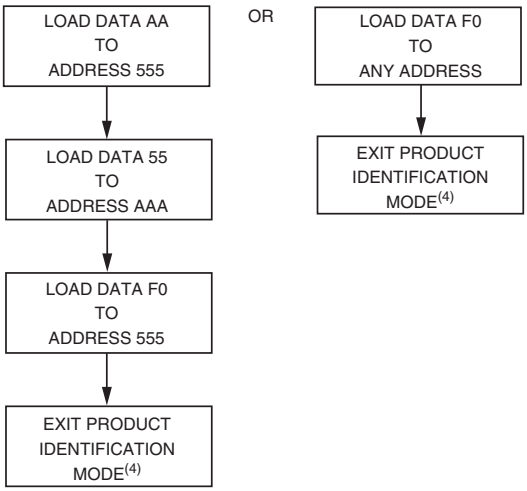


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry[1]

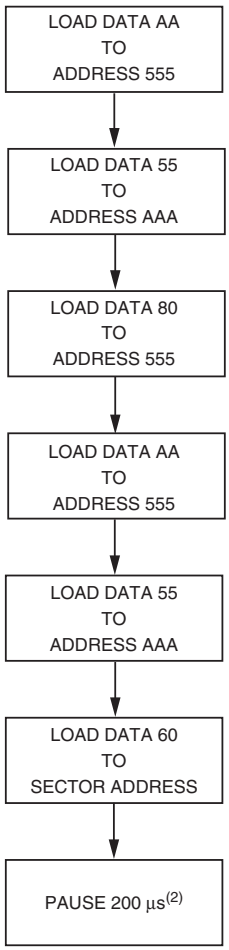


Software Product Identification Exit[1][6]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex) Address Format: A11 - A0 (Hex), and A11 - A20 (Don't Care).
2. A1 - A20 = V_{IL}. Manufacturer Code is read for A0 = V_{IL}; Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 001FH(x16)
   Device Code: 00C8 (x16)-Bottom Boot
   00C9H (x16)-Top Boot.
6. Either one of the Product ID Exit commands can be used.

Sector Lockdown Enable Algorithm[1]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex) Address Format: A11 - A0 (Hex), A-1, and A11 - A20 (Don't Care).
2. Sector Lockdown feature enabled.

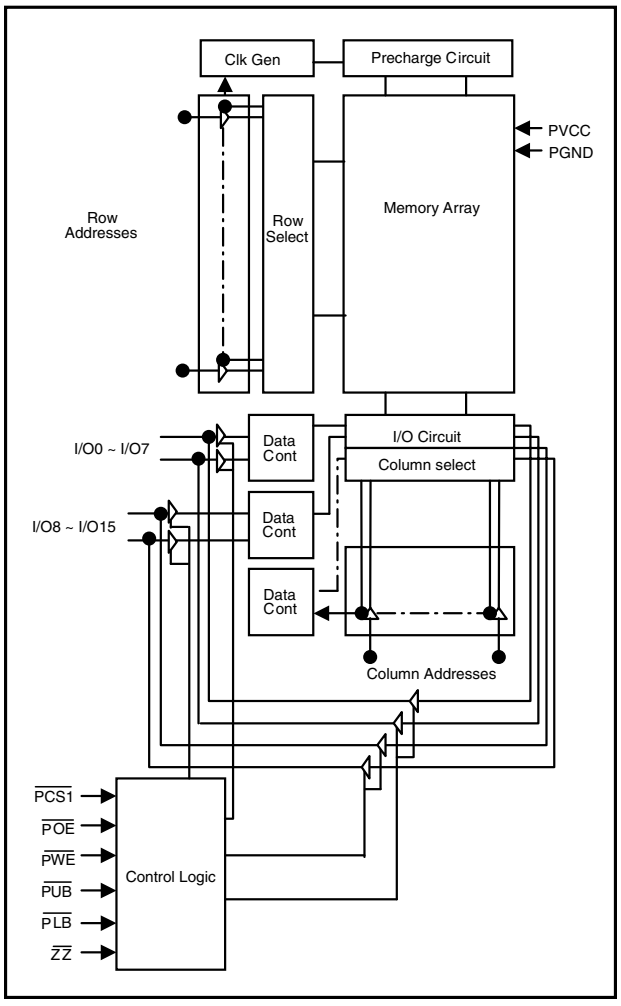
PSRAM Description

The Pseudo-SRAM (PSRAM) is an integrated memory based on a self-refresh DRAM array. The device is offered with density of 8-Mbit organized as 512,288 words by 16 bits. It is designed to be identical in operation and interface to the standard 6T SRAMS. The device is designed for low standby, low operating current and includes a user configurable low-power mode. Two chip selects ($\overline{PCS1}$ and $\overline{ZZ}$) and an output enable ($\overline{POE}$) is available to allow for easy memory expansion. Byte controls ($\overline{PUB}$ and $\overline{PLB}$) allow the upper and lower bytes to be accessed independently and can also be used to deselect the device. The deep sleep mode reduces standby current drain while not retaining data in the array.

PSRAM Features

- **Fast Cycle Times**
  - **T_{ACC} < 70 ns**
- **Very Low Standby Current**
  - **I_{SB0} < 10 µA @ 3.0V**
- **Very Low Operating Current**
  - **1.0 mA at 3.0 and 1 µs (Typical)**
- **Memory Expansion with $\overline{PCS1}$ and $\overline{POE}$**
- **TTL Compatible Three-state Output Driver**

Functional Block Diagram



Functional Description

$\overline{PCS1}$	$\overline{ZZ}$	$\overline{POE}$	$\overline{PWE}$	$\overline{PLB}$	$\overline{PUB}$	I/O0 - 7	I/O8 - 15	Mode	Power
H	H	X(1)	X(1)	X(1)	X(1)	High-Z	High-Z	Deselected	Standby
X(1)	L	X(1)	X(1)	X(1)	X(1)	High-Z	High-Z	Deselected	Low-power Modes
X(1)	H	X(1)	X(1)	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X(1)	High-Z	High-Z	Output Disabled	Active
	H	H	H	X(1)	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	D_{OUT}	High-Z	Lower Byte Read	Active
				H	L	High-Z	D_{OUT}	Upper Byte Read	Active
				L	L	D_{OUT}	D_{OUT}	Word Read	Active
		X(1)	L	L	H	D_{IN}	High-Z	Lower Byte Write	Active
				H	L	High-Z	D_{IN}	Upper Byte Write	Active
				L	L	D_{IN}	D_{IN}	Word Write	Active

Note: 1. X means don't care (must be low or high state).

Recommended DC Operating Conditions(1)(2)

Item	Symbol	Min	Max	Unit
Supply Voltage	PV_{CC}	2.7	3.3	V
Ground	PGND	0	0	V
Input High Voltage	V_{IH}	0.8 PV_{CC}	PV_{CC} + 0.2(3)	V
Input Low Voltage	V_{IL}	-0.2(4)	0.2 PV_{CC}	V

Notes: 1. T_A = - 25°C to 85°C, otherwise specified.
2. Overshoot and undershoot are sampled, not 100% tested.
3. Overshoot: PV_{CC} + 1.0V in case of pulse width ≤ 20 ns.
4. Undershoot: -1.0V in case of pulse width ≤ 20 ns.

Capacitance(1) (f = 1 MHz, T_A = 25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V		8	pF

Note: 1. Capacitance is sampled, not 100% tested.

DC and Operating Characteristics

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = PGND to PV_{CC}	-1		1	µA
Output Leakage Current	I_{LO}	$\overline{PCS1}$ = V_{IH}, $\overline{ZZ}$ = V_{IH}, $\overline{POE}$ = V_{IH} or $\overline{PWE}$ = V_{IL}, $V_{I/O}$ = PGND to PV_{CC}	-1		1	µA
Average Operating Current	I_{CC1}	Cycle time = 1 µs, 100% duty, $I_{I/O}$ = 0 mA, $\overline{PCS1} \leq 0.2V$, $\overline{ZZ}$ = V_{IH}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq PV_{CC}$ - 0.2V		1	3	mA
	I_{CC2}	Cycle time = Min, $I_{I/O}$ = 0 mA, 100% duty, $\overline{PCS1}$ = V_{IL}, $\overline{ZZ}$ = V_{IH}, V_{IN} = V_{IL} or V_{IH}			25	mA
Output Low Voltage	V_{OL}	I_{OL} = 0.5 mA			0.2 PV_{CC}	V
Output High Voltage	V_{OH}	I_{OH} = -0.5 mA	0.8 PV_{CC}			V
Standby Current (TTL)	I_{SB}	$\overline{PCS1}$ = V_{IH}, $\overline{ZZ}$ = V_{IH}, other inputs = V_{IH} or V_{IL}			0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{PCS1} \geq PV_{CC}$ -0.2V, $\overline{ZZ} \geq PV_{CC}$ - 0.2V, other inputs = 0 ~ PV_{CC}			70	µA
Low Power Modes	I_{SB0}	$\overline{ZZ} \leq 0.2V$, other inputs = 0 ~ PV_{CC}, no refresh (DPD)			10	µA

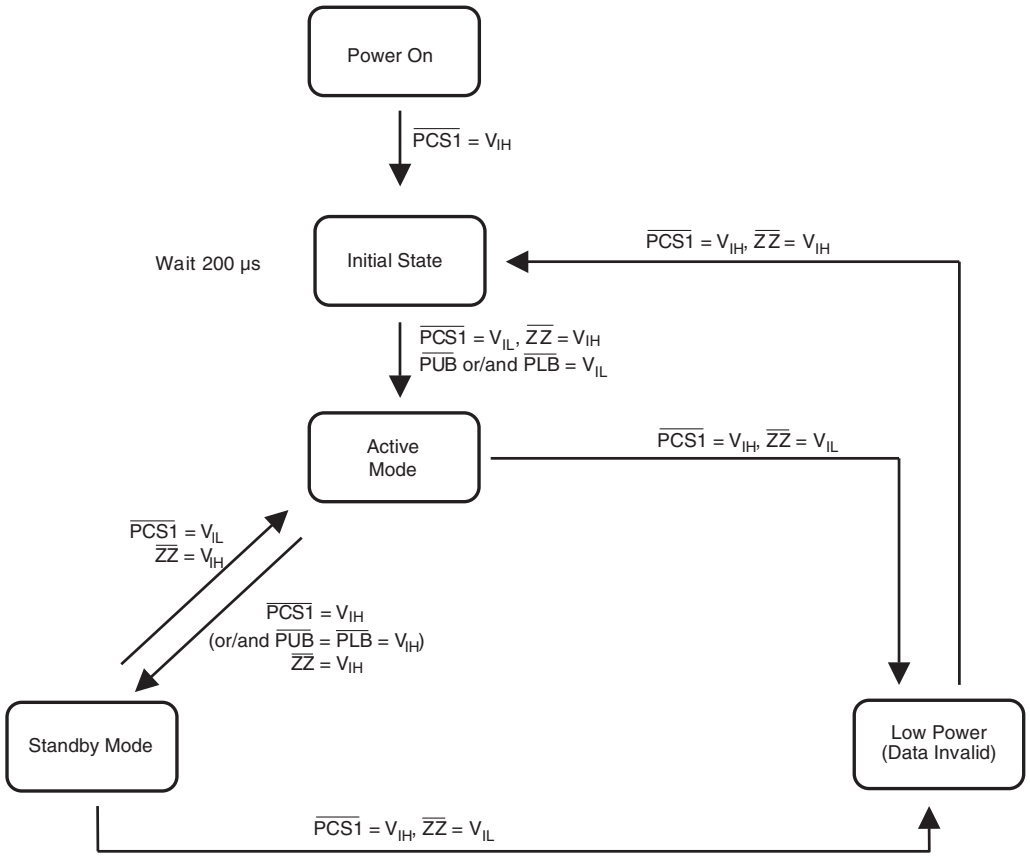
AC Characteristics (PV_{CC} = 2.7V – 3.3V, T_A = -25°C to 85°C)

Parameter List		Symbol	Speed Bins		Unit
			70 ns		
			Min	Max	
Read	Read Cycle Time	t_{RC}	70	40K	ns
	Address Access Time	t_{AA}		70	ns
	Chip Select to Output	t_{CO}		70	ns
	Output Enable to Valid Output	t_{OE}		25	ns
	$\overline{PUB}$, $\overline{PLB}$ Access Time	t_{BA}		70	ns
	Chip Select to Low-Z Output	t_{LZ}	10		ns
	$\overline{PUB}$, $\overline{PLB}$ Enable to Low-Z Output	t_{BLZ}	10		ns
	Output Enable to Low-Z Output	t_{OLZ}	5		ns
	Chip Disable to High-Z Output	t_{HZ}	0	5	ns
	$\overline{PUB}$, $\overline{PLB}$ Disable to High-Z Output	t_{BHZ}	0	5	ns
	Output Disable to High-Z Output	t_{OHZ}	0	5	ns
	Output Hold from Address Change	t_{OH}	5		ns
Write	Write Cycle Time	t_{WC}	70	40K	ns
	Chip Select to End of Write	t_{CW}	60		ns
	Address Set-up Time	t_{AS}	0		ns
	Address Valid to End of Write	t_{AW}	60		ns
	$\overline{PUB}$, $\overline{PLB}$ Valid to End of Write	t_{BW}	60		ns
	Write Pulse Width	t_{WP}	50		ns
	Write Recovery Time	t_{WR}	0		ns
	Write to Output High-Z	t_{WHZ}	0	5	ns
	Data to Write Time Overlap	t_{DW}	20		ns
	Data Hold from Write Time	t_{DH}	0		ns
	End Write to Output Low-Z	t_{OW}	5		ns
Page	Page Mode Cycle Time	t_{PC}	25		ns
	Page Mode Address Access Time	t_{PAA}		25	ns
	Maximum Cycle Time	t_{MRC}		20K	ns
	$\overline{PCS1}$ High Pulse Width	t_{CP}	10		ns

Power Up Sequence

1. Apply Power.
2. Maintain stable power for a minimum of 200 µs with $\overline{PCS1} = V_{IH}$

Standby Mode State Machines

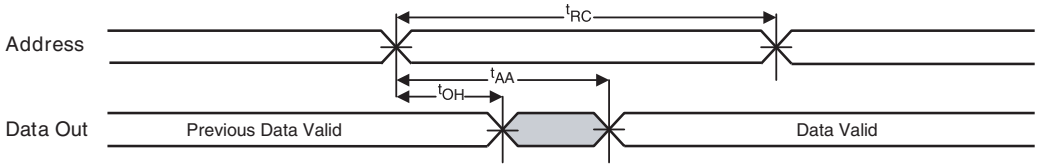


Standby Mode Characteristics

Mode	Memory Cell Data	Standby Current (µA)	Wait Time (µs)
Standby	Valid	70 (ISB1)	0
Low Power Modes	Invalid	10 (ISB0)	200

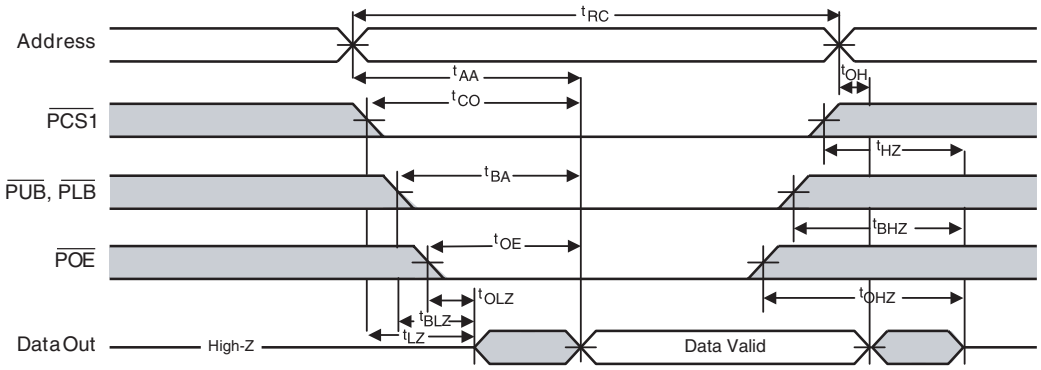
Read Cycle (1)

(Address Controlled, $\overline{PCS1}$ = $\overline{POE}$ = V_{IL}, $\overline{ZZ}$ = $\overline{PWE}$ = V_{IH}, $\overline{PUB}$ or/and $\overline{PLB}$ = V_{IL})



Read Cycle (2)

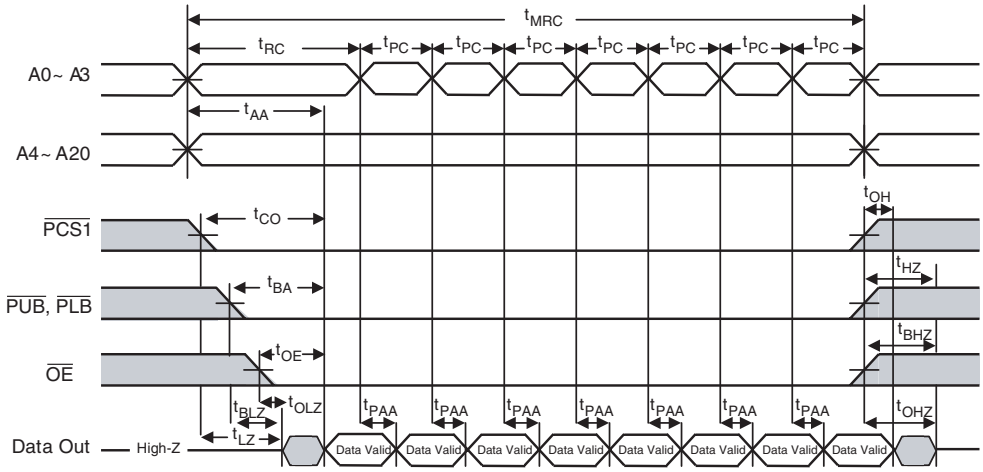
($\overline{ZZ}$ = $\overline{PWE}$ = V_{IH})



Notes:
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (max) is less than t_{LZ} (min) both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than t_{RC} (t_{WC}) for continuous periods > 40 µs.

Page Read Cycle

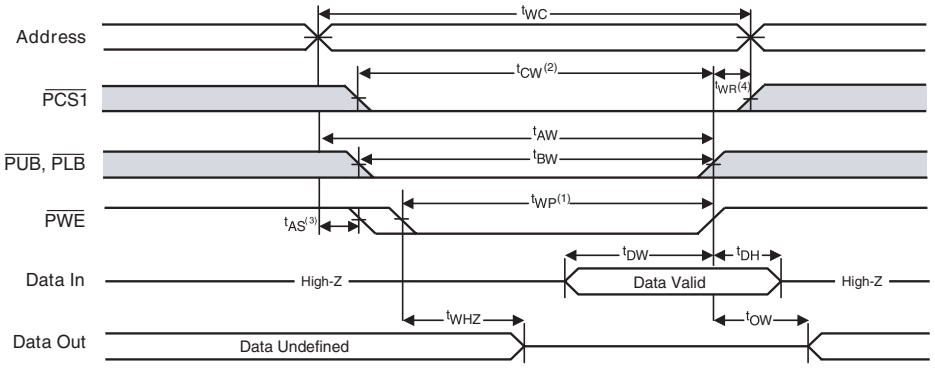
($\overline{ZZ}$ = $\overline{PWE}$ = V_{IH}, 16 Words Access)



Notes:
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (max) is less than t_{LZ} (min) both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than t_{RC} (t_{WC}) for continuous periods > 20 µs.

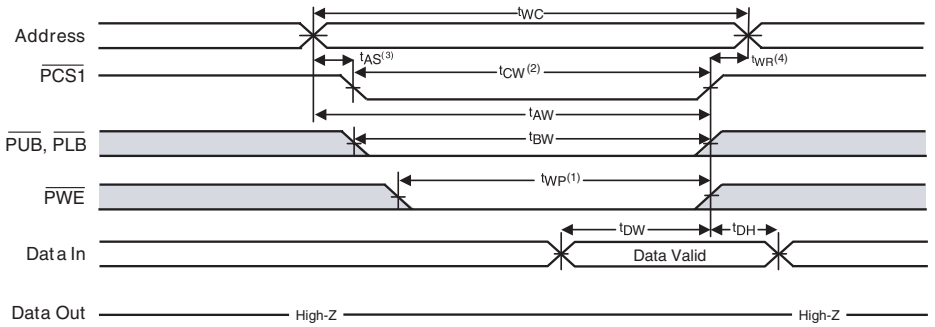
Write Cycle (1)

($\overline{PWE}$ Controlled, $\overline{ZZ}$ = V_{IH})



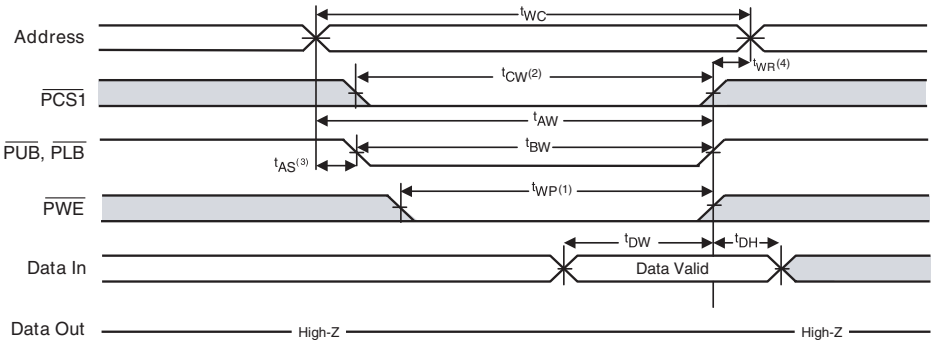
Write Cycle (2)

($\overline{PCS1}$ Controlled, $\overline{ZZ}$ = V_{IH})



Write Cycle (3)

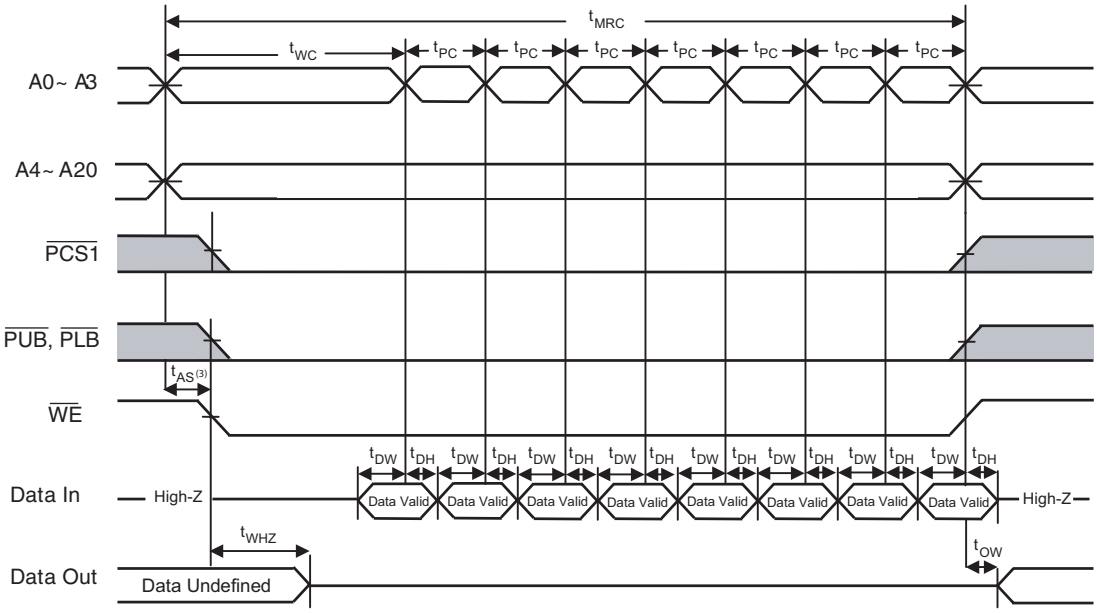
($\overline{PUB}$, $\overline{PLB}$ Controlled, $\overline{ZZ}$ = V_{IH})



Notes:
1. A write occurs during the overlap (t_{WP}) of low $\overline{PCS1}$ and $\overline{PWE}$. A write begins when $\overline{PCS1}$ goes low and $\overline{PWE}$ goes low with asserting $\overline{PUB}$ or $\overline{PLB}$ for single byte operation or simultaneously asserting $\overline{PUB}$ and $\overline{PLB}$ for double byte operation. A write ends at the earliest transition when $\overline{PCS1}$ goes high and $\overline{PWE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{PCS1}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{PCS1}$ or $\overline{PWE}$ going high.
5. Do not access device with cycle timing shorter than t_{RC} (t_{WC}) for continuous periods > 40 µs.

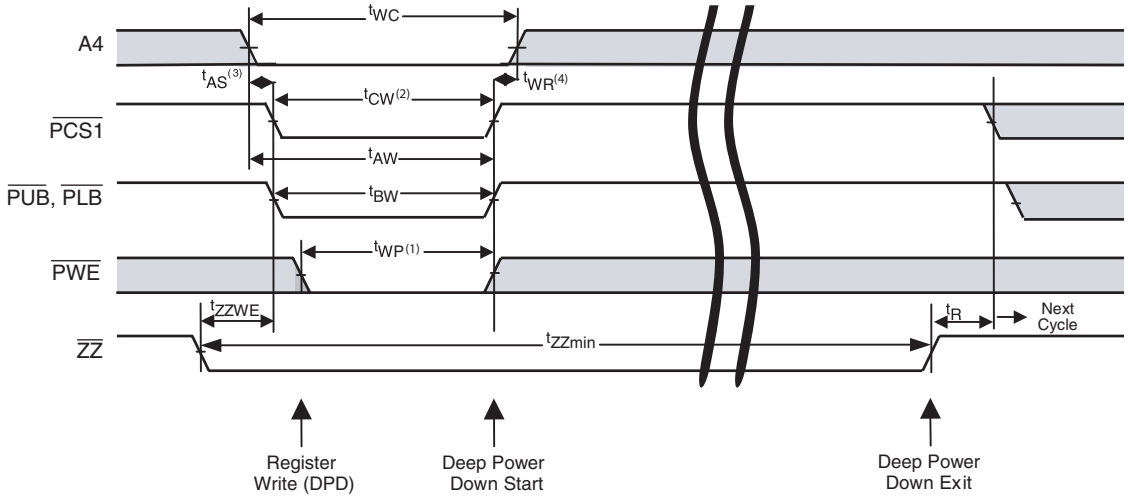
Page Write Cycle

(Address Controlled, $\overline{ZZ} = V_{IH}$)



Notes:
1. A write occurs during the overlap (t_{WP}) of low $\overline{PCS1}$ and $\overline{PWE}$. A write begins when $\overline{PCS1}$ goes low and $\overline{PWE}$ goes low with asserting $\overline{PUB}$ or $\overline{PLB}$ for single byte operation or simultaneously asserting $\overline{PUB}$ and $\overline{PLB}$ for double byte operation. A write ends at the earliest transition when $\overline{PCS1}$ goes high and $\overline{PWE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{PCS1}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{PCS1}$ or $\overline{PWE}$ going high.
5. Do not access device with cycle timing shorter than t_{RC} (t_{WC}) for continuous periods > 20 µs.

Deep Power-down Mode Entry/Exit



Parameter	Description	Min	Max	Units
t_{ZZWE}	$\overline{ZZ}$ low to Write Enable Low	0	1	µs
t_R (Deep Power-down Mode Only)	Operation Recovery Time		200	µs
t_{ZZmin}	Low Power Mode Time	10		µs

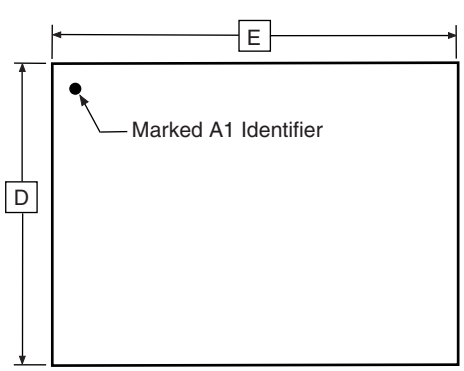
Ordering Information

t_{ACC} (ns)	Ordering Code	Flash Boot Block	Flash Plane Architecture	PSRAM	Package	Operation Range
70	AT52BC3221A-70CI	Bottom	32M – Single Bank	512K x 16	66C5	Extended (-25° to 85°C)
70	AT52BC3221AT-70CI	Top	32M – Single Bank	512K x 16	66C5	Extended (-25° to 85°C)

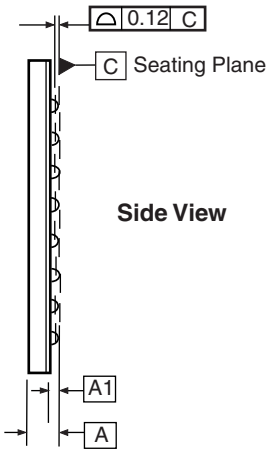
Package Type	
66C5	66-ball, Plastic Chip-size Ball Grid Array Package (CBGA)

Packaging Information

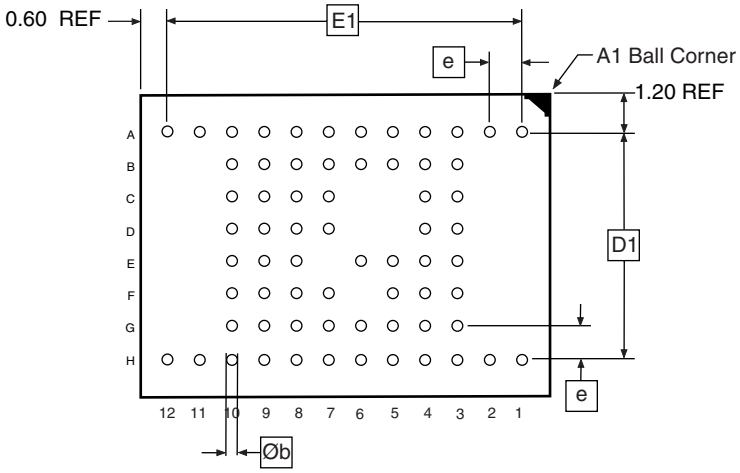
66C5 – CBGA



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
E	9.90	10.00	10.10	
E1	–	8.80	–	
D	7.90	8.00	8.10	
D1	–	5.60	–	
A	–	–	1.20	
A1	0.25	–	–	
e	0.80 BSC			
Øb	–	0.40	–	

09/19/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**66C5**, 66-ball (12 x 8 Array), 10 x 8 x 1.2 mm Body, 0.8 mm Ball Pitch Chip-scale Ball Grid Array Package (CBGA)	66C5	A

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