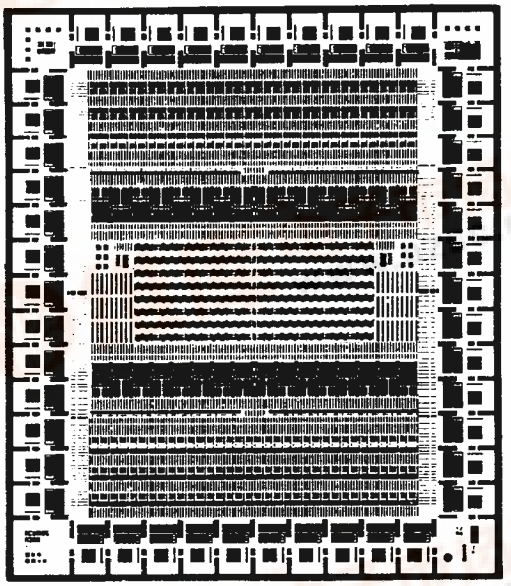
A300
Analog/Digital Gate Array

DESCRIPTION

The Acumos A300 is a high performance analog/digital gate array. The gate array can perform analog and/or digital functions. The gate array is silicon gate construction using a double-poly p-well process. The minimum gate channel length is 4 microns. Customization is done by single layer metal.

FEATURES

- √ Analog & Digital sections
- √ High breakdown voltage -- 12V
- √ Internal gate prop delay -- less than 5ns
- √ Output sink current per transistor 6 mA
- √ Op amps with gain over 70 dB
- √ Matched resistors and capacitors on chip
- √ 300 equivalent gates in digital section
- √ Single or dual supply operation



A300 Analog/Digital Gate Array Chip
Chip size: 138 mils X 167 mils

APPLICATIONS

The A300 can be configured to do many functions. Here's a list of some of them:

- A to D and D to A converter with up to 8 bits resolution
- A set of filters. For example the chip can contain two "MF10" type filters plus other functions.
- A set of comparators . . . as many as 20 comparators . . . Offset voltage (uncompensated) as low as 15mV . . . . offsets that are internally compensated (no external components)can be in the micro volt region.
- Voltage reference.
- Phase locked loops, including the loop filter.
- Peak detectors and sample and hold circuits.
- Analog multiplexer.

Besides performing a selection of any of these functions, one chip can contain the normal housekeeping jobs such as decoding, buffering, etc.

ORGANIZATION of the ARRAY

The array has 9 sections:

1. **Digital section.** This area contains 400 CMOS transistor pairs. A transistor pair consists of one p channel and one n channel device. Since it takes two pairs to make a two input NAND gate, this area has the potential of making 200 two input NAND gates. Due to interconnect congestion it is difficult to realize 200 gates -- a good estimate is 80 to 90% depending on the particular circuit.

2. **Analog/digital section.** This section contains 200 transistor pairs. The dimensions of the devices are the same as those in the digital section, however they are laid out such that p and n channel devices can be used separately. This allows the designer to use them either as individual transistors for analog applications or as pairs for additional digital functions. Used as pairs this gives the chip an additional 100 two input NAND gates.

3. **Analog switch section.** This section contains 192 minimum geometry MOS switches. These devices are particularly suited for building switched capacitor filters.

4. **Analog section.** This section contains 256 large transistors. This is the section that is used to make op amps, comparators, etc.

5. **Capacitor section.** This section contains 250 capacitor units of 0.4 pF each. Units can be paralleled to make larger values. Capacitors are constructed of poly-silicon, silicon-dioxide-poly silicon. They have a tolerance of approximately plus or minus 15%.

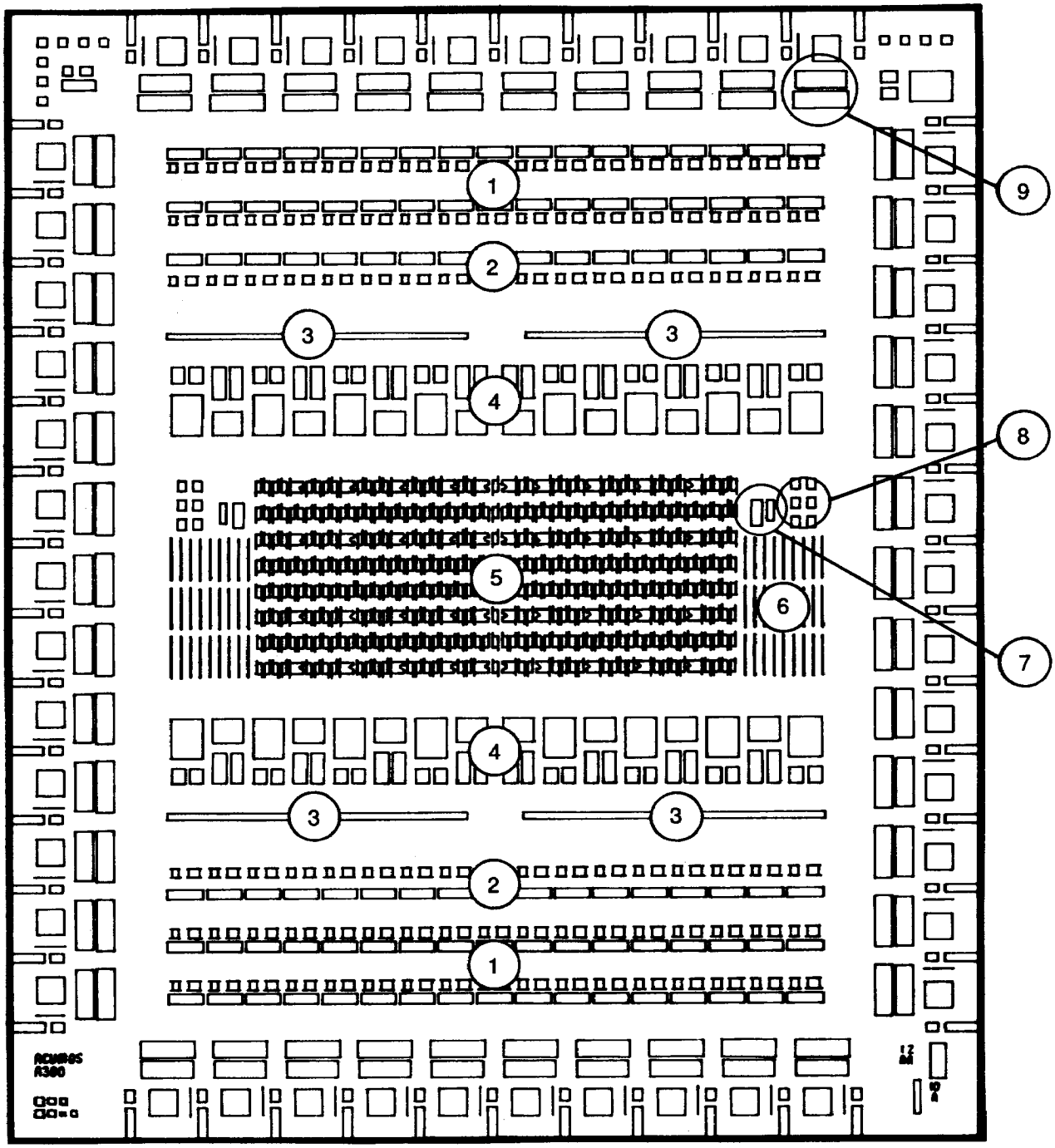
6. **Resistor section:** This contains 54 20k ohm P well resistors and have a tolerance of about 30%.

7. **High resistance FET section.** These devices are used to make high resistance values. Values on these devices can become very high but due to their nature the tolerances are more than 2 to 300%.

8. **Bipolar transistor section.** This contains 12 lateral NPN transistors which can be used as low noise input devices or in a voltage reference circuit.

9. **Output driver section.** There are 46 driver pairs arranged around the periphery of the device. These devices can sink 6 mA at a VOL of 0.4V maximum.

SECTION	DEVICE	QUANTITY	SIZE
Digital	nMOS	400	31/4
	pMOS	400	39/4
Digital-Analog	nMOS	100	31/4
	pMOS	100	39/4
Analog	nMOS	64	59/9
	pMOS	64	59/9
	nMOS	64	118/9
	pMOS	64	118/9
Analog Switch	nMOS	96	4/4
	pMOS	96	4/4
Bipolar	NPN	12	
Output Transistor	pMOS	176	80/4
	nMOS	176	80/4
Output Pads		46	
Capacitor	Poly-Poly	250	0.4 pf
Resistor	P - Well	54	20 k
Hi R. FET	Pinch FET	4	>15 meg



A300 ORGANIZATION

1. Digital section
2. Digital/analog section
3. Analog/switch section
4. Analog section
5. Capacitor section
6. Resistor section
7. High resistance FET section
8. Bipolar transistor section
9. Output driver section (entire periphery)

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MAXIMUM OPERATING CONDITIONS:

SYMBOL	ITEM	RATING	UNITS
V_{CC}	D.C. Supply voltage	12 volts	V
	Voltage on any pin	VSS − 0.3 V to VDD+ 0.3 V	V
I_I	Input current	± 20 mA	mA
T_{opr}	Operating temp	−10 to + 85° C	C

DIGITAL CIRCUIT SECTION SPECIFICATIONS:

D.C. CHARACTERISTICS : V_{CC} = 5 V; T_A = 25° C

SYMBOL	ITEM	TEST CONDITIONS	RATING			UNITS
			MIN	TYP	MAX	
V_{IL}	Low level input voltage (TTL Input)	V_{CC} = 5 V			0.8	V
V_{IH}	High level input voltage (TTL Input)		2.0			V
V_{OL}	Low level outout voltage:					
		@ I_{OL} = −1μA			0.05	V
		@ I_{OL} = − 6 mA			0.4	V
V_{OH}	High level outout votage					
		@ I_{OH} = 1μA	4.95			V
		@ I_{OH} = 2 mA	4.0			V

A.C. CHARACTERISTICS : V_{CC} = 5 V; T_A = 25° C

SYMBOL	ITEM	TEST CONDITIONS	RATING			UNITS
			MIN	TYP	MAX	
fmax	Maximum Clock Frequency	50% duty cycle			20	MHz
t_d	Gate Delay for 2-input gate			5		ns
t_{dz}	Gate Delay for input buffer			10		ns
t_{do}	Gate Delay for output buffer			10		ns

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AVAILABLE PACKAGES

TYPES	NO. OF PINS
DIP	14, 16, 18, 20, 22,24,28, and 40
PLCC	28 and 44

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