VERSATILE SEMICONDUCTOR PRODUCTS

PHASE ENCODED TRANSPONDER VSP1000

The VSP1000 is a high performance, low power identification system building block which supports several modes of operation. The device has an internal programmable memory array which can allow for up to 39 bits of internal identification data or about 549,755,813,000 discrete codes. The device is capable of sending internal data in 21, 27, 33, and 39 bit formats. The device can also be programmed to send up to 18 bits of data from external data registers, and it can also be placed in a mode which allows an external intelligent device to take over control of the chip and send an unlimited amount of 7 bit data with automatic parity generation.

The device has a wide voltage operating range and consumes little operating power, due to its pseudo-static architecture. The clock rate can be as low as DC and as high as 3.0 MHz.

The data format includes word parity and frame checksum for high data integrity.

FEATURES

Three major operating modes

1. **Internal data - 21, 27, 33, or 39 bits of data**
2. **Internal/external data**
   - **21 bits internal and 6, 12, or 18 bits of external data**
   - **26 bits internal and 6 or 12 bits of external data**
   - **33 bits internal and 6 bits of external data**
3. **External streaming data - unlimited data of 7 bit words with automatic parity generation**

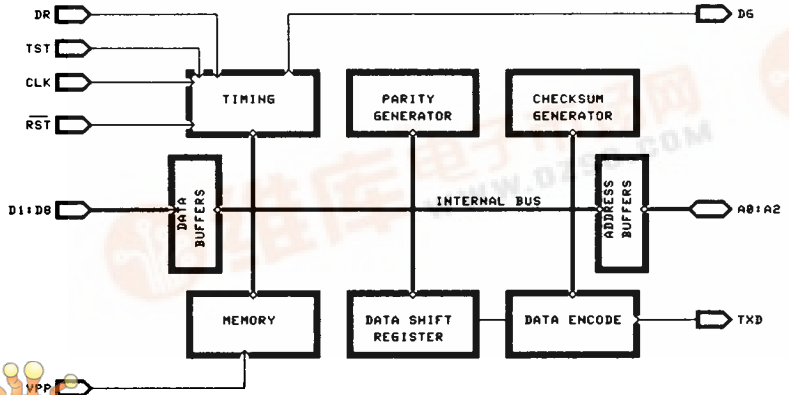
Wide operating range

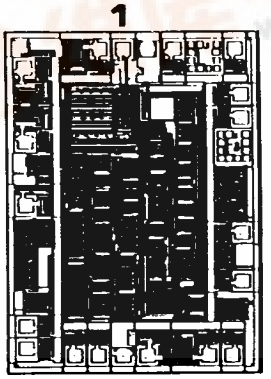
1.25 TO 7 VOLTS (VCC)
DC TO 3.0 MHz CLOCK
DATA RATE OF F(clk)/16

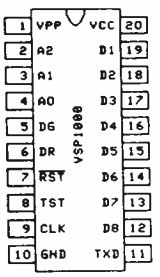
Low power consumption of 0.5 uA/KHz (typ)

PC (or clone) programming card and software available

BLOCK DIAGRAM AND PINOUT







RECOMMENDED OPERATING CONDITIONS				
ITEM	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE - VCC GND	1.25 [1] 0	5.00 0	7.00 0	VOLTS VOLTS
INPUT VOLTAGE - HIGH LOW	VCC/2 -0.3	— —	VCC+.5 VCC/6	VOLTS VOLTS
TEMPERATURE - PLASTIC CERAMIC	-40 -55	— —	70 85	DEG. C DEG. C
STORAGE CONDITIONS				
TEMPERATURE	-65	—	90	DEG. C
DC OPERATING CHARACTERISTICS (VCC = 5V, Ta=20 C)				
INPUT LEAKAGE CURRENT (Vin=GND)	—	—	2	uA
POWER SUPPLY CURRENT	—	—	10	uA
OUTPUT VOLTAGE HIGH NO LOAD	4.0	4.5	5.0	VOLTS
LOW NO LOAD	0	0.2	0.4	VOLTS
OUTPUT CURRENT [Rl=300 ohms] Voh Vol	— —	13.0 2.0	16.6 7.7	mA mA
RESET CURRENT (Vreset=GND)	—	15	50	uA
AC CHARACTERISTICS (VCC=5V, Ta=20 C, Fclk=15 KHz)				
CLOCK EDGE SLEW RATE	.15	—	100	V/uS
CLOCK PULSE WIDTH HIGH	.3	—	33	uS
Dgrant TO Drequest ACCEPT TIME	—	—	38,400	CLK [2]
Drequest TO DATA STABLE TIME	—	—	16	CLK [2]
TXD STATE SWITCHING TIME	—	20	—	nS
POWER SUPPLY CURRENT	—	0.5	2.0	uA/KHz

NOTES:

[1] OPERATION BELOW 3 VOLTS (VCC) IS LIMITED TO F(clk) < 1.0 MHz.

[2] SPECIFIED TIME IS A NUMBER OF CLOCK CYCLES.

PHASE ENCODED TRANSPONDER "PET" DATA TRANSMISSION

Each data word consists of a unique start bit, a sync bit, 6 data bits, odd parity, and one stop bit. Word 1 contains three ID bits. In addition, three bits W5EN, W6EN, and W7EN indicate if any additional data words are to follow the fourth word. Each data word contains 6 data bits. After the data (words 1 to 4 and, if enabled, words 5, 6, or 7) has been transmitted, the checksum word (XOR) is sent and the data frame is repeated. A data frame can consist of 5, 6, 7, or 8 words depending on the operating mode selected. The XOR is only computed on the 6 data bits of each frame. Words 5, 6, and 7 may be internal ROM or external bus data depending on the state of D8 during programming. Optional ROM data words should be enabled in order.

DATA FORMAT: TIME ⟶

	WORD1	WORD2	WORD3	WORD4	WORD5	WORD6	WORD7	WORD8
B9	STOP	STOP	STOP	STOP	STOP	STOP	STOP	STOP
B8	PAR 1	PAR 2	PAR 3	PAR 4	PAR 5	PAR 6	PAR 7	PAR 8
B7	W7EN	W2D7	W3D7	W4D7	W5D7	W6D7	W7D7	XOR 7
B6	W6EN	W2D6	W3D6	W4D6	W5D6	W6D6	W7D6	XOR 6
B5	W5EN	W2D5	W3D5	W4D5	W5D5	W6D5	W7D5	XOR 5
B4	W1D4	W2D4	W3D4	W4D4	W5D4	W6D4	W7D4	XOR 4
B3	W1D3	W2D3	W3D3	W4D3	W5D3	W6D3	W7D3	XOR 3
B2	W1D2	W2D2	W3D2	W4D2	W5D2	W6D2	W7D2	XOR 2
B1	SYNC	0	0	0	0	0	0	0
B0	START	START	START	START	START	START	START	START

TIME ⟶

--- N O T E S ---

[1] The start bit consists of two 50% duty cycle square waves which are 8 clock cycles wide (4 clock cycles on and 4 clock cycles off).

[2] The stop bit consists of a 16 clock cycle quiet period (TXD=0).

[3] A one bit is 75% on followed by 25% off.

[4] The zero bit is 25% on and 75% off.

EXTERNAL DATA TRANSMISSION

If any of W5EN, W6EN, or W7EN are ones during the priority decoder load, A2 will be pulsed high during word 1 to indicate a possible external data read cycle. If word 5, 6, or 7 has been enabled and if the ROM has been programmed with D8 at a logical one at word 5, 6, or 7, the ROM data is disabled to the end of the data frame. The external data bus is enabled allowing 6 bits of data to be placed on the internal data bus.

STREAMING DATA TRANSMISSION

After 655,360 clock cycles, the streaming data mode is entered, the DG signal enables the external data port, D1-D7, D1 takes the place of the sync bit in the word. Entry into the mode is indicated by DG going to a high. If DR goes to a high level within 40,960 clock cycles, the first word in the data steaming mode can be transmitted (DR must be pulled low before the end of the transmitted word). At the end of the transmission, another DG will be issued. After all data streaming words are sent, DR should remain at a logical low level. This is sensed and resets the system just as in power up initialization, and the chip reverts to normal transmission. It is recommended that a streaming data preamble of three words of all bits (D1-D7) at ones be sent in this mode. No XOR checksums are sent upon exit of the streaming data mode; however, parity generation (odd) is automatic. If data integrity is required, the micro controller should block and checksum the data.

The streaming data mode may be quickly bypassed by connecting DG to TST. The chip may be accelerated to streaming data mode by inverting DG and connecting the inverted DG signal to TST.

SERIAL DATA OUT

The start and stop bits are unique to the remaining data bits. The start bit is a double transition bit cell whereas the data bits are single transition cells. The stop bit has no transitions within its time window. This allows for a quiet period for microprocessor decoding of the data word, parity, and checksum verification.

PROGRAMMING

The internal PMOS PROM can be programmed by setting Vpp to a zero level. This disables the ROM's output circuitry and enables the address mux to allow the external address bits A0-A2 to drive the ROM. By setting clock to a one (+5V), the data port is also enabled to drive the ROM data port. The ROM is programmed as follows:

[1] Insert the chip to be programmed. VCC to +5 volts. Present the address of the word to be programmed to A0-A2 and the data to D2 thru D8. Keep D1, TST, VPP , and DR at ground. Keep RST to VCC.

[2] Lower VPP to programming voltage level (-14V) no faster than 500 micro-seconds/volt.

[3] Hold VPP at -14 volts for 10 milliseconds.

[4] Allow VPP to return to 0 volts no faster than 500 micro-sec/volt.

[5] Repeat the procedure for each word to be programmed (Go to 2).

<table>
<tr><th>PIN</th><th>NAME</th><th>SYMB</th><th>FUNCTION</th></tr>
<tr><td>19</td><td>DATA(1)</td><td>D1</td><td>When in streaming external data mode, this extra data bit replaces the sync bit.</td></tr>
<tr><td>12-18</td><td>DATA(2:8)</td><td>D2-D8</td><td>In program mode (VPP=0 or -14 Volts), D2-D8 are data inputs. When D8=1 in word 5,6, or 7, external data is selected. When D8=0, internal data is selected. D8 has an internal pullup. In operation, the external data bus D2 to D7 can be read into the internal bus if D8 has been programmed to a "1" at that specific word and the proper enable bits have been programmed to a "1" in word 1. A2 is a wake up flag in this mode of operation (pulses high at word 1). If no external data access is enabled, the data lines (except D8) should be connected to the GND pin. D8 should be left unconnected.</td></tr>
<tr><td>7</td><td>RESET</td><td>$\overline{\text{RST}}$</td><td>A low level applied to this line resets the internal logic. A capacitor should be connected between it and ground (GND). Connecting the test pin to Data Grant (DG) and the reset pin to VCC will act to speed the chip past streaming data mode (if this mode is unused) and reduce component count.</td></tr>
<tr><td>10</td><td>GROUND</td><td>GND</td><td>The VCC reference point.</td></tr>
<tr><td>2-4</td><td>ADD(0:2)</td><td>A0-A2</td><td>Address outputs if VPP is high. In this mode, A2 indicates the added external data read cycle by going high (1) during word 1. A0 and A1 indicate the external data word to be read during word 5, word 6 or word 7:
<table>
<tr><th>A0</th><th>A1</th><th>Read Word</th></tr>
<tr><td>1</td><td>1</td><td>external word 5</td></tr>
<tr><td>0</td><td>1</td><td>external word 6</td></tr>
<tr><td>1</td><td>0</td><td>external word 7</td></tr>
<tr><td>0</td><td>0</td><td>none selected</td></tr>
</table>
During program mode (VPP=low), A0-A2 are active ROM address inputs:
<table>
<tr><th>A0</th><th>A1</th><th>A2</th><th>Program Word</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>word 1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>word 2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>word 3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>word 4</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>word 5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>word 6</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>word 7</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>invalid (do not use)</td></tr>
</table>
The address lines have internal pull downs and should not be connected to GND or VCC.</td></tr>
<tr><td>5</td><td>DATA GRANT</td><td>DG</td><td>This output goes to a high level when it is permitted to enter streaming data mode and then on each new data word load.</td></tr>
</table>

PIN	NAME	SYM	FUNCTION
6	DATA REQ	DR	This input should go high (logic 1) in response to DG if streaming data is is to be transmitted. It should be returned to low when DG goes low or is connected to GND if no streaming data is to be sent.
1	PROGRAM	VPP	This input should go from 0 to -14 volts when programming the ROM. It should be tied to VCC when not programming.
8	TEST	TST	This pin should be tied to GND unless it is tied to DG to accelerate through streaming data mode. If DG is inverted and tied to TST, then the system will accelerate to streaming mode.
11	DATA OUT	TXD	This output is the phase encoded serial data to drive a transmitter.
9	CLOCK	CLK	This input is the basic clock used by the circuit. In program mode, this input should be connected to VCC.
20	POWER	VCC	This is the power input.

ORDERING INFORMATION

20 pin plastic DIP is part number VSP1000N
20 pin plastic SOIC (wide body) is part number VSP1000F
20 pin ceramic DIP is part number VSP1000C
Tested die (88 X 123 mils) is part number VSP1000D
Manual programmer is MPGX1000
PC based programmer is APGX1000

MARKETED BY

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General Notices

These specifications are subject to change without notice.

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