GEC PLESSEY
SEMICONDUCTORS

ADVANCE INFORMATION

D.S.3182 2.2

VP8708

30MHz 8–BIT ANALOG VIDEO INPUT INTERFACE

(Supersedes edition in December 1993 Digital Video & Digital Signal Processing Handbook)

The VP8708 is an analog input interface designed for video signal conditioning and digitisation.

Operating from a single +5V supply, the VP8708 includes an input multiplexer, video amplifier with clamp and gain control, an onboard reference and a buffered 8–bit ADC capable of digitising signals upto the Nyquist limit.

Video signals may be supplied to the VP8708 either directly to the ADC, or via one of three multiplexed inputs for signal conditioning. The analog signal (with appropriate gain and clamping) is available as output prior to digitisation. The coded data, updated at the sample rate, is available in either binary or two's complement format via the 3–state TTL output buffers.

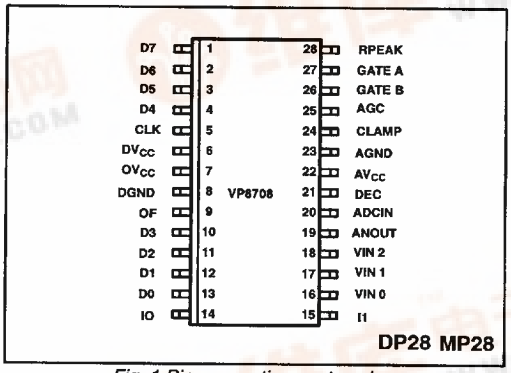

Fig. 1 Pin connections – top view

FEATURES

- Direct replacement for the PhilipsTDA8708†
- 30MHz Sampling rate
- Selectable data format:
- Internal ADC reference
- Clamp and AGC functions
- 3–state TTL outputs

†GEC Plessey also offer direct replacements for Philips TDA8708A (GPS part no VP87A8) TDA8709A (GPS part no VP87A9)

ORDERING INFORMATION

VP8708G CG DPAS (Commercial – Plastic DIL)
VP8708G CG MPES (Commercial – Miniature Plastic DIL)

ABSOLUTE MAXIMUM RATINGS

Supply voltages, AV_{CC}, DV_{CC}, OV_{CC}	+7V
Supply differential	±1V
Ground differential	±1V
Video input voltage	AV_{CC}
Output current	10mA

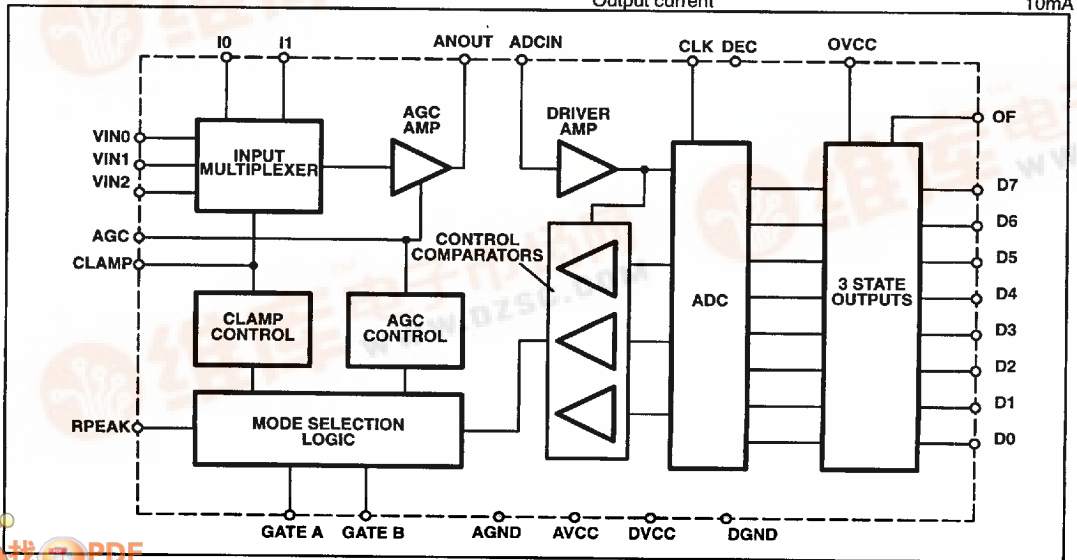

Fig. 2 System block diagram

RECOMMENDED OPERATING CONDITIONS

Supply voltage AV_{CC}, DV_{CC}, OV_{CC}	+5V
Supply differential	0V
Ground differential	0V
Video input voltage	1Vp–p

OPERATING TEMPERATURE RANGE

Commercial	0°C to +70°C (still air ambient)

THERMAL CHARACTERISTICS

Storage temperature range	–65°C to 150°C
Lead temperature (soldering 11 seconds)	+265°C
THERMAL RESISTANCES, DP PACKAGE	
Junction to ambient (θ_{ja})	55°C/W
Junction to case (θ_{jc})	14°C/W
THERMAL RESISTANCES, MP PACKAGE	
Junction to ambient (θ_{ja})	84°C/W
Junction to case (θ_{jc})	32°C/W

ELECTRICAL CHARACTERISTICS:

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value Min	Value Typ	Value Max	Units	Conditions
POWER SUPPLY								
Analog supply voltage	AV_{CC}	25 FULL	1 4	4.5 4.5	5.0 5.0	5.5 5.5	V V	
Digital supply voltage	DV_{CC}	25 FULL	1 4	4.5 4.5	5.0 5.0	5.5 5.5	V V	
Output supply voltage	OV_{CC}	25 FULL	1 4	4.5 4.5	5.0 5.0	5.5 5.5	V V	
Analog supply current	AI_{CC}	25 FULL	1 4		60	 72	mA mA	
Digital supply current	DI_{CC}	25 FULL	1 4		13	 19	mA mA	
Output supply current	OI_{CC}	25 FULL	1 4		12	 18	mA mA	
Power dissipation	P	25 FULL	1 4		425	 600	mW mW	
VIDEO INPUTS								
Input range	V_{IN} (p–p)	FULL	4	0.5	1.0	1.6	V	
Input impedance	$\|Z_{IN}\|$	FULL	4	18	20	22	kΩ	f_{in}=6MHZ
Input capacitance	C_{in}	25	5		2		pF	f_{in}=6MHZ
I1, IO GATE B,TTL INPUTS + GATE A								
Input voltage LOW	V_{il}	25 FULL	1 4			0.8 0.8	V V	
Input current HIGH	V_{ih}	25 FULL	1 4	2.0 2.0			V V	
Input current LOW	I_{il}	25 FULL	1 4	–150 –200			µA µA	V_i=0.4V V_i=0.4V
Input current HIGH	I_{ih}	25 FULL	1 4			10 20	µA µA	V_i=3.6V V_i=3.6V
RPEAK Input								
Peak capacitor charge/discharge current	I_{PEAK}	FULL	4		80		µA	R_{peak} = 0Ω

ELECTRICAL CHARACTERISTICS:

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
AGC Control Input								
AGC voltage for minimum gain	V_{agc}	25	4		2.7		V	
AGC voltage for maximum gain	V_{agc}	25	4		3.9		V	
AGC output current	I_{agc}	25	1		*			* See table 4
CLAMP Control Input								
Clamp voltage	V_{clp}	25	4		3.5		V	ADC output = 128
Clamp output current	I_{clp}	25	1		*			* See table 4
VIDEO Amplifier Outputs								
Internal current source	I_{19}	25	4			2	mA	
DC Output voltage for black level	V_{blk}	FULL	4		AV_{CC}– 3.25		V	
AC Output voltage (peak–peak)	V_{19}	FULL	4		1		V	
Output impedance	Z_{19}	25	4		45		Ω	
CLK INPUT								
Input voltage LOW	V_{il}	25 FULL	1 4			0.8 0.8	V V	
Input voltage HIGH	V_{ih}	25 FULL	1 4	2.0 2.0			V V	
Input current LOW	I_{il}	25 FULL	1 4	–150 –200			µA µA	V_i = 0.4V V_i = 0.4V
Input current HIGH	I_{ih}	25 FULL	1 4			10 20	µA µA	V_i= 3.6V V_i= 3.6V
Input impedance	$\|Z_{IN}\|$	25	4		3.5		kΩ	
Input capacitance	C_{clk}	25	4		5		pF	
Maximum frequency	f_{max}	FULL	4	30			MHz	
OF INPUT (3–state control)								
Input voltage LOW	V_{il}	25 FULL	1 4			0.8 0.8	V V	
Input voltage HIGH	V_{ih}	25 FULL	1 4	2.0 2.0			V V	
Input voltage 3–STATE	V_z	25	1		1.4		V	
Input current LOW	I_{il}	25 FULL	1 4	–175 –200			µA µA	V_i=0.4V V_i=0.4V
Input current HIGH	I_{ih}	25 FULL	1 4			500 700	µA µA	V_i=3.6V V_i=3.6V

ELECTRICAL CHARACTERISTICS:

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
ADCIN INPUT								
Input voltage	V_{adc}	FULL	4		AV_{CC}– 1.75		V	For Code 0
Input voltage	V_{adc}	FULL	4		AV_{CC}– 1.25		V	For Code 255
Input voltage amplitude (p–p)	V_{20}	FULL	4		0.5		V	
Input current	I_{adc}	25	1		1		µA	
Input impedance	Z_{adc}	25	1		14		MΩ	
Input capacitance	C_{adc}	25	4		5		pF	
DIGITAL OUTPUTS								
Output voltage LOW	V_{ol}	25 FULL	4 4			0.4 0.4	V V	I_{ol}= 2mA I_{ol}= 2mA
Output voltage HIGH	V_{oh}	25 FULL	1 4	2.4 2.4			V V	I_{oh}=–0.4mA I_{oh}=–0.4mA
3–STATE Output current	I_{OZ}	25	4		2		µA	
ADC PERFORMANCE								
Static differential non – linearity	DNL	25 FULL	1 4		±0.5 ±0.5		lsb lsb	
Static integral non – linearity	INL	25 FULL	1 4		±1 ±1		lsb lsb	
Dynamic integral non – linearity	INL	25 FULL	1 4		±2 ±2		lsb lsb	
VIDEO AMPLIFIER DYNAMIC PERFORMANCE								
–3dB Bandwidth	f3dB	25	4		20		MHz	
Differential gain	G_d	25	4		2		%	
Differential phase	$\varnothing_d$	25	4		2		degrees	
Gain range	ΔG	25	4	–3		7	dB	
Crosstalk between VIN inputs		25	4		–60		dB	
Signal–to–noise ratio	SNR	25	4		55		dB	
ANALOG SIGNAL* PROCESSING								*f_{clk} = 30MHz
–3dB Bandwidth	f3dB	25	1		15		MHz	
Differential gain	G_d	25	4		2		%	
Differential phase	$\varnothing_d$	25	4		2		degrees	
Total harmonic distortion	THD	25	4		–55		dB	
Supply voltage ripple rejection	SVRR	25	4		5		%/V	

ELECTRICAL CHARACTERISTICS:

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
TIMING*								* f_{clk}=30MHz C_1=15pF I_{OI}=2mA
Sampling delay	t_{ds}	FULL	4		3		ns	
Output hold time	t_{ho}	FULL	4	5			ns	
Output delay time	t_d	FULL	4			20	ns	
3 State delay time for enble	t_{ez}	FULL	4			25	ns	
3 State delay time for disable	t_{dz}	FULL	4			25	ns	

ELECTRICAL CHARACTERISTIC DEFINITIONS

Analog –3dB Bandwidth ADC

The analog input frequency at which the spectral power of the fundamental frequency, as determined by Fast Fourier Transform analysis, is 3dB down on the DC level.

Differential Non–Linearity (DNL)

The deviation of any code width from an ideal 1LSB step size.

Integral Non–Linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least–square curve–fit.

Differential Gain (G_d) and Phase ($\varnothing_d$)

The difference in gain/phase at the ADC output when a 17.5 IRE units peak to peak, 3.58MHz input signal is superimposed on a dc level at 1/16 and 15/16 full scale input.

Supply Voltage Rejection Ratio (SVRR)

The variation in the amplitude of the given signal when the supply voltage is changed by 1V.

Signal–to–Noise Ratio

The ratio of the RMS signal amplitude to the RMS value of "noise" which is defined as the sum of all other spectral components including harmonics, but excluding DC with a full–scale analog input signal.

Total Harmonic Distortion (THD)

The RMS addition of all peaks in a Fast Fourier Transform measurement, which occur at integer multiples of the fundamental frequency of the input signal.

Test Levels

Level 1	100% production tested
Level 2	100% production tested at 25°C and sample tested at specified temperatures
Level 3	Sample tested only
Level 4	Parameter is guaranteed by design and characteristics testing
Level 5	Parameter is a typical value only

GENERAL CIRCUIT DESCRIPTION

The VP8708 is an analog video input interface capable of digitising signals at sample rates upto 30MHz.

The multiplexer uses the logic conditions on the selection pins (IO, I1) to select one of upto three signals applied to the video inputs (VIN0, VIN1, VIN2). This signal is then clamped to the required dc level by the action of the clamp control logic. The output of the multiplexer passes through the AGC amplifier, where the gain of the signal is adjusted such that after going through the driver amplifier, the signal fills the desired portion of the ADC range. This input to the ADC also drives three reference comparators which supply the signals necessary to control the clamp and AGC circuitry.

Two modes of operation are available; these being determined by the relative occurrences, during the sync and rear porch periods, of logic pulses at the GATE A and GATE B inputs.

Mode 1 (see Fig. 3) is employed initially to allow the device to reach its optimum operation point. The gain and dc level of the signal are roughly adjusted to set the sync level to ADC code 0 and the peak level to ADC code 255. This allows rapid recovery of the video synchronisation pulses.

If the GATE A and GATE B pulses become distinct (see Fig. 4) then the VP8708 will switch into mode 2. In this configuration a more sophisticated control scheme is used in order to produce a 'fixed'digitised output from the device: Whilst the GATE A pulse (which must be within the sync period) is high, the sync level is adjusted to code 0,.Similarly, the black level is adjusted to code 64 if the GATE B pulse occurs during the rear porch periods. Peak level control is always active such that maximum digital output will tend to lie below code 240. Nominal input signals, 1Vp–p, should have a peak output level equal to code 213.

For the device to operate, two external capacitors must be connected to the AGC and CLAMP pins. An optional external resistor may be attached to the RPEAK input to alter the maximum charge/discharge current into these capacitors. This varies the loop response time.

The format of the output data, updated at the sample rate, is determined by the logic level on the OF pin. The OF pin may also be used to force the outputs to a high impedance state.

The DEC ('decouple') pin is not connected on the VP8708. On similar devices (e.g. TDA8708) an external capacitor may be attached to this pin to stabilise the ADC reference voltage. The VP8708 has an internally stable reference and thus requires one less external component.

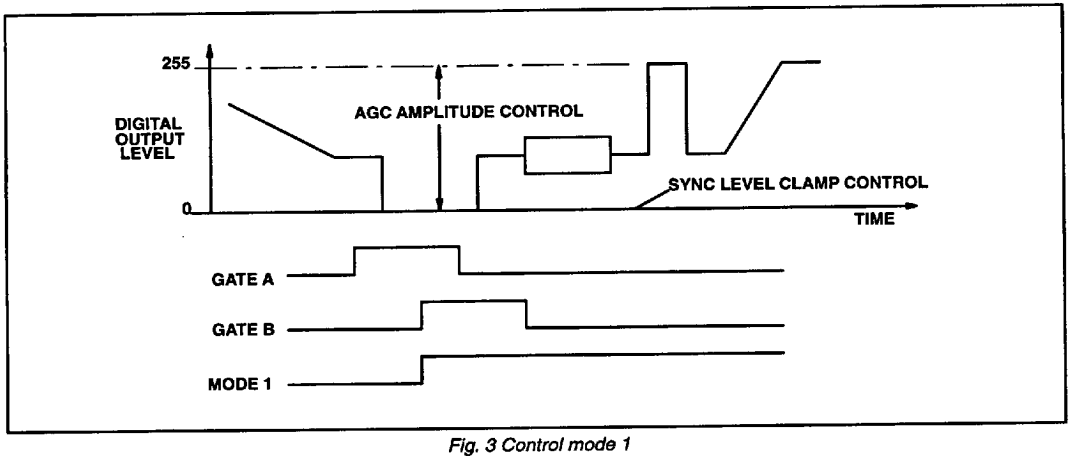

Fig. 3 Control mode 1

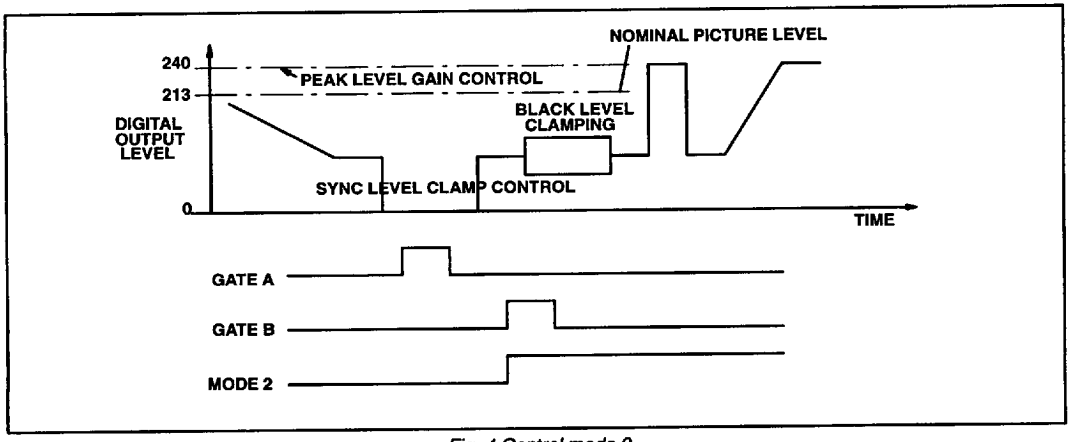

Fig. 4 Control mode 2

VIDEO INPUTS

Each of the three video inputs may be selected with the selection pins I0 and I1. Table 2 shows the action of these pins.

I1	I0	SELECTED INPUTS
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 Video input selection

OUTPUT FORMAT (OF PIN)

The format of the output data is selectable via the OF pin as shown in Table 3. To improve noise immunity, a small (10nF) capacitor may be connected between this pin and ground if binary operation is required.

OF	D0 TO D7
0	Active, two's complement
Open	Active, binary
1	High impedance

Table 3 Output format control

ANOUT AND ADCIN

The analog output (ANOUT) and ADC input (ADCIN) pins should have an external anti-aliasing filter connected betwen them. Care must be taken to ensure that the filter input impedance and filter output levels are in accordance with the specifications.

As an evaluatuion tool, two 1.5kΩ resistors may be used to form a potential divider between ANOUT and AV_{CC}. The centre tap of this divider can then be used to connect the signal to ADCIN. It should be noted however, that dynamic device performance will not be maximum.

TIMING INFORMATION

Fig. 5 depicts the system relationship between sampling edge offset and output data.

The analog input signal is sampled t_{ds} seconds after the rising edge of the clock signal. Old data will remain valid for at least t_{ho} and new data will become valid after at most t_d. Data may be latched on either the falling or rising edges of the clock signal.

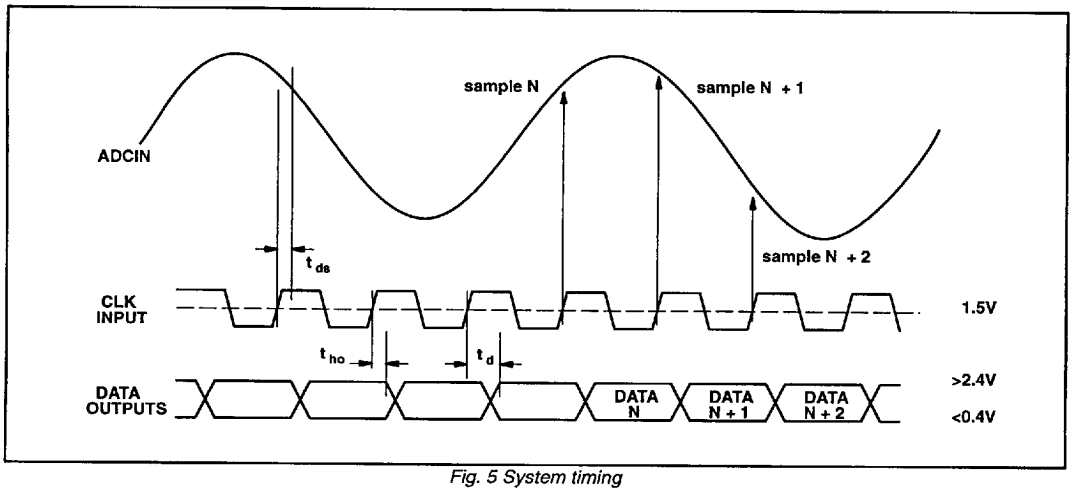

Fig. 5 System timing

AGC AND CLAMP CONTOL

In both mode 1 and 2, AGC and clamp control is achieved by the charging and discharging of two external capacitors attached to the AGC and CLAMP pins. Suggested values for these capacitors are C_{agc}=220nF and C_{clp}=18nF.

For correct device operation, the relative occurrences of the control pulses at the GATE A and GATE B pins must be as given below:

MODE 1 – GATE A and GATE B must overlap, GATE B being delayed with respect to GATE A. This will ensure that the signal fills the complete ADC range and thus allows quick recovery of the video sync pulses.

MODE 2 – GATE A must occur wholly within the sync period GATE B must occur wholly within the rear porch. This will tend to hold the output signal amplitude below code 240, the black level at code 64, and the sync tip at code 0.

Table 4 shows the control action of the device with reference to the logic states of the GATE A and GATE B inputs.

GATE A	GATE B	MODE	DIGITAL OUTPUT CODE	I_{AGC}	I_{CLP}
1	↑	Device will enter mode 1			
		1	Output >255	$-I_{peak}$	+5µA
		1	Output <255	+5µA	–
		1	Output >0	–	+5µA
		1	Output <0	+5µA	$-I_{peak}$
↑ ↓ 0	0 0 ↑	This control sequence will switch the device into mode 2.			
0	1	2	Output >240	$-I_{peak}$	+50µA
0	1	2	Output >64	–	+50µA
0	1	2	Output <64	–	–50µA
0	0	2	Output >240	$-I_{peak}$	–
1	0	2	Output >240	$-I_{peak}$	–
1	0	2	Output >0	–5µA	–
1	0	2	Output <0	+5µA	–

Table 4: Mode 1/Mode 2 control

PIN	NAME	DESCRIPTION
1	D7	Data Output Bit 7 (MSB)
2	D6	Data Output Bit 6
3	D5	Data Output Bit 5
4	D4	Data Output Bit 4
5	CLK	Clock Input
6	DV_{CC}	Digital Supply Voltage
7	OV_{CC}	Output Buffer Supply Voltage
8	DGND	Digital Ground
9	OF	Output Format/Chip Enable
10	D3	Data Output Bit 3
11	D2	Data Output Bit 2
12	D1	Data Output Bit 1
13	D0	Data Output Bit 0 (LSB)
14	I0	Input Selection Bit 0

PIN	NAME	DESCRIPTION
15	I1	Input Selection Bit 1
16	VIN0	Video Input 0
17	VIN1	Video Input 1
18	VIN2	Video Input 2
19	ANOUT	Analog Output
20	ADCIN	ADC Input
21	DEC	Not Connected – VP8708 is internally stable
22	AV_{CC}	Analog Supply Voltage
23	AGND	Analog Ground
24	CLAMP	Clamp Capacitor
25	AGC	AGC Capacitor
26	GATE B	Black Level Control Pulse
27	GATE A	Sync Level Control Pulse
28	RPEAK	Peak Current Resistor

PCB CONSTRUCTION

As with all high speed analog to digital converters, careful consideration must be given to the PCB layout.

In general, the best results will be obtained by tying all grounds to a 'solid' low impedance ground plane. Separate analog and digital ground planes will also help. Device connections to the ground plane should be as short as possible.

Supply decoupling is important when dealing with mixed analog and digital signals, it can provide a feedback path for the digital output currents. The VP8708 should therefore be decoupled as close to the supply pins as possible. Good quality, high frequency, low inductance capacitors. Isolation may be further improved by adding series inductors to the supplies.

Jitter and noise on the clock pin and its reference to ground must be minimised. Long clock lines should be avoided and all lines correctly terminated.

A typical application circuit is shown below.

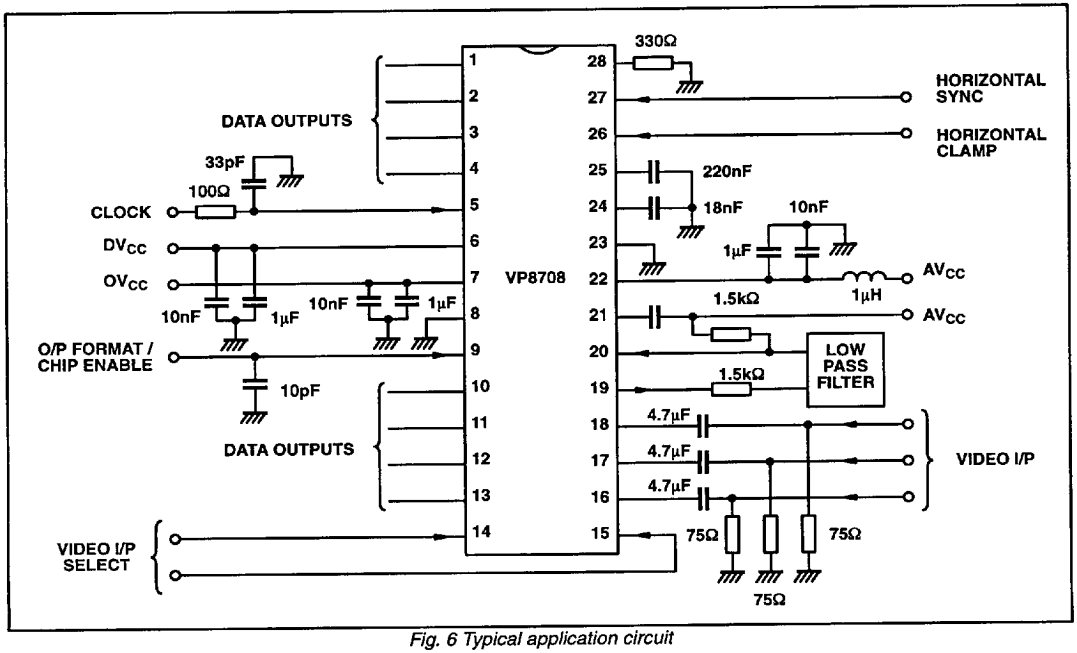

Fig. 6 Typical application circuit