VND5050J-E
VND5050K-E

Double channel high side driver with analog current sense for automotive applications

Features

General

Max supply voltage	V_{CC}	41V
Operating voltage range	V_{CC}	4.5 to 36V
Max On-State resistance (per ch.)	R_{ON}	50 mΩ
Current limitation (typ)	I_{LIMH}	19 A
Off state supply current	I_S	2 µA(*)

(*) Typical value with all loads connected

Application

- All types of resistive, inductive and capacitive loads

Main

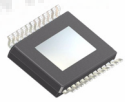
- Inrush current active management by power limitation
- Very low stand-by current
- 3.0V CMOS compatible input
- Optimized electromagnetic emission
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/ec european directive

Diagnostic Functions

- Open drain status output
- On state open load detection
- Off state open load detection
- Thermal shutdown indication

Protections

- Undervoltage shut-down
- Overvoltage clamp
- Output stuck to V_{CC} detection
- Load current limitation

PowerSSO-12 **PowerSSO-24**

- Self limiting of fast thermal transients
- Protection against loss of ground and loss of V_{CC}
- Thermal shut down
- Reverse battery protection (see *Figure 28*)
- Electrostatic discharge protection

Description

The VND5050K-E and VND5050J-E is a monolithic device made using STMicroelectronics VIPower M0-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). The device detects open load condition both in on and off state, when STAT_DIS is left open or driven low. Output shorted to V_{CC} is detected in the off state.

When STAT_DIS is driven high, STATUS pin is in high impedance state.

Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears..

Order codes

Package	Part number (Tube)	Part number (Tape & Reel)
PowerSSO-12	VND5050J-E	VND5050J-E13TR
PowerSSO-24	VND5050K-E	VND5050K-E13TR

Contents

1 Block diagram and pin description

Figure 1. Block Diagram

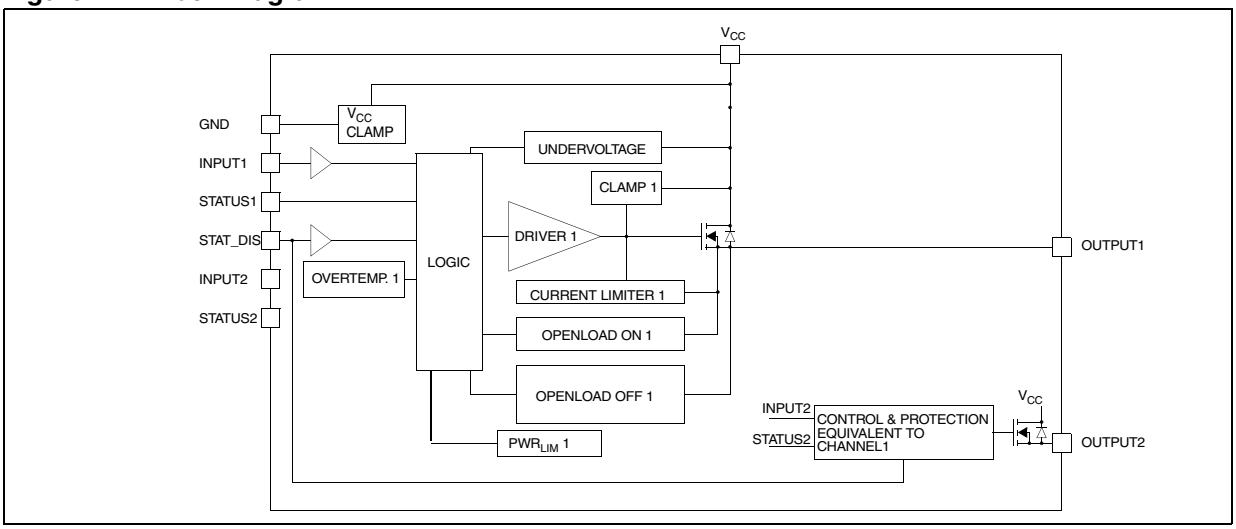
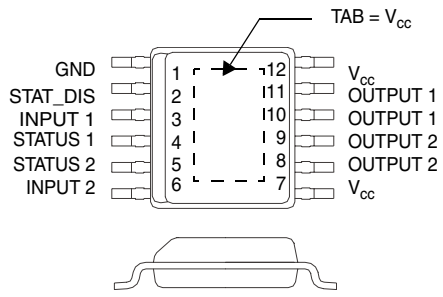


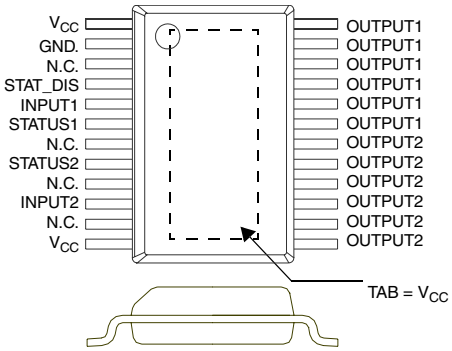
Table 1. Pin Function

Name	Function
V_{CC}	Battery connection
OUTPUTn	Power output
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network
INPUTn	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
STATUSn	Open drain digital diagnostic pin
STAT_DIS	Active high CMOS compatible pin, to disable the STATUS pin

Figure 2. Configuration diagram (top view) & suggested connections for unused and n.c. pins



PowerSSO-12



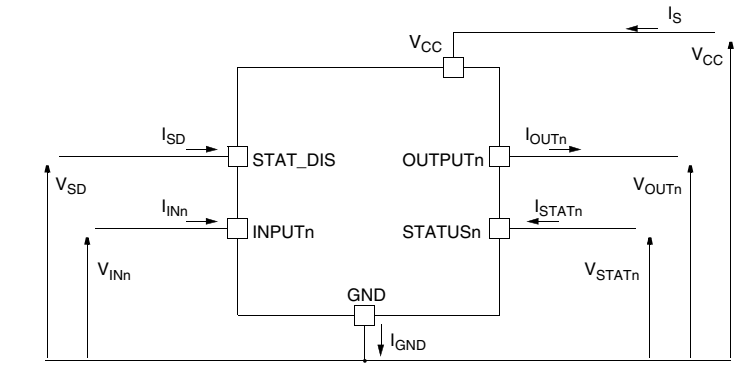
PowerSSO-24

Connection / Pin	Status	N.C.	Output	Input	STAT_DIS
Floating	X	X	X	X	X
To Ground	N.R.	X	N.R.	10KΩ resistor	10KΩ resistor

N.R. = Not recommended

2 Electrical specifications

Figure 3. Current and Voltage Conventions



2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	41	V
- V_{CC}	Reverse DC Supply Voltage	0.3	V
- I_{GND}	DC Reverse Ground Pin Current	200	mA
I_{OUT}	DC Output Current	Internally Limited	A
- I_{OUT}	Reverse DC Output Current	15	A
I_{IN}	DC Input Current	+10 / -1	mA
I_{STAT}	DC Status Current	+10 / -1	mA
I_{STAT_DIS}	DC Status Disable Current	+10 / -1	mA
E_{MAX}	Maximum switching energy (L=1.5mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150ºC; I_{OUT} = I_{limL} *(Typ.)*)	51	mJ
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - STATUS - STAT_DIS - OUTPUT - V_{CC}	 4000 4000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	- 55 to 150	°C

2.2 Thermal Data

Table 3. Thermal Data

Symbol	Parameter	Value		Unit
		PowerSSO-12	PowerSSO-24	
$R_{thj\text{-}case}$	Thermal resistance junction-case (Max.) (with one channel ON)	2.8	2.8	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (Max.)	See *Figure 31*	See *Figure 35*	°C/W

2.3 Electrical Characteristics

8V<V_{CC}<36V; -40°C<T_j<150°C, unless otherwise specified.

Table 4. Power section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
R_{ON}	On state resistance(2)	I_{OUT}=2A; T_j=25°C I_{OUT}=2A; T_j=150°C I_{OUT}=2A; V_{CC}=5V; T_j=25°C			50 100 65	mΩ mΩ mΩ
V_{clamp}	Clamp Voltage	I_S=20mA	41	46	52	V
I_S	Supply current	Off State; V_{CC}=13V; T_j=25°C; V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0V On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A		2(1) 3	5(1) 6	µA mA
$I_{L(off1)}$	Off state output current(2)	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=25°C V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=125°C	0 0	0.01	3 5	µA
$I_{L(off2)}$	Off state output current(2)	V_{IN}=0V; V_{OUT}=4V	-75		0	
V_F	Output - V_{CC} diode voltage(2)	-I_{OUT}=4A; T_j=150°C			0.7	V

(1) PowerMOS leakage included.

(2) For each channel

Table 5. Switching (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L=6.5Ω (see *Figure 5*)		20		µs
$t_{d(off)}$	Turn-off delay time	R_L=6.5Ω (see *Figure 5*)		40		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L=6.5Ω	see *Figure 22*			V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L=6.5Ω	see *Figure 24*			V/µs

Table 5. Switching (V_{CC}=13V) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
W_{ON}	Switching energy losses during t_{won}	R_L=6.5Ω (see *Figure 5*)		0.21		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L=6.5Ω (see *Figure 5*)		0.28		mJ

Table 6. Status Pin (V_{SD}=0V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	I_{STAT}= 1.6 mA, V_{SD}=0V			0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation or V_{SD}=5V, V_{STAT}= 5V			10	µA
C_{STAT}	Status Pin Input Capacitance	Normal Operation or V_{SD}=5V, V_{STAT}= 5V			100	pF
V_{SCL}	Status Clamp Voltage	I_{STAT}= 1mA I_{STAT}= - 1mA	5.5	 -0.7	7	V V

Table 7. Protections (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC Short circuit current	V_{CC}=13V 5V<V_{CC}<36V	12	18	24 24	A A
I_{limL}	Short circuit current during thermal cycling	V_{CC}=13V T_R<T_j<T_{TSD}		7		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
t_{SDL}	Status Delay in Overload Conditions	T_j>T_{TSD} (see *Figure 4*)			20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT}=2A; V_{IN}=0; L=6mH	V_{CC}-41	V_{CC}-46	V_{CC}-52	V
V_{ON}	Output voltage drop limitation	I_{OUT}=0.1A; T_j= -40°C...+150°C (see *Figure 6*)		25		mV

(1) To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Table 8. Openload Detection

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Openload ON State Detection Threshold	V_{IN} = 5V ,8V<V_{CC}<18V	10	See *Figure 19*	70	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	I_{OUT} = 0A, V_{CC}=13V (see *Figure 4*)			200	µs
t_{POL}	Delay between INPUT falling edge and STATUS rising edge in Openload condition	I_{OUT} = 0A (see *Figure 4*)	200	500	1000	µs
V_{OL}	Openload OFF State Voltage Detection Threshold	V_{IN} = 0V, 8V<V_{CC}<16V	2	See *Figure 20*	4	V
t_{DSTKON}	Output Short Circuit to V_{CC} Detection Delay at Turn Off	(see *Figure 4*)	180		t_{POL}	µs

Table 9. Logic input

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level				0.9	V
I_{IL}	Low Level Input Current	V_{IN} =0.9 V	1			µA
V_{IH}	Input High Level		2.1			V
I_{IH}	High Level Input Current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.25			V
V_{ICL}	Input Clamp Voltage	I_{IN} = 1mA I_{IN} = -1mA	5.5	 -0.7	7	V V
V_{SDL}	STAT_DIS low level voltage				0.9	V
I_{SDL}	Low level STAT_DIS current	V_{SD} = 0.9 V	1			µA
V_{SDH}	STAT_DIS high level voltage		2.1			V
I_{SDH}	High level STAT_DIS current	V_{SD} = 2.1 V			10	µA
$V_{SD(hyst)}$	STAT_DIS hysteresis voltage		0.25			V
V_{SDCL}	STAT_DIS clamp voltage	I_{SD}=1mA I_{SD}=-1mA	5.5	 -0.7	7	V V

Figure 4. Status Timings

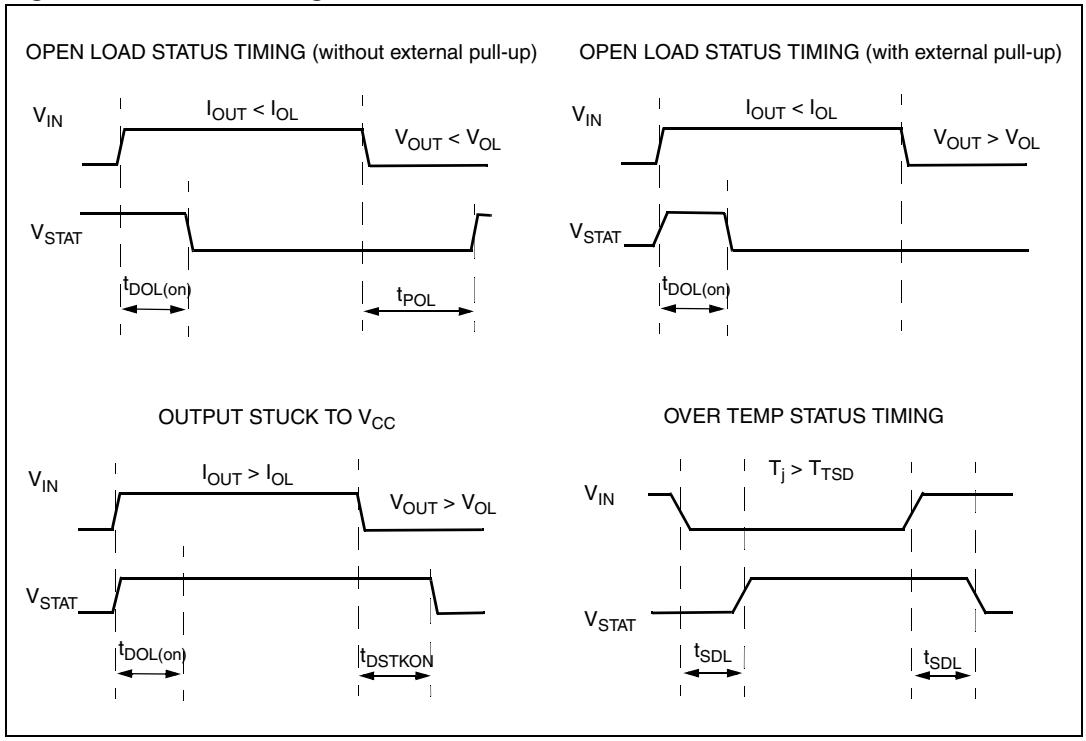


Table 10. Truth table

CONDITIONS	INPUT	OUTPUT	SENSE (V_{CSD}=0V)(1)
Normal Operation	L H	L H	H H
Current Limitation	L H	L X	H H
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Output Voltage > V_{OL}	L H	H H	L(2) H
Output Current < I_{OL}	L H	L H	H (3) L

(1) If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

(2) The STATUS pin is low with a delay equal to tDSTKON after INPUT falling edge.

(3) The STATUS pin becomes high with a delay equal to tPOL after INPUT falling edge.

Figure 5. Switching characteristics

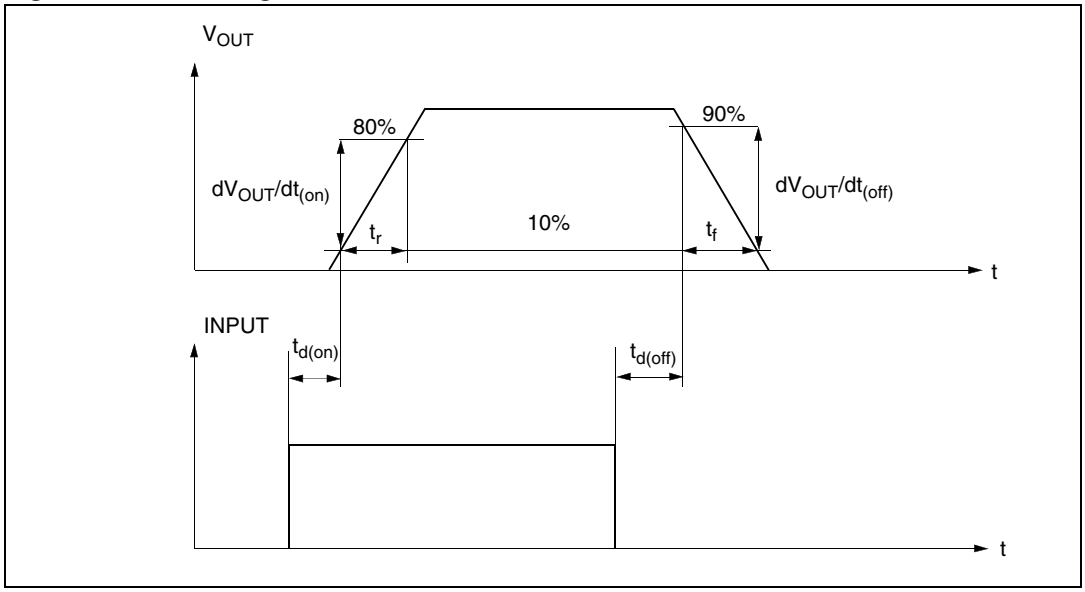


Figure 6. Output Voltage Drop Limitation

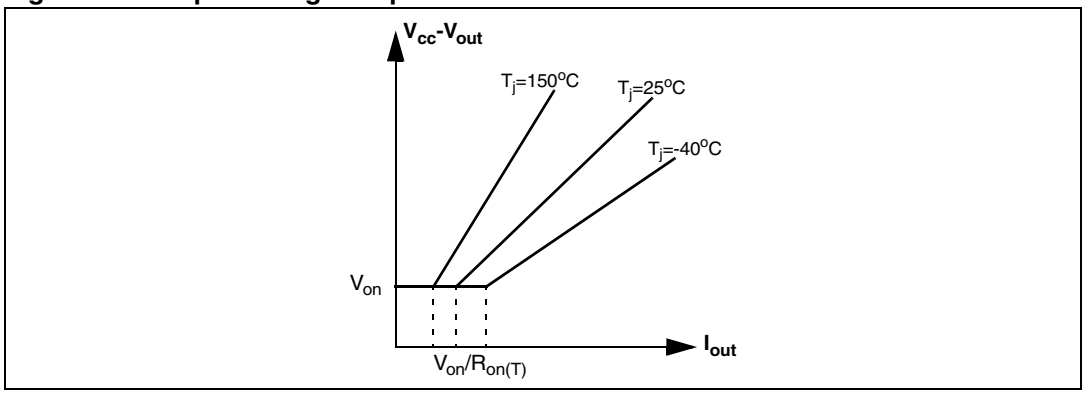


Table 11. Electrical Transient Requirements

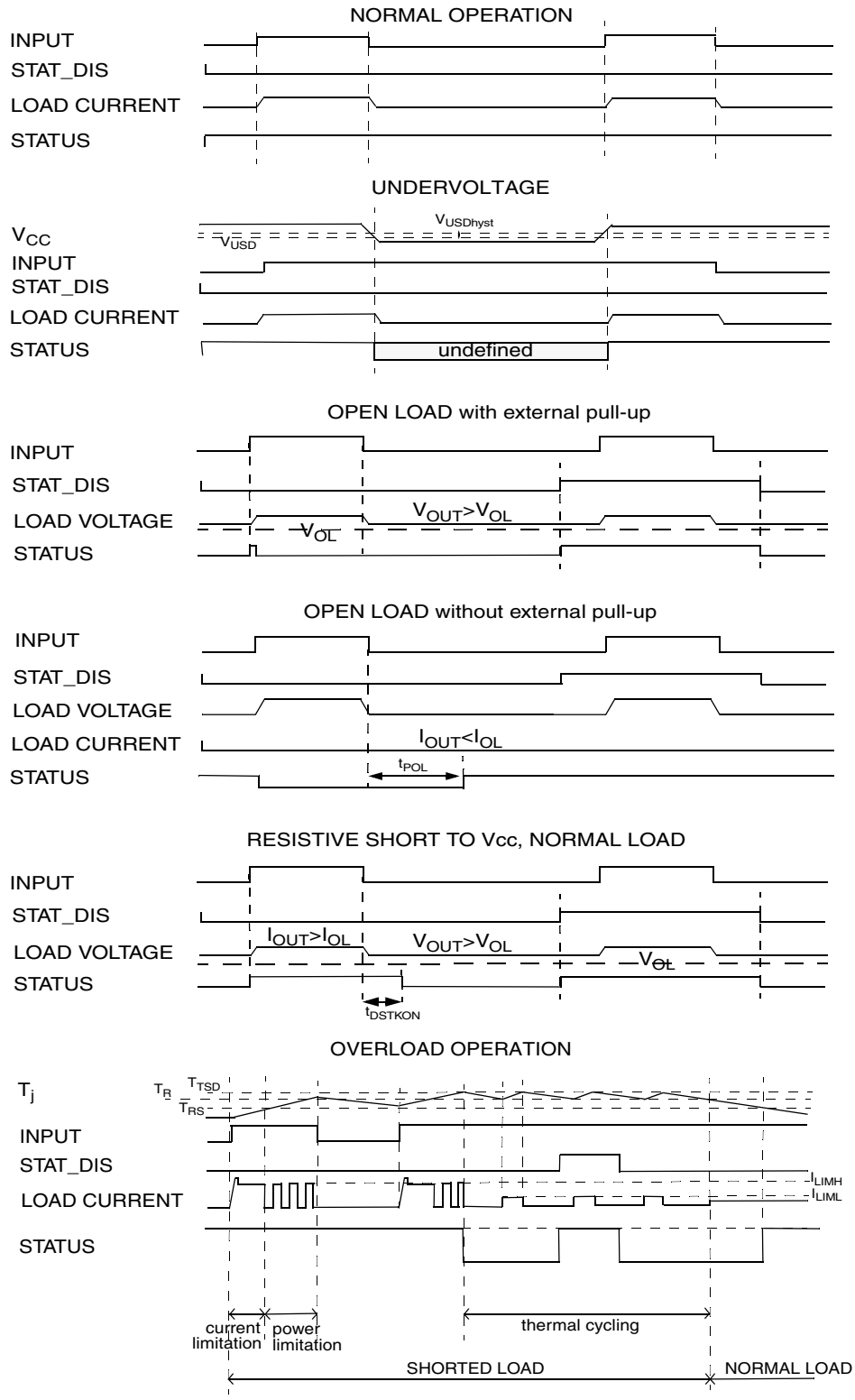
ISO 7637-2: 2004(E) Test Pulse	TEST LEVELS		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6V	-7V	1 pulse			100 ms, 0.01 Ω
5b(1)	+40V	+40V	1 pulse			400 ms, 2 Ω

ISO 7637-2: 2004(E) Test Pulse	TEST LEVEL RESULTS	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(1)	C	C

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

(1) For load dump exceeding the above value a centralized suppressor must be adopted.

Figure 7. Waveforms



2.4 Electrical characteristics curves

Figure 8. Off State Output Current

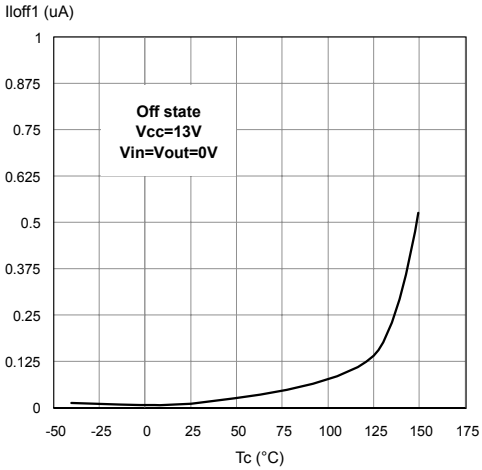


Figure 9. High Level Input Current

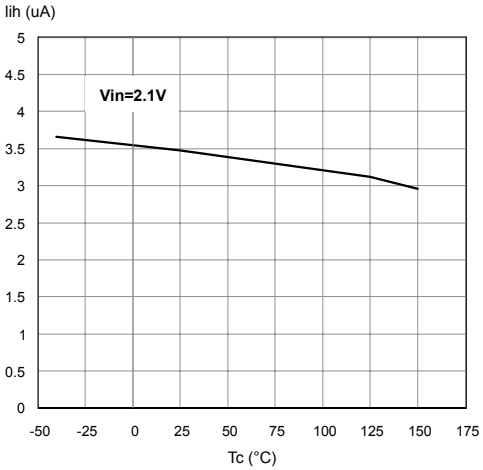


Figure 10. Input Clamp Voltage

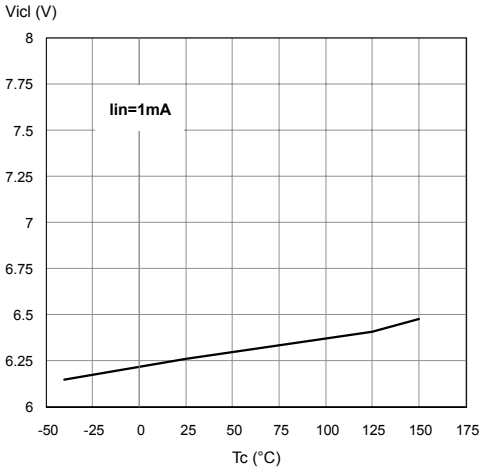


Figure 11. Input High Level

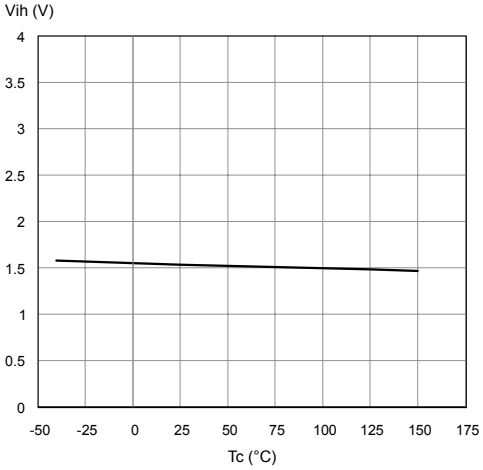


Figure 12. Input Low Level

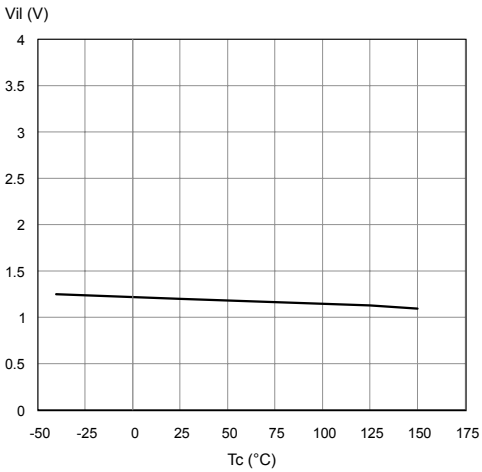


Figure 13. Input Hysteresis Voltage

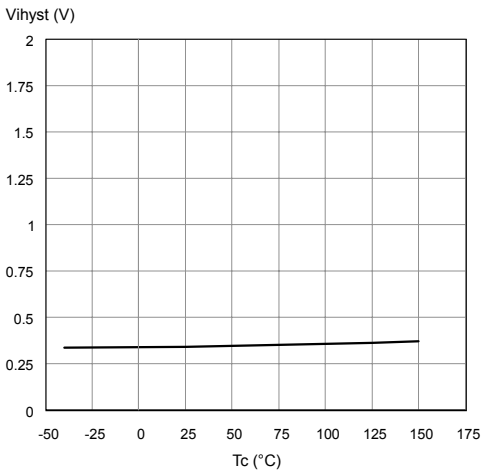


Figure 14. Status Low Output Voltage

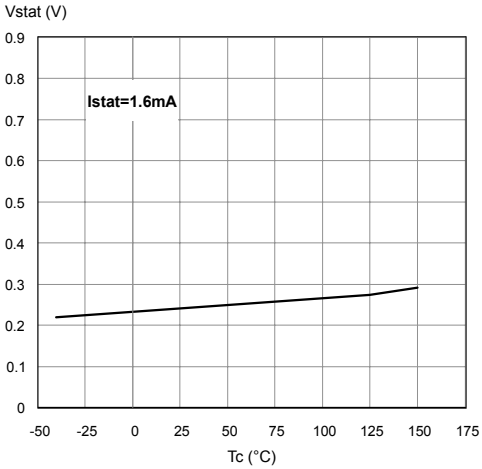


Figure 15. On State Resistance Vs T_{case}

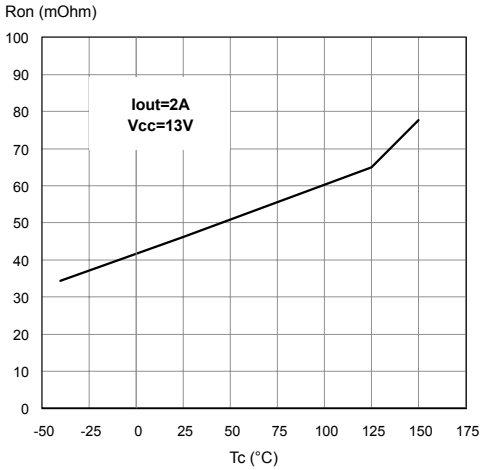


Figure 16. Status Leakage Current

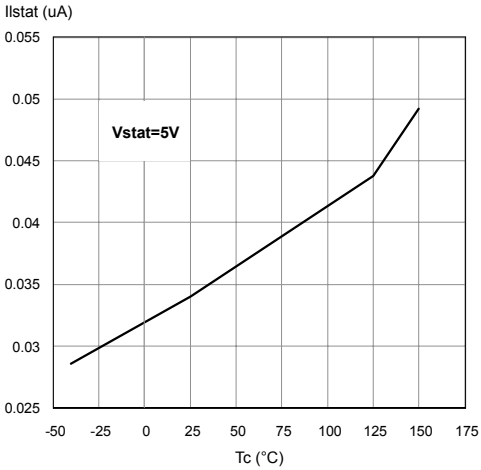


Figure 17. On State Resistance Vs V_{CC}

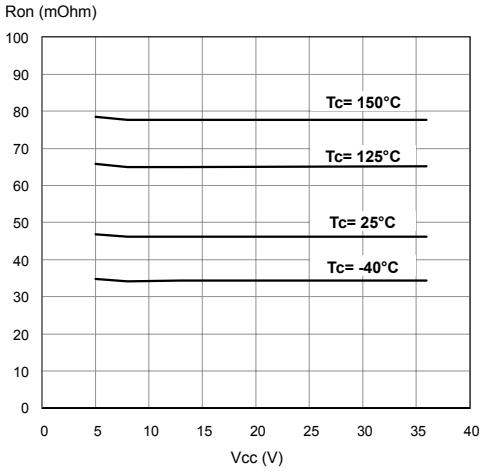


Figure 18. Status Clamp Voltage

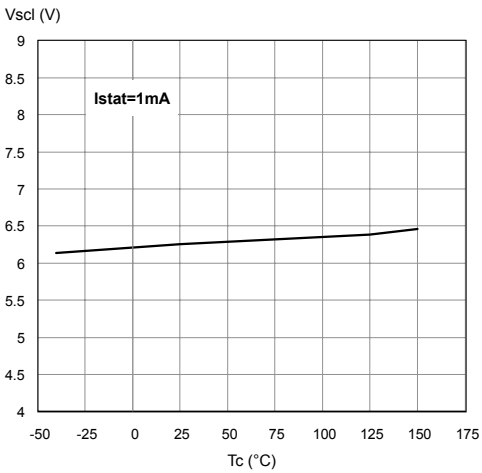


Figure 19. Openload On State Detection Threshold

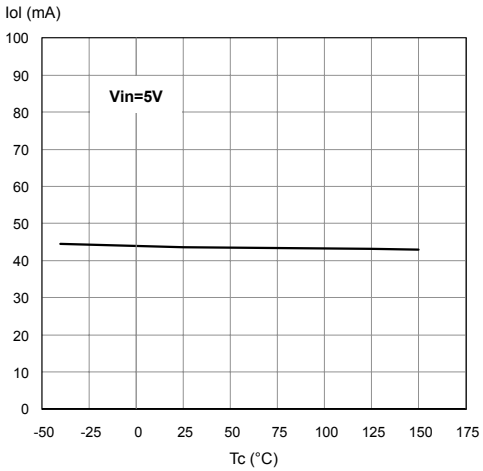


Figure 20. Openload Off State Voltage Detection Threshold

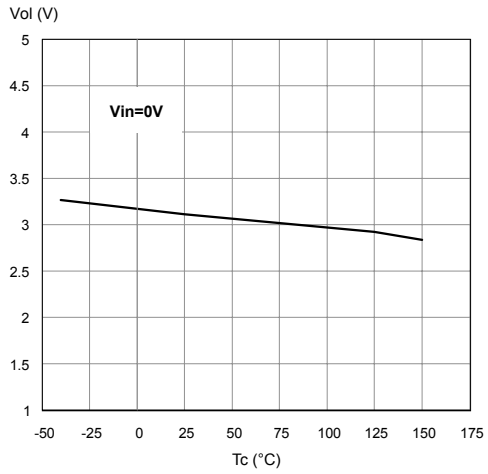


Figure 21. I_{LIM} Vs T_{case}

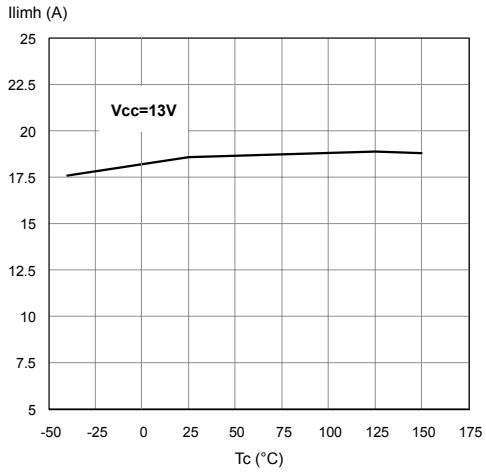


Figure 22. Turn-on Voltage Slope

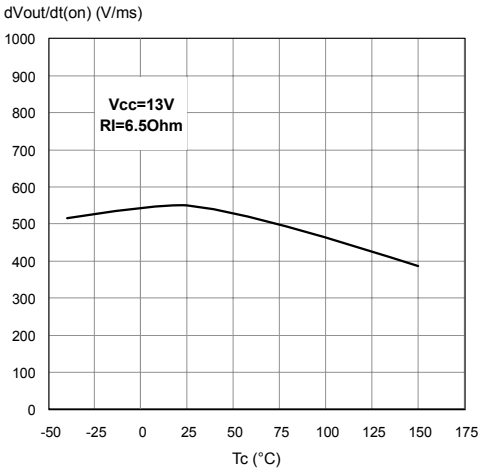


Figure 23. Undervoltage Shutdown

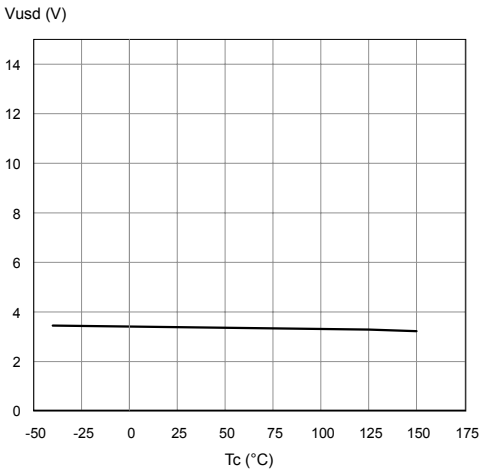


Figure 24. Turn-off Voltage Slope

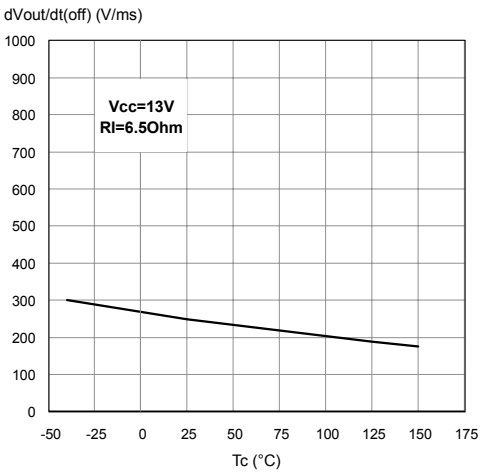


Figure 25. STAT_DIS Clamp Voltage

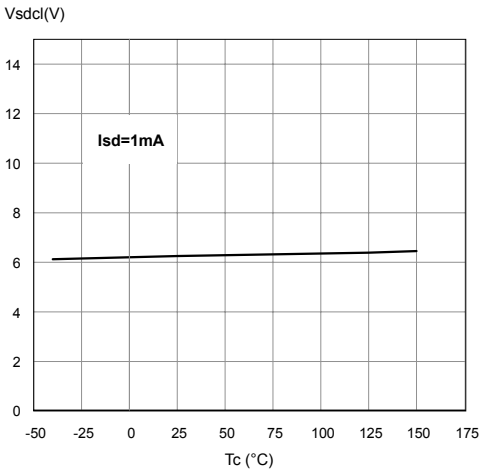


Figure 26. High Level STAT_DIS Voltage

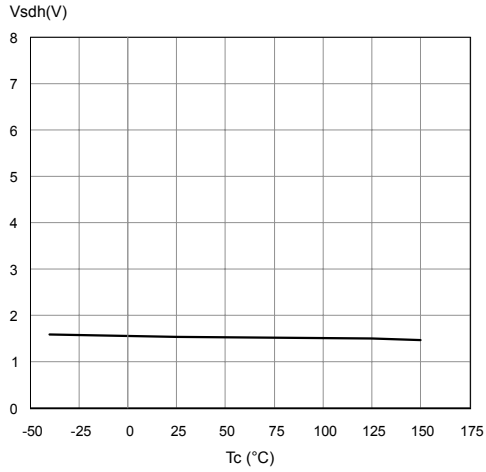
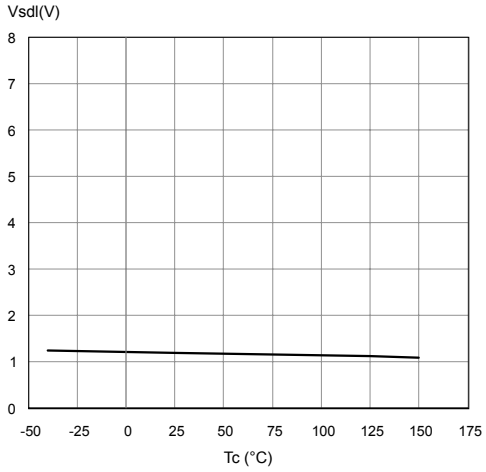
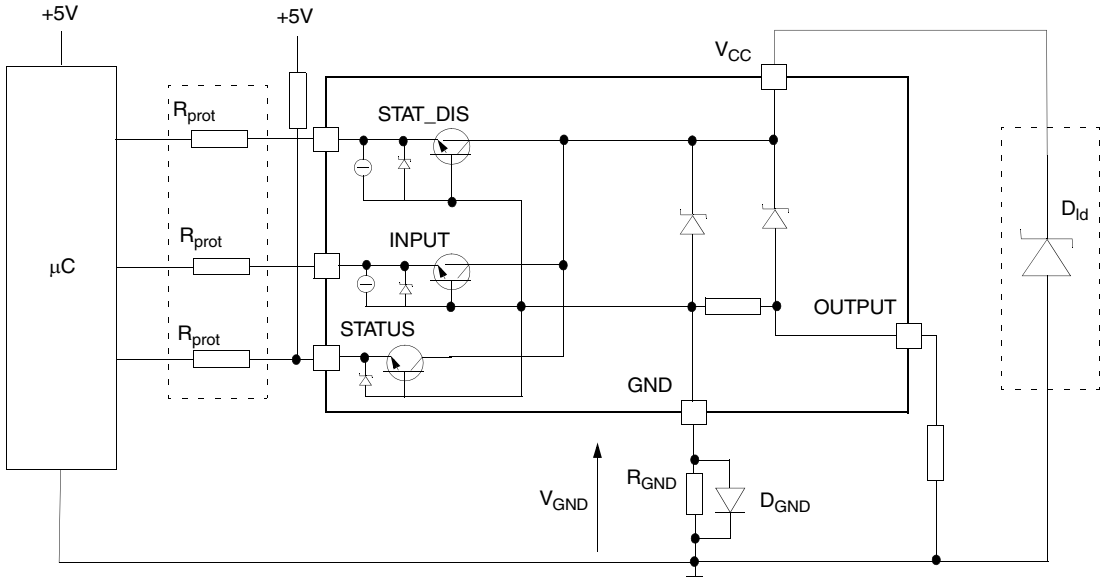


Figure 27. Low Level STAT_DIS Voltage



3 Application information

Figure 28. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

3.1.1 Solution 1:

Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2:

A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 µC I/Os protection:

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5kΩ ≤ R_{prot} ≤ 180kΩ.

Recommended values: R_{prot} =10kΩ, C_{EXT}=10nF.

3.4 Open load detection in off state

Off state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

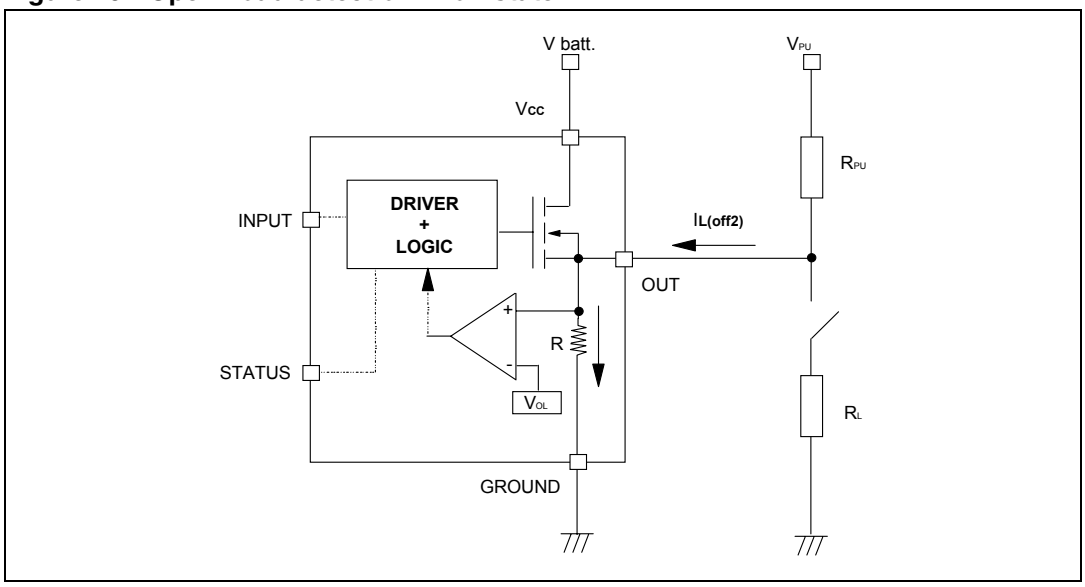
The external resistor has to be selected according to the following requirements:

1. no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{Olmin}; this results in the following condition $V_{OUT}=(V_{PU}/(R_L+R_{PU}))R_L<V_{Olmin}$.
2. no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition $R_{PU}<(V_{PU}–V_{OLmax})/I_{L(off2)}$.

Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

The values of V_{OLmin}, V_{OLmax} and $I_{L(off2)}$ are available in the Electrical Characteristics section.

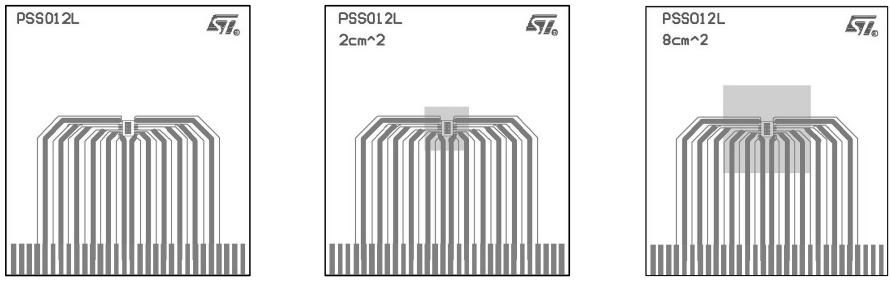
Figure 29. Open Load detection in off state



4 Package and PCB thermal data

4.1 PowerSSO-12 thermal data

Figure 30. PowerSSO-12 PC Board



Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70µm (front and back side), Copper areas: from minimum pad lay-out to 8cm^2).

Figure 31. $R_{thj\text{-}amb}$ Vs. PCB copper area in open box free air condition

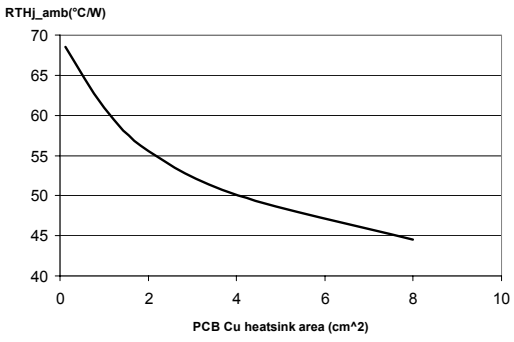
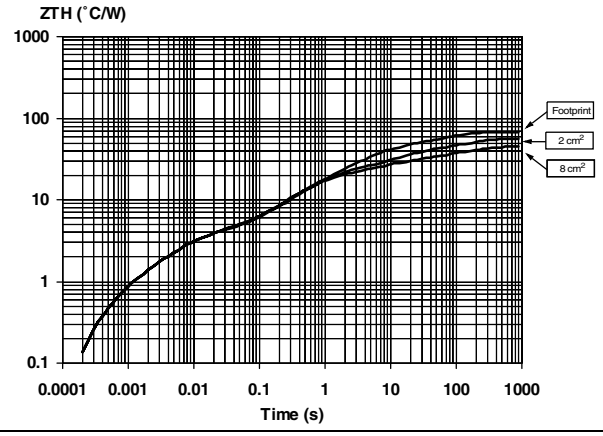


Figure 32. PowerSSO-12 Thermal Impedance Junction Ambient Single Pulse

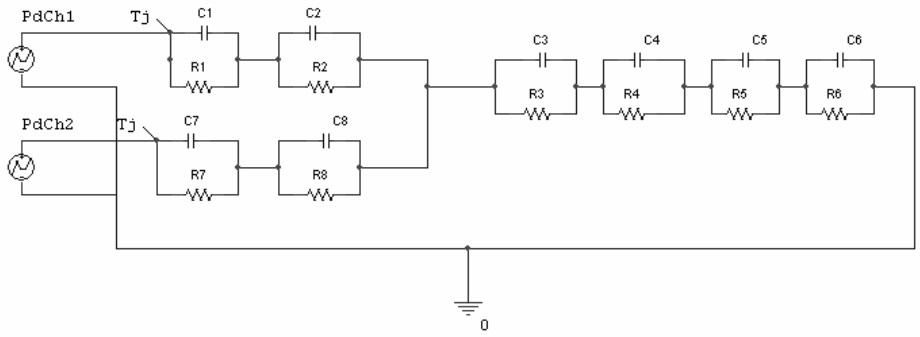


Pulse Calculation Formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 33. Thermal Fitting Model of a Double Channel HSD in PowerSSO-12

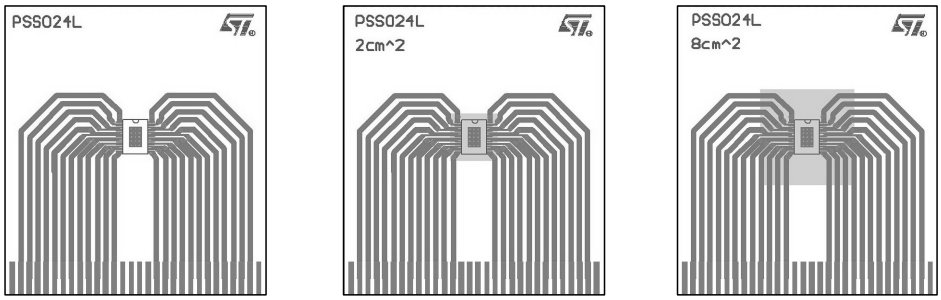


Thermal Parameter

Area/island (cm^2)	Footprint	2	8
R1=R7 (°C/W)	0.7		
R2=R8 (°C/W)	2.8		
R3 (°C/W)	7		
R4 (°C/W)	10	10	9
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1=C7 (W.s/°C)	0.001		
C2=C8 (W.s/°C)	0.0025		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

4.2 PowerSSO-24 thermal data

Figure 34. PowerSSO-24 PC Board



Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70µm (front and back side), Copper areas: from minimum pad lay-out to 8cm^2).

Figure 35. $R_{thj\text{-}amb}$ Vs. PCB copper area in open box free air condition

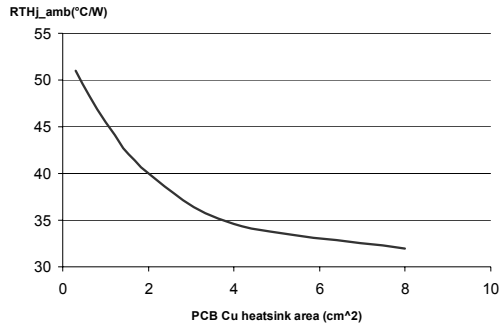
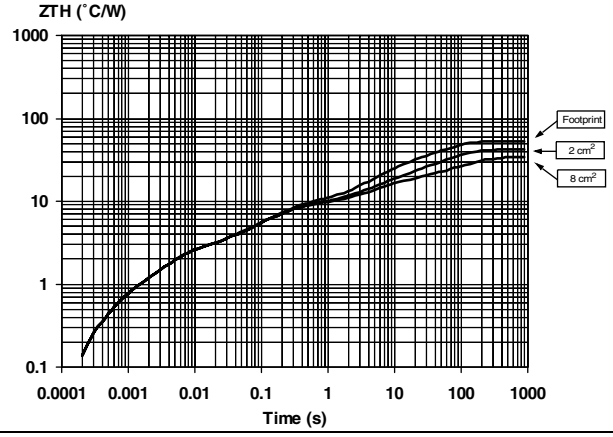


Figure 36. PowerSSO-24 Thermal Impedance Junction Ambient Single Pulse

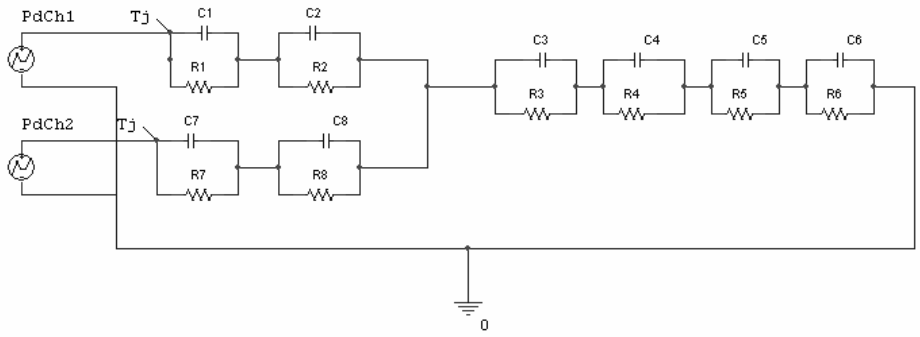


Pulse Calculation Formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 37. Thermal Fitting Model of a Single Channel HSD in PowerSSO-12



Thermal Parameter

Area/island (cm^2)	Footprint	2	8
R1=R7 (°C/W)	0.4		
R2=R8 (°C/W)	2		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1=C7 (W.s/°C)	0.001		
C2=C8 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

5 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.
The maximum ratings related to soldering conditions are also marked on the inner box label.
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5.1 Package Mechanical

Figure 38. PowerSSO-12™ Package Dimensions

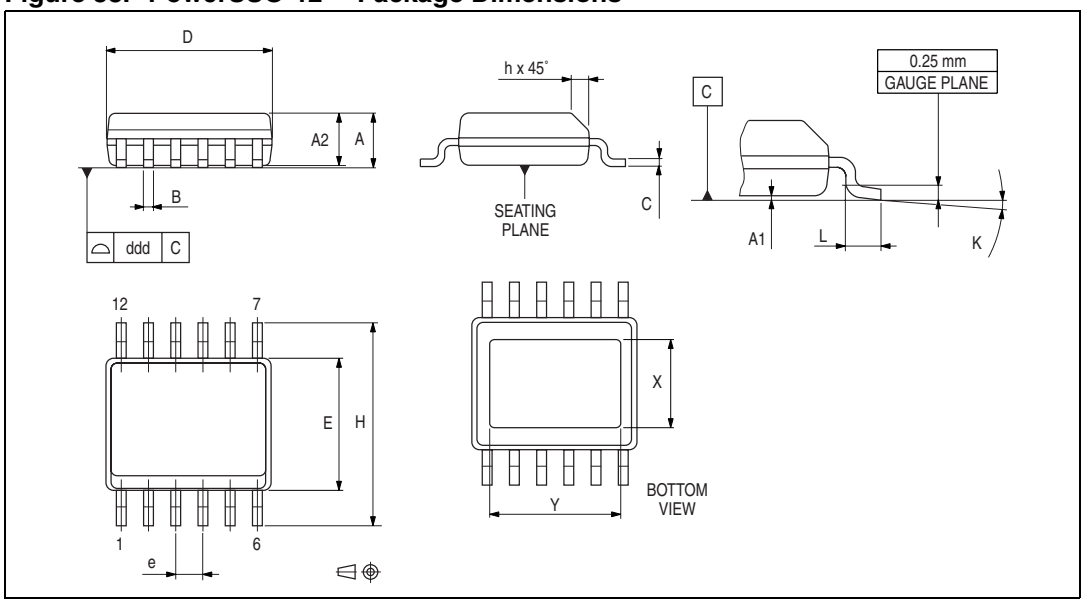


Table 12. PowerSSO-12™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

Figure 39. PowerSSO-24™ Package Dimensions

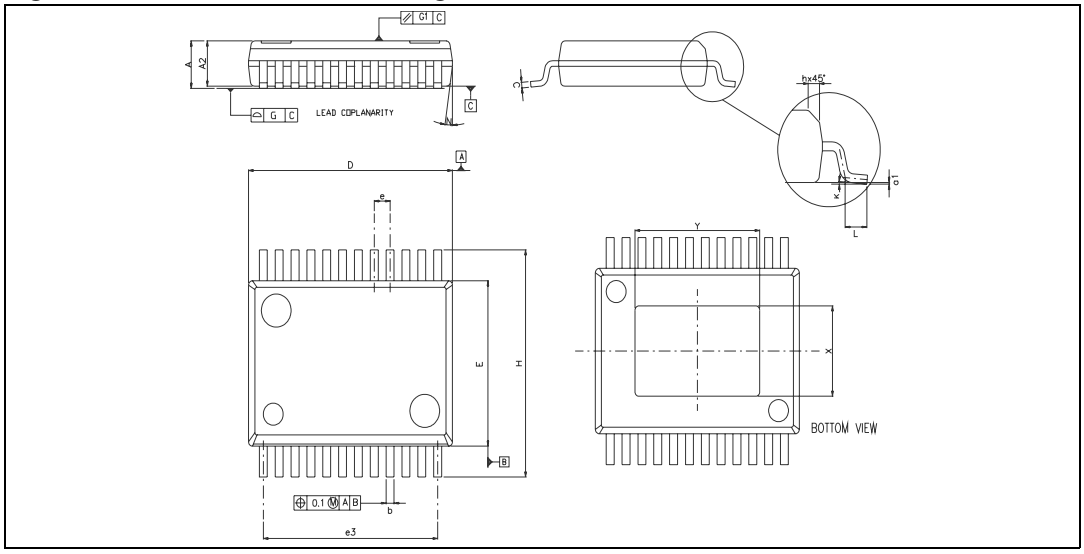
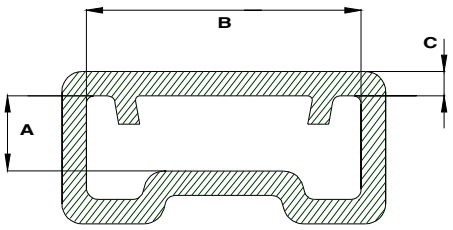


Table 13. PowerSSO-24™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

5.2 Packing information

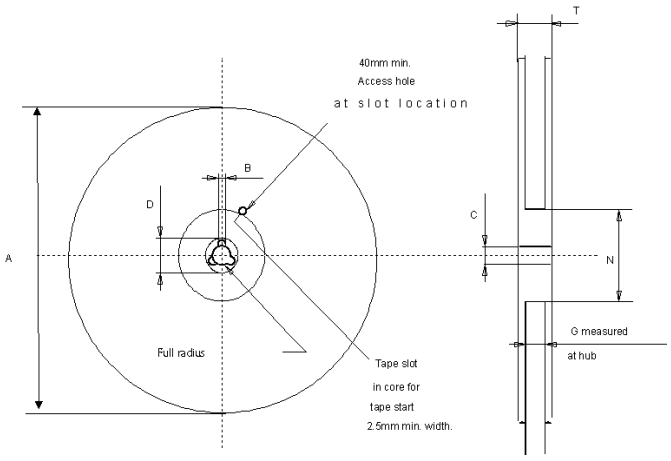
Figure 40. PowerSSO-12 Tube Shipment (No Suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

All dimensions are in mm.

Figure 41. PowerSSO-12 Tape And Reel Shipment (Suffix "TR")



REEL DIMENSIONS

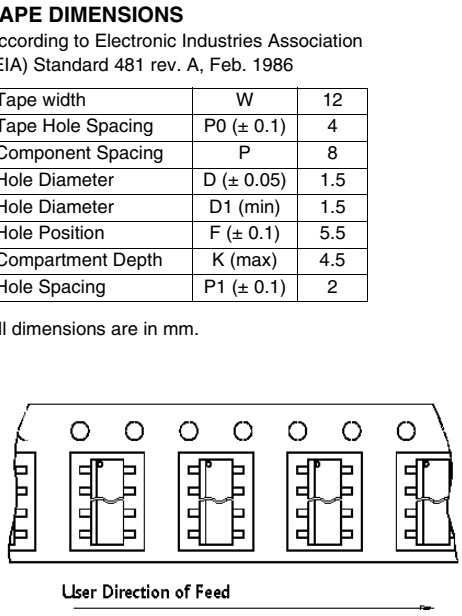
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D (± 0.05)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.1)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



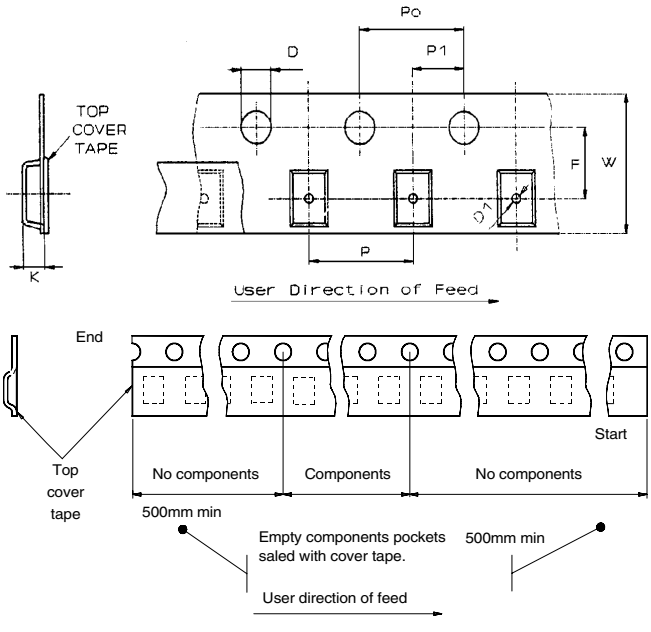
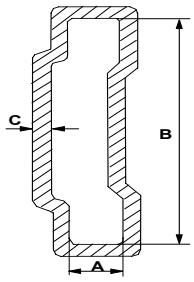


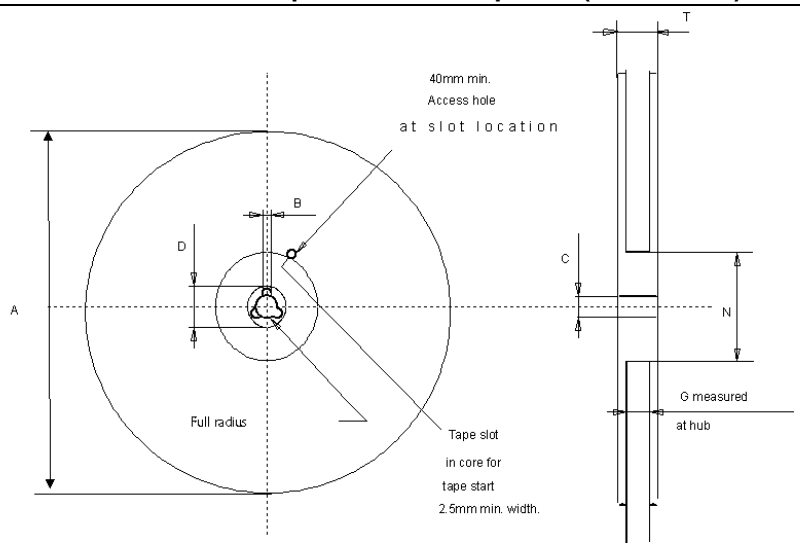
Figure 42. PowerSSO-24 Tube Shipment (No Suffix)



Base Q.ty	49
Bulk Q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 43. PowerSSO-24 Tape And Reel Shipment (Suffix "TR")



REEL DIMENSIONS

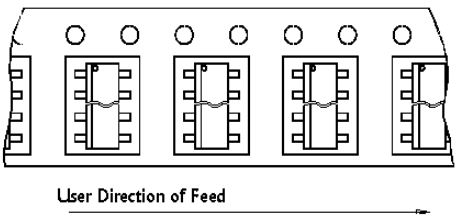
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	100
T (max)	30.4

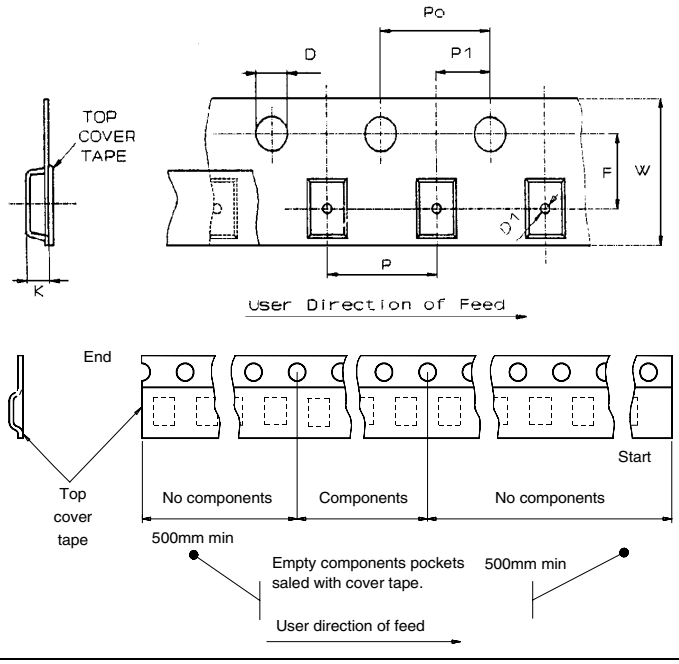
TAPE DIMENSIONS

According to Electronic Industries Association
(EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.





6 Revision history

Table 14. Document revision history

Date	Revision	Changes
30-Mar-2006	1	Initial release.

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