Siliconix incorporated

VN67 SERIES

N-Channel Enhancement-Mode MOS Transistors

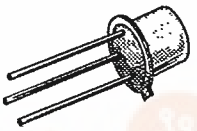
T-39-05

PRODUCT SUMMARY

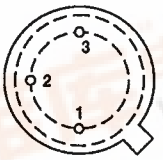
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN67AB	60	3.5	0.79	TO-205AD
VN67AD	60	3.5	1.58	TO-220
VN67AFD	60	3.5	1.37	TO-220SD

Performance Curves: VNDQ06 (See Section 7)

TO-205AD (TO-39)



BOTTOM VIEW

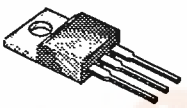


1 SOURCE
2 GATE
3 DRAIN & CASE

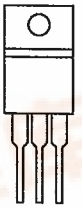
TO-220
1 GATE
2 & TAB – DRAIN
3 SOURCE

TO-220SD
1 SOURCE
2 GATE
3 & TAB – DRAIN

TO-220/TO-220SD



TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted) [2]

PARAMETERS/TEST CONDITIONS		SYMBOL	VN67AB	VN67AD	VN67AFD	UNITS
Drain-Source Voltage		V_{DS}	60	60	60	V
Gate-Source Voltage		V_{GS}	±20	±30	±30	
Continuous Drain Current	T_C = 25°C	I_D	0.79	1.58	1.37	A
	T_C = 100°C		0.5	1	0.87	
Pulsed Drain Current [1]		I_{DM}	3	3	3	
Power Dissipation	T_C = 25°C	P_D	5	20	15	W
	T_C = 100°C		2	8	6	
Operating Junction and Storage Temperature		T_J, T_{stg}	−55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN67AB	VN67AD	VN67AFD	UNITS
Junction-to-Case	R_{thJC}	25	6.25	8.3	°C/W

[1] Pulse width limited by maximum junction temperature
[2] Absolute maximum ratings have been revised from previous data sheet

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VN67 SERIES

T-39-05

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN67[4]		
PARAMETER	SYMBOL	TEST CONDITIONS[4]	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	± 1		±100	nA
		T_C = 125°C	± 5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	0.05		10	µA
		V_{DS} = 48 V, T_C = 125°C	0.3		500	µA
On-State Drain Current[3]	I_D	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.8		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		3.5	Ω
		T_C = 125°C	2.6		7	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}		25		40	pF
Reverse Transfer Capacitance	C_{rss}		5		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω	8		15	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	9.5		15	ns

NOTES: 1. T_C = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. Data sheet limits and/or test conditions have been revised.