



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information
Standard Commercial Devices

| BV _{DSS} / BV _{DGS} | R _{DS(ON)} (max) | I _{D(ON)} (min) | Order Number / Package | |
|---------------------------------------|---------------------------|--------------------------|------------------------|----------|
| | | | TO-39 | TO-92 |
| 200V | 10Ω | 0.4A | VN0120N2 | VN0120N3 |

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

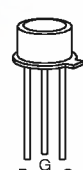
| | |
|-----------------------------------|-------------------|
| Drain-to-Source Voltage | BV _{DSS} |
| Drain-to-Gate Voltage | BV _{DGS} |
| Gate-to-Source Voltage | ± 20V |
| Operating and Storage Temperature | -55°C to +150°C |
| Soldering Temperature* | 300°C |

Advanced DMOS Technology


These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-39
Case: DRAIN



TO-92

Note: See Package Outline section for dimensions.



Thermal Characteristics

| Package | I_D (continuous)* | I_D (pulsed) | Power Dissipation @ $T_C = 25^\circ\text{C}$ | θ_{jc} $^\circ\text{C/W}$ | θ_{ja} $^\circ\text{C/W}$ | I_{DR}^* | I_{DRM} |
|---------|---------------------|----------------|---|-------------------------------------|-------------------------------------|------------|-----------|
| TO-39 | 350mA | 1.0A | 3.5W | 35 | 125 | 350mA | 1.0A |
| TO-92 | 250mA | 0.9A | 1.0W | 125 | 170 | 250mA | 0.9A |

* I_D (continuous) is limited by max rated T_j .

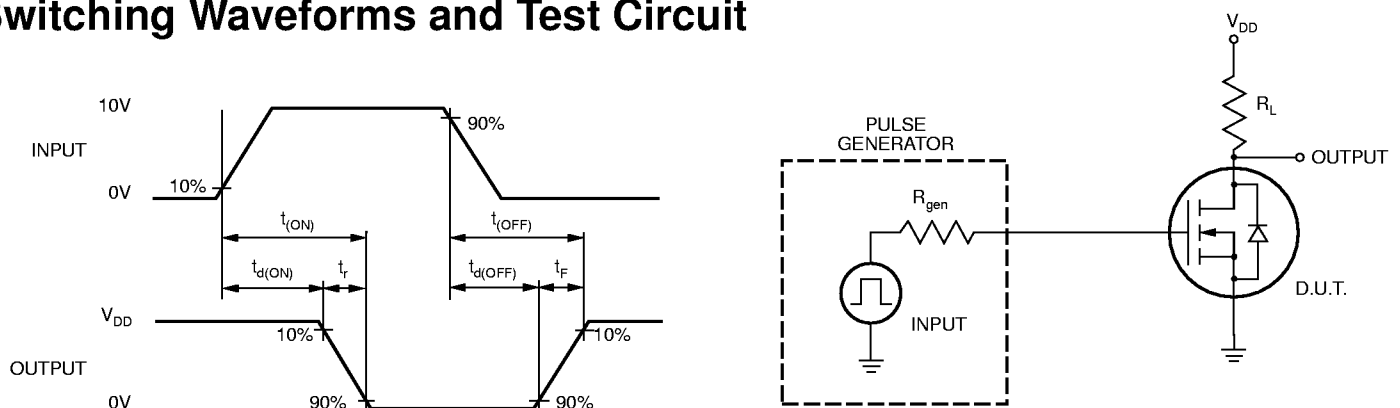
Electrical Characteristics (@ 25°C unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|---------------------|--|-----|------|------|-----------------------|---|
| BV_{DSS} | Drain-to-Source Breakdown Voltage | 200 | | | V | $V_{GS} = 0V, I_D = 1mA$ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1 | | 3 | V | $V_{GS} = V_{DS}, I_D = 1mA$ |
| $\Delta V_{GS(th)}$ | Change in $V_{GS(th)}$ with Temperature | | -5.1 | -6.0 | mV/ $^\circ\text{C}$ | $V_{GS} = V_{DS}, I_D = 1mA$ |
| I_{GSS} | Gate Body Leakage | | | 100 | nA | $V_{GS} = \pm 20V, V_{DS} = 0V$ |
| I_{DSS} | Zero Gate Voltage Drain Current | | | 10 | μA | $V_{GS} = 0V, V_{DS} = \text{Max Rating}$ |
| | | | | 1 | mA | $V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$ |
| $I_{D(ON)}$ | ON-State Drain Current | 0.3 | 0.6 | | A | $V_{GS} = 5V, V_{DS} = 25V$ |
| | | 0.4 | 0.9 | | | $V_{GS} = 10V, V_{DS} = 25V$ |
| $R_{DS(ON)}$ | Static Drain-to-Source ON-State Resistance | | 10 | 15 | Ω | $V_{GS} = 5V, I_D = 100mA$ |
| | | | 8.0 | 10 | | $V_{GS} = 10V, I_D = 100mA$ |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with Temperature | | 1.0 | 1.2 | %/ $^\circ\text{C}$ | $V_{GS} = 10V, I_D = 100mA$ |
| G_{FS} | Forward Transconductance | 100 | | | $\text{m}\mathcal{U}$ | $V_{DS} = 25V, I_D = 250mA$ |
| C_{ISS} | Input Capacitance | | 45 | 55 | pF | $V_{GS} = 0V, V_{DS} = 25V$ $f = 1 \text{ MHz}$ |
| C_{OSS} | Common Source Output Capacitance | | 20 | 30 | | |
| C_{RSS} | Reverse Transfer Capacitance | | 5 | 8 | | |
| $t_{d(ON)}$ | Turn-ON Delay Time | | 3 | 5 | ns | $V_{DD} = 25V,$ $I_D = 1A,$ $R_{GEN} = 25\Omega$ |
| t_r | Rise Time | | 5 | 8 | | |
| $t_{d(OFF)}$ | Turn-OFF Delay Time | | 6 | 9 | | |
| t_f | Fall Time | | 5 | 8 | | |
| V_{SD} | Diode Forward Voltage Drop | | 1.2 | 1.8 | V | $V_{GS} = 0V, I_{SD} = 1.0A$ |
| t_{rr} | Reverse Recovery Time | | 400 | | ns | $V_{GS} = 0V, I_{SD} = 1.0A$ |

Notes:

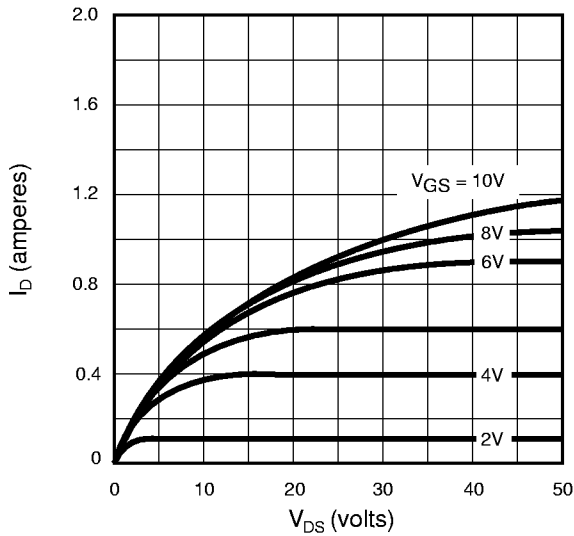
- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: $300\mu\text{s}$ pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

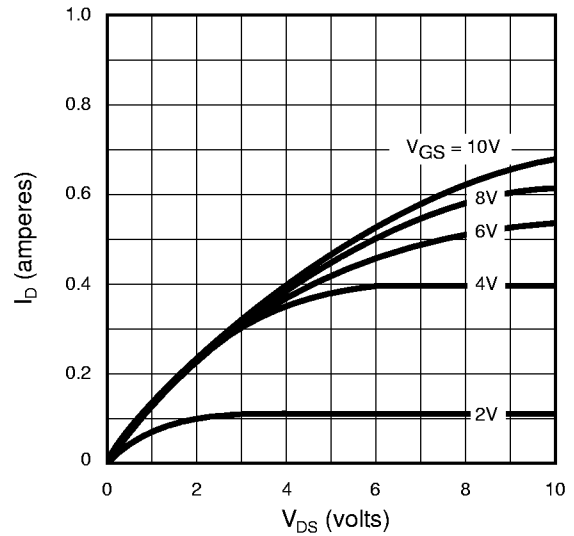


Typical Performance Curves

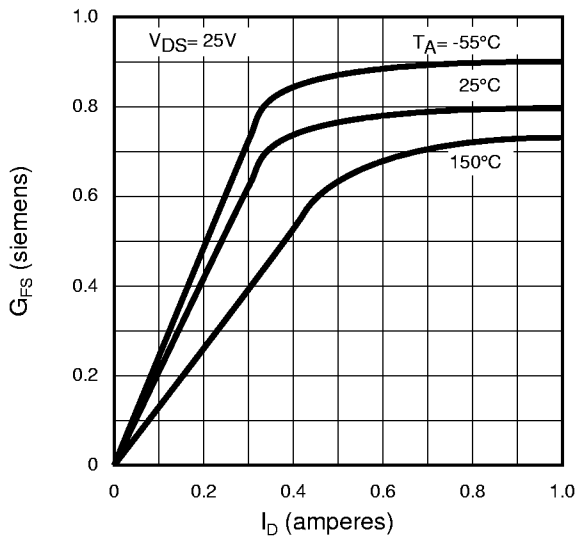
Output Characteristics



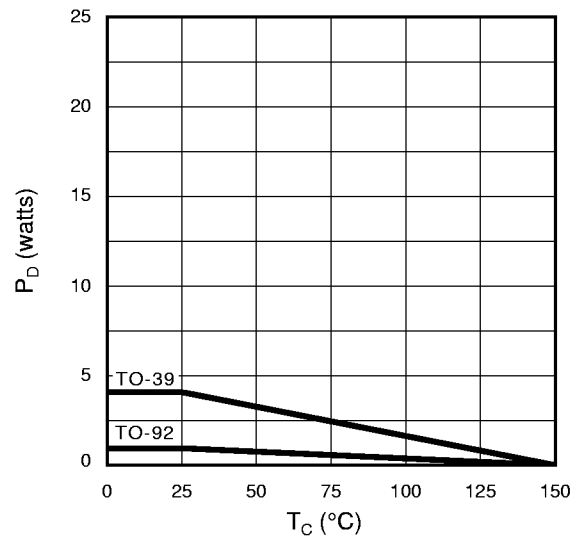
Saturation Characteristics



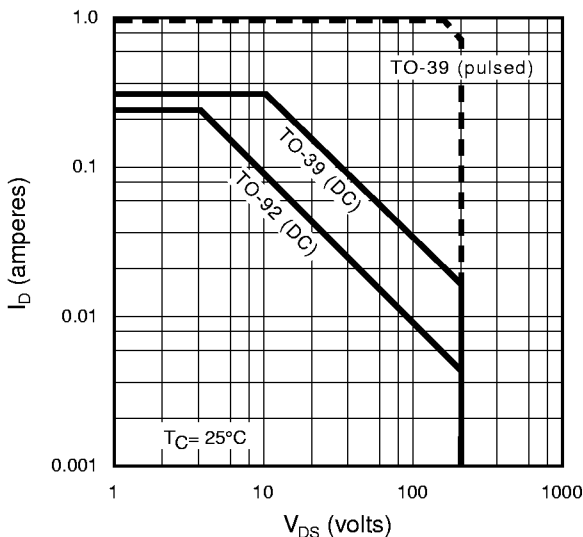
Transconductance vs. Drain Current



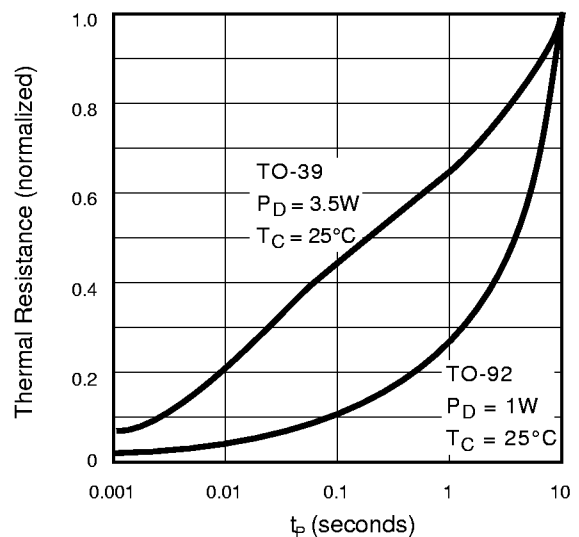
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

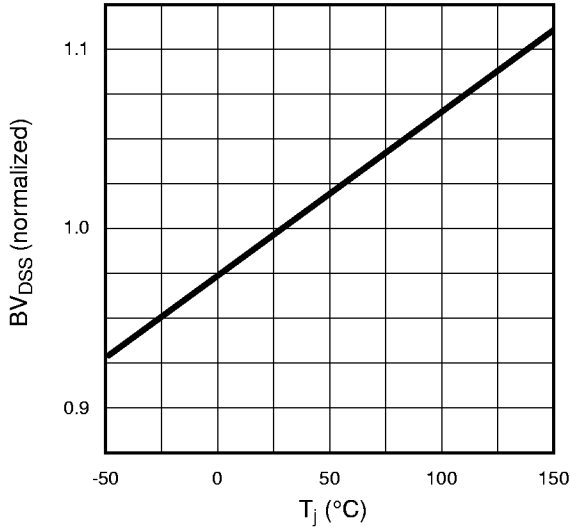


Thermal Response Characteristics

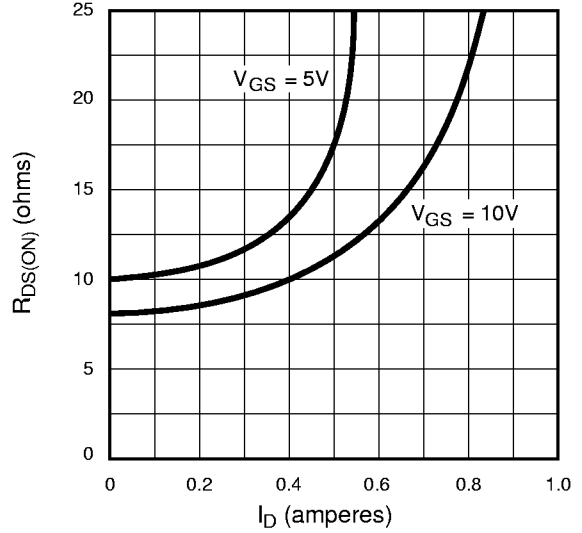


Typical Performance Curves

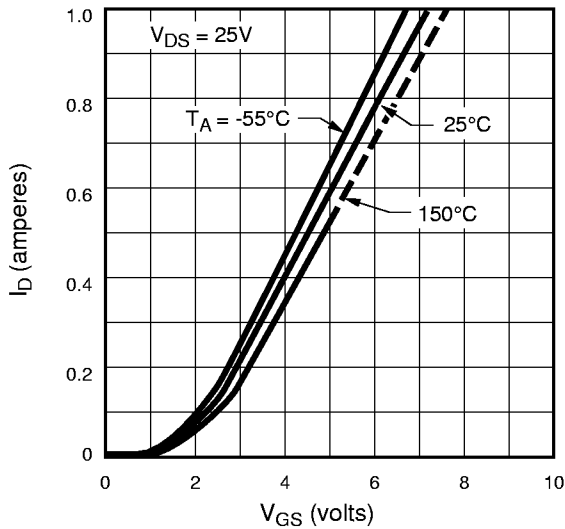
BV_{DSS} Variation with Temperature



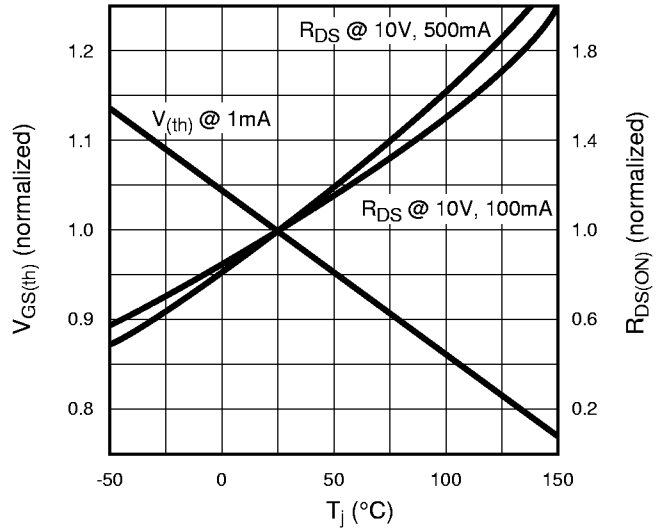
On-Resistance vs. Drain Current



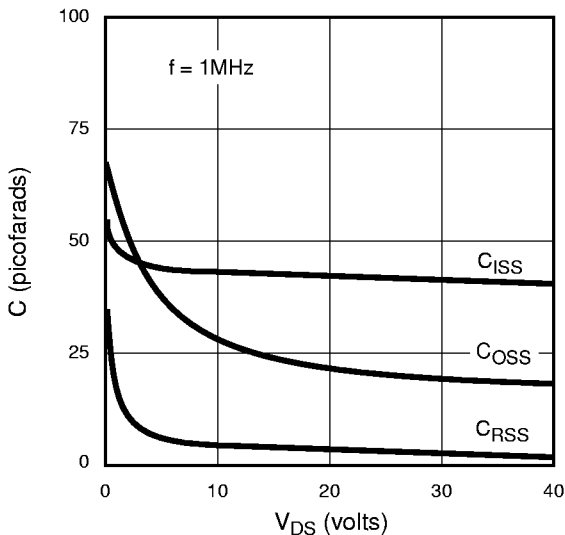
Transfer Characteristics



V_(th) and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

