VME 2000

VMEbus
Slave Module Interface Device

December 1990

Distinctive Features

- **Provides logic, high current drive and buffers for slave module to VMEbus interface in 300 mil 24 pin DIP or 28 pin LCC package**
- **Supports Address Pipelining and Block Move Transfers**
- **Slave module selection in any VMEbus address space**
- **Drives 48mA VMEbus DTACK* and BERR* signals**
- **Input hysteresis filters bus noise**
- **Available in Commercial, Industrial and Military temperature ranges**

Programmable Version Available

If the VME 2000 does not match the requirements of the design, a programmable version is available (the PLX 448) which allows the user to customize all inputs, outputs and logic. Programming is performed using industry standard tools such as ABEL™ or CUPL™ software and commonly available PLD programming hardware. Contact PLX for a data sheet on the PLX 448 and other information.

Applications

- **Bus interface circuitry for VMEbus slave modules such as memories or I/O devices**

General Description

The VME 2000 is a CMOS device which incorporates most of the logic required to interface a slave module, such as a memory or an I/O device, to the VMEbus. It is packaged in a compact 24 pin 300 mil wide DIP or 28 pin LCC. In a VMEbus system, the slave responds to a master and transfers data to and from a master. The protocols of the VME 2000 meet the VMEbus specification IEEE 1014 timing requirements. The device buffers and drives the VMEbus signals to the IEEE 1014 electrical specifications.

The VME 2000 supports address pipelining and block move data transfers. This part will function with any type of master module that meets the VMEbus specifications.

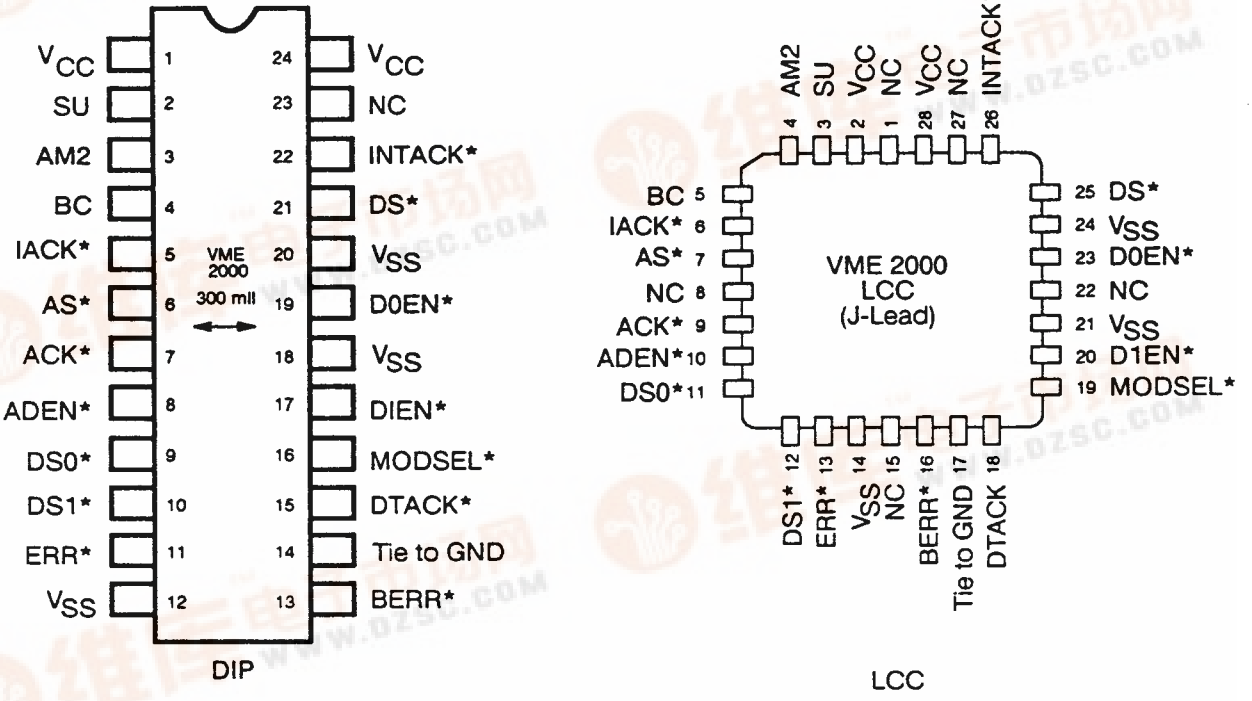


Figure 1. Pinout of VME 2000

Patent Pending
ABEL is a trademark of Data I/O Corp
CUPL is a trademark of Logical Devices, Inc.

PLX Technology, Inc., 625 Clyde Avenue, Mountain View, CA 94043 (415) 960-0448 FAX (415) 960-0479

Pin Description

28Pin LCC	24Pin DIP	Signal	Type	Function
2	1	V_{CC}	–	5V Power Supply
3	2	SU	I	Active high, supervisor/user; when high, supervisor only transfers, when low, supervisor or non-supervisor modes (user)
4	3	AM2	I	Address modifier bit 2, for address size, cycle type
5	4	BC	I	BERR* control, when high VME 2000 asserts BERR* if non-supervisor accesses are attempted when device is supervisor mode only, when low, BERR* control is disabled
6	5	IACK*	I	Interrupt Acknowledge, denotes interrupt command
7	6	AS*	I	Active low, Address Strobe, indicates valid address on bus
9	7	ACK*	I	Active low, Data Acknowledge, local slave strobes ACK* to indicate data is available or accepted during read or write
10	8	ADEN*	I	Active low, Address Enable, enable output from Address decoder
11	9	DS0*	I	Active low, Data Strobe 0
12	10	DS1*	I	Active low, Data Strobe 1, Data strobes indicate how many bytes are being transferred and indicate valid data on bus
13	11	ERR*	I	Local Error
14	12	V_{SS}	–	Chip Ground
16	13	BERR*	I/O	Active low, Bus Error, indicates data transfer was not complete. 48mA open collector
17	14		I	Tie to GND
18	15	DTACK*	I/O	Active low, Data Transfer Acknowledge, handshake to master indicating data is available or accepted during read or write, 48mA open collector
19	16	MODSEL*	O	Active low, Module Select, the local slave module is selected if ADEN in enabled and AM codes match
20	17	DIEN*	O	Active low, Data One enable, upper case data byte enable
21	18	V_{SS}	–	Chip Ground
23	19	D0EN*	O	Active low, Data Zero Enable, lower case data byte enable
24	20	V_{SS}	–	Chip Ground
25	21	DS*	O	Active low, D0EN* or D1EN* active enables DS*
26	22	INTACK*	I	Active low, Interrupt Acknowledge, from local slave's interrupt generator. When low, indicates interrupt cycle for this slave and enables MODSEL*
27	23	NC	I	No Connect
28	24	V_{CC}	–	5V power supply
1, 8 15,22	–	NC	–	No Connect

Detailed Description

In a VMEbus system a slave, such as a memory or an I/O device, responds to a master initiating a data transfer cycle. The slave monitors the address and address modifier bits and the address and data strobes. The VME 2000 responds to these signals when the slave is selected and acknowledges the data transfer back to the master to complete the handshake. The addresses and AM codes (except for AM2 and LWORD*) are externally coded.

Figure 2. contains a block diagram of a typical slave module configuration. Figure 3. shows critical timing relationships.

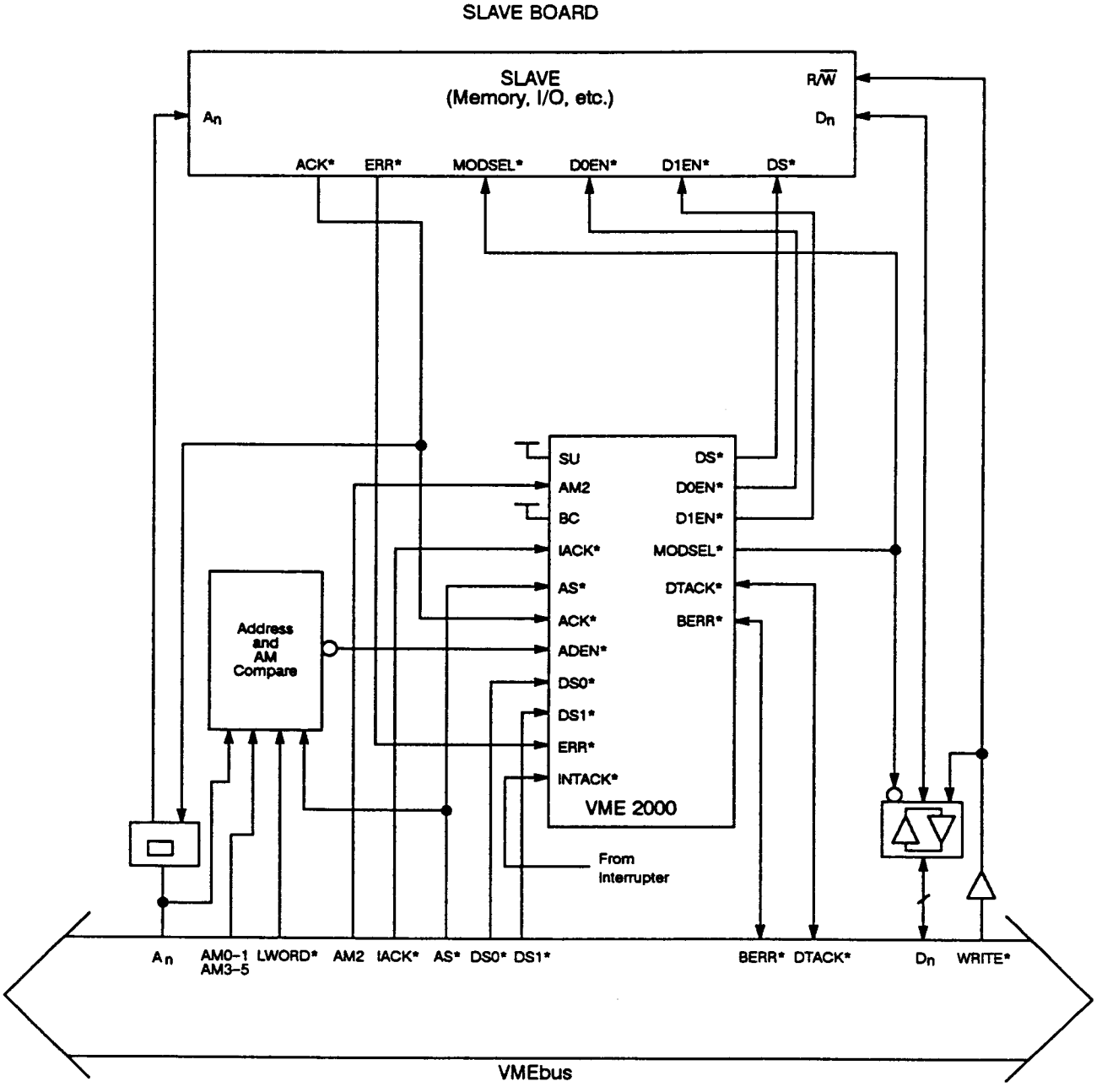


Figure 2. Slave Module Selector, Typical Implementation

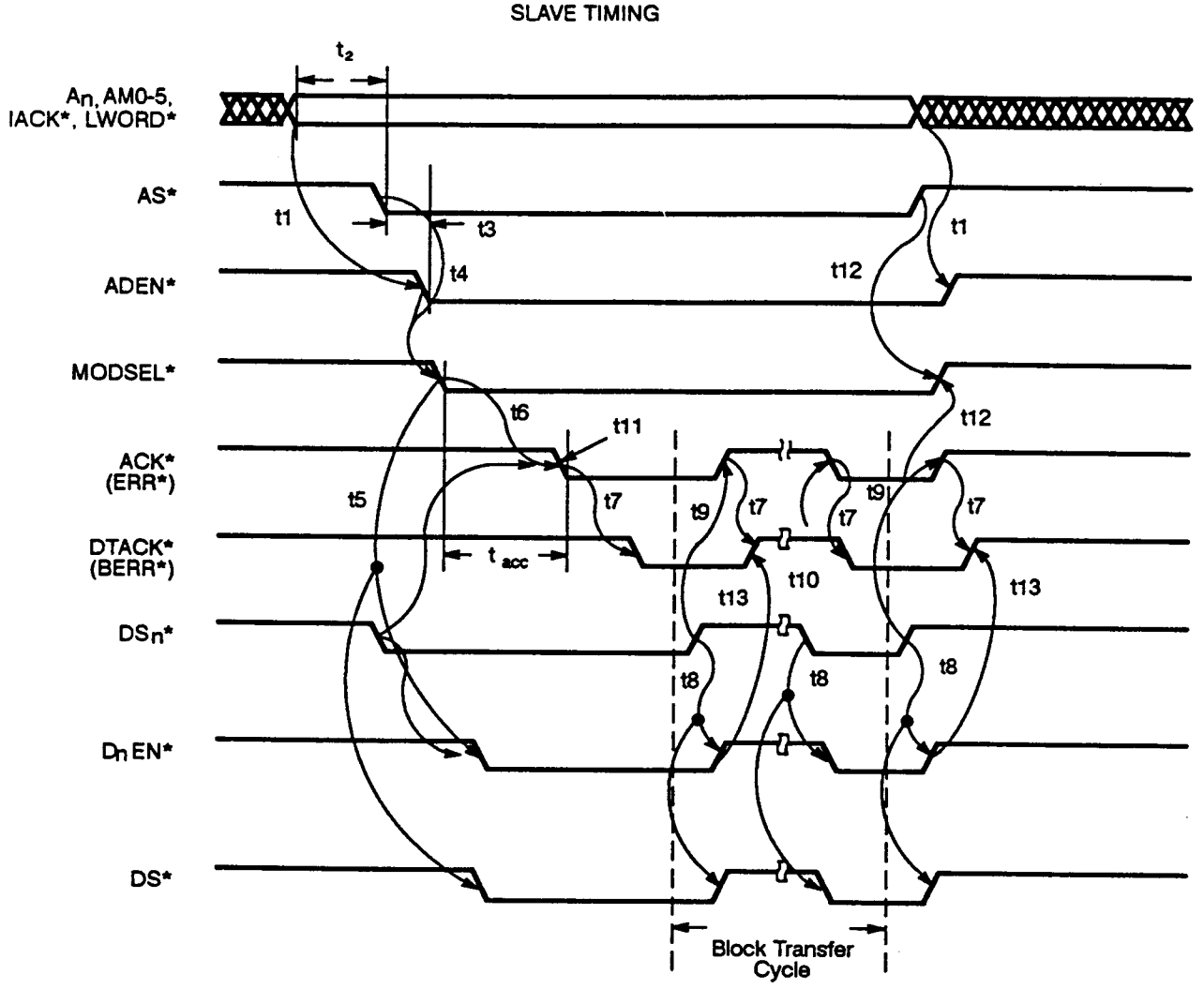


Figure 3. VMEbus Slave Module Timing Diagram

Address Decode

An external decoder monitors the addresses, Address Modifiers 0, 1, 3, 4, 5 and LWORD* to determine if the slave module is to be selected for a data transfer cycle. If this slave module is to be selected, ADEN* (the decoded value of the addresses, Address Modifiers and LWORD*) is enabled. To commence a data transfer cycle IACK* must be high (deasserted).

While the external decoder decodes the addresses, the VME 2000 monitors AM2 and SU to determine what cycle type is desired. The SU input in conjunction with AM2 selects the cycle type according to the table below:

ADEN*	AS*	MODSEL*	SU	AM2	Mode
0	0	0	0	0	Non-privileged
0	0	0	0	1	Supervisor
0	0	1	1	0	Invalid
0	0	0	1	1	Supervisor

Note: If SU is low, both supervisor and non-supervisor accesses will be accepted. If BC is high then the VME 2000 will assert BERR* for the invalid condition.

If SU is high and BC is low, no local error is asserted and no access is allowed (Modsel* not asserted). This condition will eventually cause a Bus timeout.

Slave Module Selection

If ADEN* is enabled and the VME 2000 detects an AM2 code match, then the VME 2000 will drive MODSEL* low to indicate that the slave is selected. To drive MODSEL* low, the VME 2000 must also detect address strobe (AS*) low to ensure that the address and address modifiers are valid. DTACK* and BERR* must also be high to signify the end of the previous data cycle.

DESIGN NOTE: VMEbus timing specifications require a minimum address to AS* set-up time of 10 nanoseconds. To ensure meeting this set up time, AS* should be connected to the address decoder as shown in Figure 2. If the address decode time is less than 10 ns then the address decode does not need to be qualified with AS*.

If the slave is selected (ADEN* goes low), MODSEL* is enabled from the edge of AS*. MODSEL* enables the VMEbus data transceivers and provides a global select signal to the slave device. D0EN* and D1EN* are strobed with DS0* and DS1* when MODSEL* is enabled and DTACK* and BERR* are high. An additional signal, DS*, is provided to enable the local slave's DTACK* generator (if required), following the assertion of either DS0* or DS1*. Additionally DS* may be used to increment an address counter on slaves which support block transfers.

Slave module selection will also occur from the assertion of INTACK*, when IACK* and AS* are low but ADEN* is not asserted.

Data Acknowledge

The falling edge of ACK* (ERR*) from the local slave indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. ACK*, in turn, drives DTACK* (BERR*).

The master releases the address and data strobes after it receives DTACK* low from the VME 2000. The release at the strobes also disables the VME 2000, ending the current cycle.

If there is an error, the VME 2000 gives precedence to BERR* over DTACK* if ACK* is also asserted, since overlapped DTACK* and BERR* signals are disallowed. For logic simplification, the user may overlap ACK* and ERR* but if ERR* is asserted it must be asserted before ACK*.

Block Moves

During a block move data transfer cycle, AS* is kept low and DS0*, DS1* and DTACK* are strobed with each individual data transfer. The slave provides its own address counter. The initial address is latched at the edge of MODSEL* and can be incremented by the rising edge of DS*. DS* is strobed from D0EN* and D1EN* during each data transfer within the block. The VME 2000 ensures that MODSEL* can not be deasserted until the end of the block transfer.

Address Pipelining

The VME protocol provides for address pipelining, or strobing of address and data separately to improve data transfer rates. The master can broadcast the address of the next cycle while the data transfer of the current cycle is occurring. AS* may be released as soon as DTACK* goes low.

The VME 2000 supports address pipelining by allowing the local slave to finish the current data cycle even though the AS* has been released. In address pipelining mode, DS* should be used to enable the data buffers instead of MODSEL*.

During address pipelining, MODSEL* will remain asserted until both data strobes, DS0* and DS1*, are released.

VME 2000 Timing Specifications

Timing Parameter	Signals	Max. Time (ns) unless otherwise specified		Description
		C-45	I-55, M-65	
t1	Address to ADEN* enable	@ decoder	@ decoder	External Address decode time
t2	Address to AS* enable	min. = 10	min. = 10	
t3	AS* to ADEN* enable	min. = 0	min. = 0	AS* input to address comparator ensures address to AS* set up time of 10ns minimum. This is valid if decode qualified with AS*
t4	AS* or ADEN* enable to MODSEL* enable	45	55, 65	MODSEL* enabled from whichever signal, AS* or ADEN*, is valid later. If the address decode is qualified with AS*, then ADEN* is valid later. If the address decode is not qualified with AS* then AS* is valid later.
t5	MODSEL* to D_nEN*	45	55, 65	MODSEL* must be enabled before the data strobes are enabled to local slaves
t5	MODSEL* to D_nEN* and DS*	45	55, 65	
t6	MODSEL* to ACK*	min. = memory access time	min. = memory access time	Local slave must receive MODSEL* low at start of cycle before it enables ACK* after memory ac cess. Min. delay = memory access time
t7	ACK* to DTACK*	45	55, 65	ACK* disables DTACK* if ACK* is disabled before D_nEN*
t8	DS_n* to D_nEN* and DS*	45	55, 65	
t9	DS_n* to ACK* release	@ local slave	@ local slave	Local Slave's time to release ACK*
t10	DS_n* to ACK* enable	min. = memory access time	min. = memory access time	Local Slave's time to enable ACK*, minimum time should be greater than memory access time (Block transfer cycles)
t11	ERR* enable to ACK* enable	min. = 0	min. = 0	Only if ACK* and ERR* overlap
t12	AS* or DS0* and DS1* disable to MODSEL* disable	45	55, 65	MODSEL* is disabled from whichever signal, AS* or DS0* and DS1*, is deasserted last. During address pipelining, DS0* and DS1* disable MODSEL*.
t13	D_n EN* disable to DTACK* disable	45	55, 65	D_nEN* disables DTACK* if D_nEN* is disabled before ACK*

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with
Power Applied ..... -55°C to +125°C
Supply Voltage to Ground
(pin 24 to pins 12, 18, & 20 on DIP) .. -0.5V to +7.0V
DC Voltage to Outputs in
High Z State ..... -0.5V to +7.0V

Operating Ranges

	Ambient Temperature	Supply Voltage (V_{CC})
Commercial	0°C to +70°C	5V + 5%
Industrial (I)	-40°C to +85°C	5V + 10%
Military (M)	-55°C to +125°C	5V + 10%

Electrical Characteristics Tested over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	Output pins I_{OL} = 24 mA (Com'l)		0.5	V
			I_{OL} = 24 mA (MIL)		0.6	V
			Pin 13, 15 I_{OL} = 48mA (Com'l)		0.5	V
			I_{OL} = 48mA (MIL)		0.6	V
V_{IH}	Input HIGH Level			2.0		V
V_{IL}	Input LOW Level				0.8	V
I_{IX}	Input Leakage Current	V_{SS} <= V_{IN} <= V_{CC}, V_{CC} = Max		-10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{SS} <= V_{OUT} <= V_{CC}		-40	40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.5V		-30	-90	mA
I_{CC}	Power Supply Current	V_{CC} = Max, V_{IN} = GND Outputs Open (Com'l)			80	mA
		V_{CC} = Max, V_{IN} = GND Outputs Open (MIL)			90	mA

Capacitance (sample tested only)

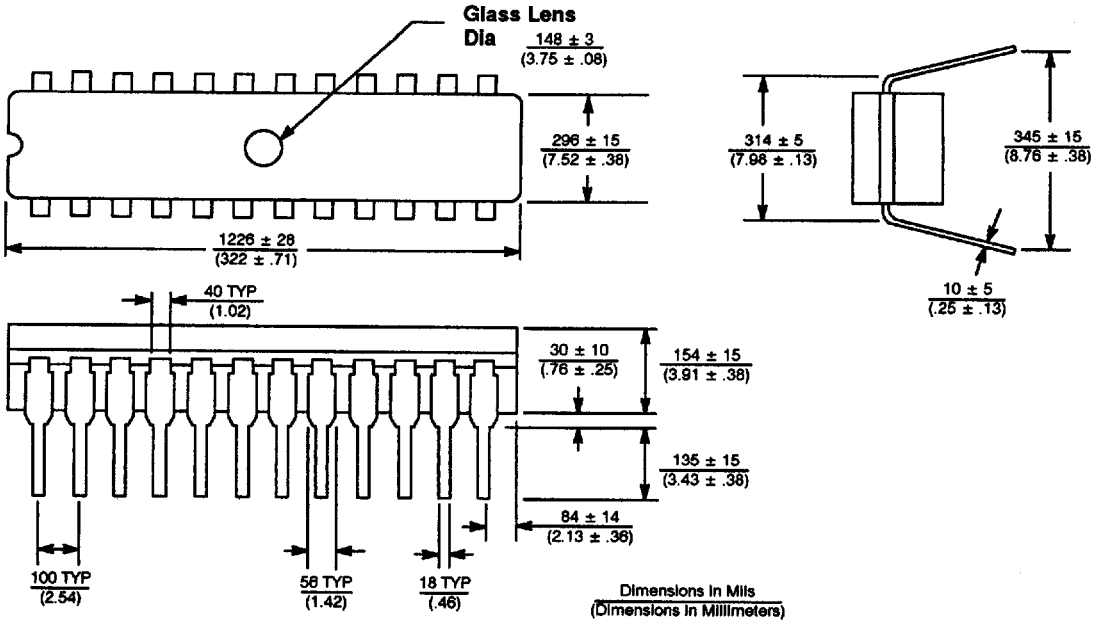
Parameter	Test Conditions	Pins	Typ	Units
C_{IN}	V_{IN} = 2.0V @ f = 1MHz	2-11, 14 (DIP)	5	pF
		13, 15-17, 19, 21-23 (DIP)	10	pF
C_{OUT}	V_{IN} = 2.0V @ f = 1MHz	13, 15-17, 19, 21-23 (DIP)	10	pF

Package Information

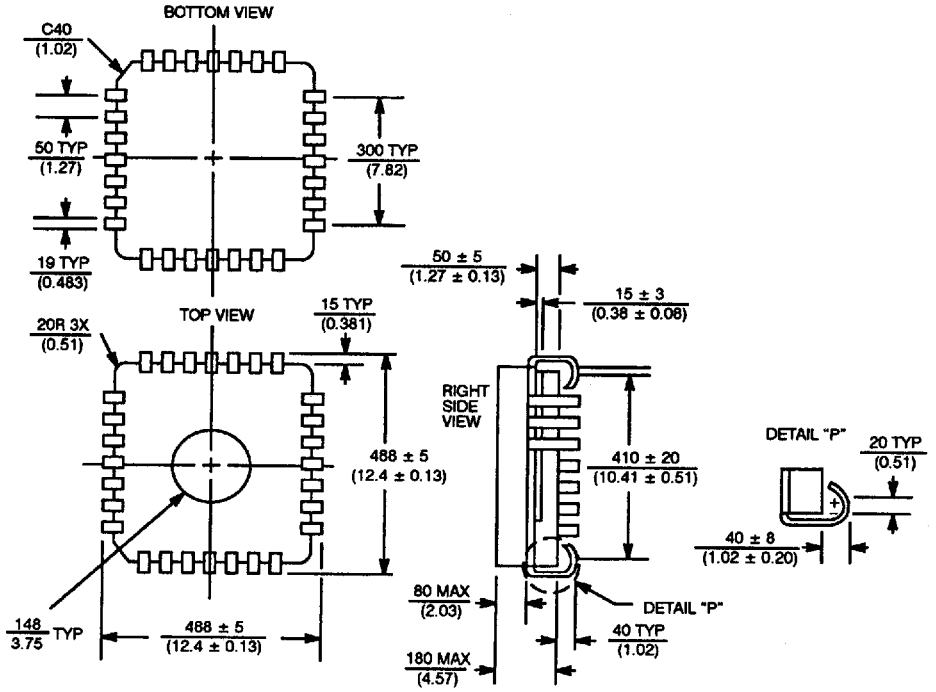
The devices are available in 24 pin slimline DIP (300 mil wide) or 28 pin LCC.

See PLX 448 or PLX 464 January 1989 or later data sheets for package dimensions. Contact PLX for further packaging information.

24-Lead Ceramic Dual In-line Package (CERDIP)

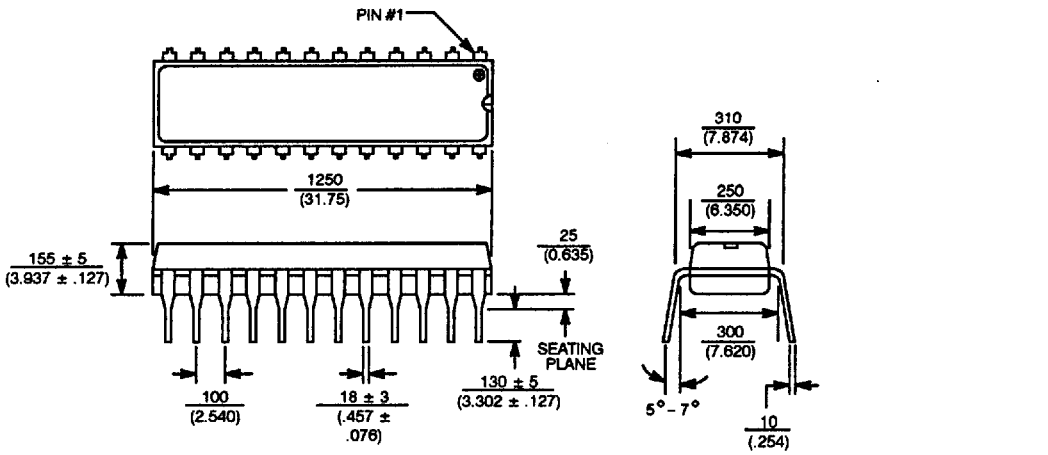


28-Pin J Lead Ceramic Chip Carrier



PLX 464 T-46-19-09

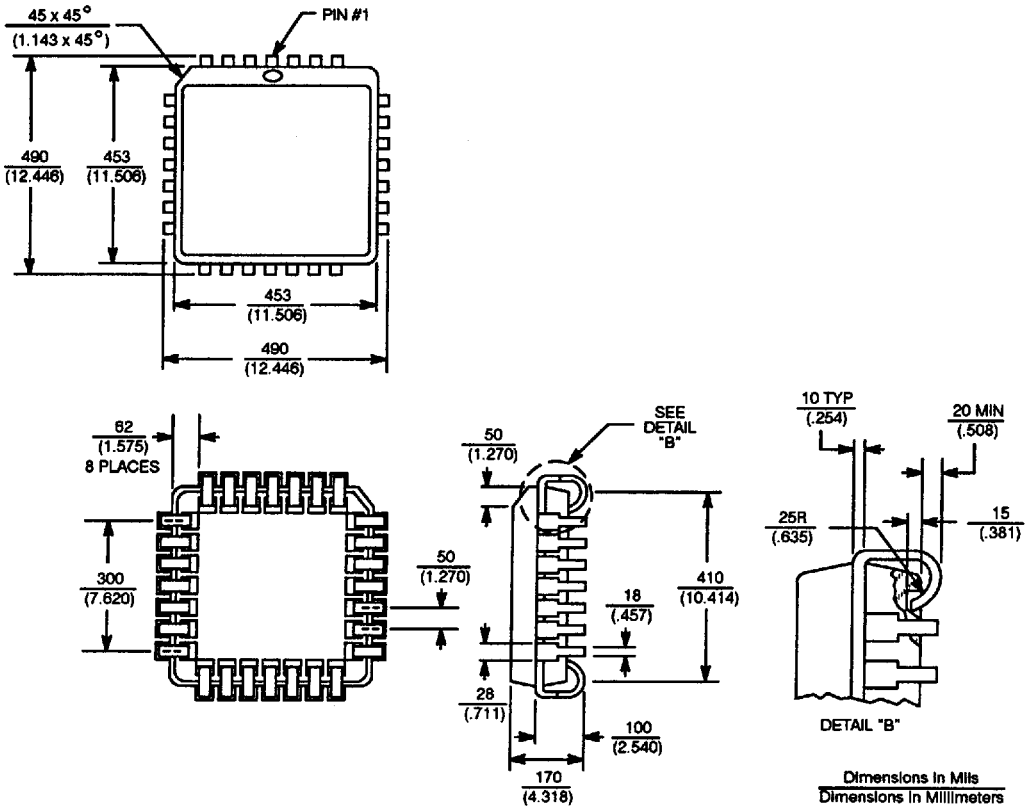
24-Pin DIP Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 (± 0.254) unless otherwise specified

28-Pin LCC Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 (± 0.254) unless otherwise specified