VTC Inc.
Value the Customer™

VM5711
FREQUENCY SYNTHESIZER/ PHASE LOCKED LOOP

July, 1993

FEATURES

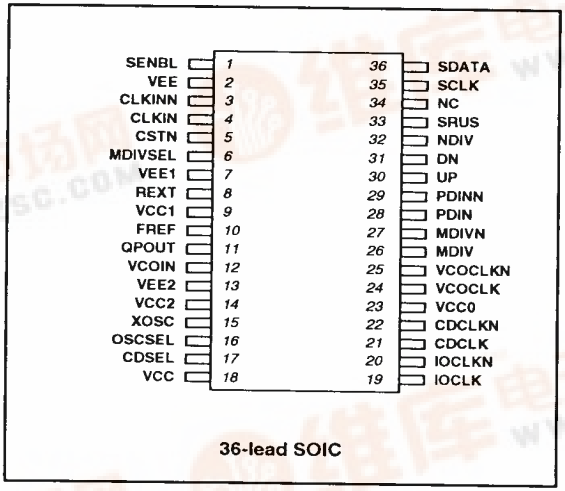
- Compatible with Zoned-Density Recording Applications
- Suitable for Many Applications in Data Communications, Graphics, etc.
- Differential ECL Output Frequency from 40 to 200 MHz
- Supports (1,7) Channel Data Rates up to 64 Mbits/sec
- Compatible with VTC's VM5603, VM5355, and VM5351/VM5352
- User Determined PLL Loop Filter Network
- Low Power Mode
- Power Dissipation less than 500 mW typical
- Power Supplies: +5 V Only

DESCRIPTION

The VM5711 is an integrated circuit designed to be used in high-performance zoned-density recording schemes. Its primary circuit function is to generate a variable frequency reference clock which is used as the fundamental system clock by the data recording channel. A serial microprocessor interface provides convenient access to internal registers which control the internal dividers and DAC. It can be used in zoned density schemes with recording frequency ratios of up to 1:2.5.

Please consult VTC for package availability.

CONNECTION DIAGRAM



36-lead SOIC

ABSOLUTE MAXIMUM RATINGS

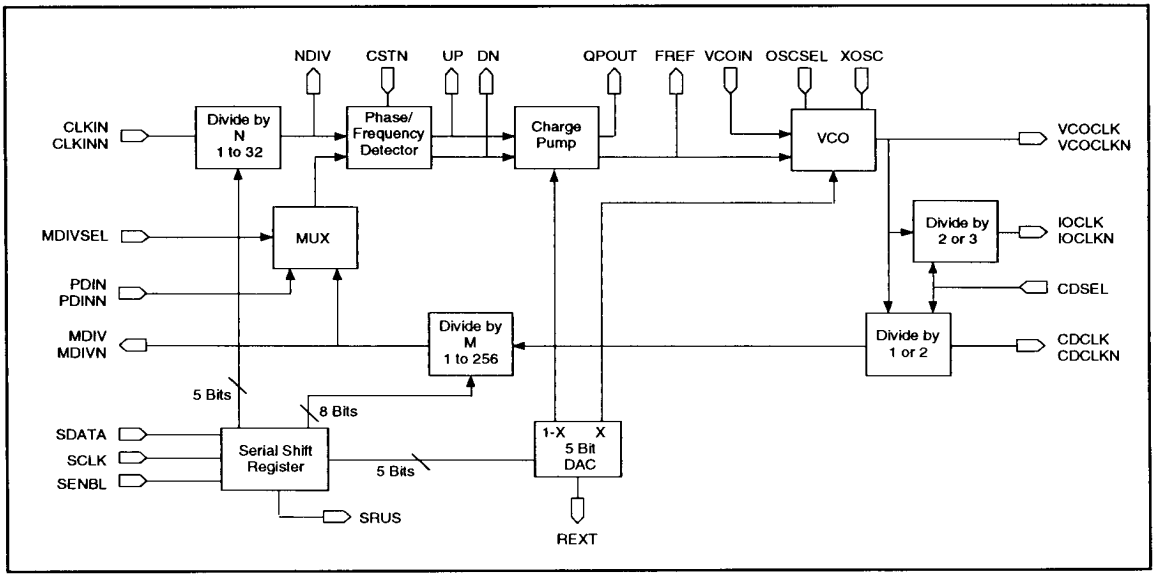
Supply Voltage, V_{CC} (V_{EE} = 0V)	-0.5V to +7.0V
Voltage Applied to TTL Inputs	
V_{EE} = 0V	-0.5V to VCC +0.5V
ECL Output Current - Continuous	25mA
- Surge	50mA
Maximum Power Dissipation	650mW
Storage Temperature	-65° to +150°C
Ambient Operating Temperature	0° to +70°C
Junction Temperature	0° to +150°C
Thermal Impedance Θ_{JA},	
36-lead SOIC	50°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages, VCC, VCC0, 1, 2	+4.5V to +5.5V
Junction Operating Temperature	0° to 130°C
Operating Temperature	0° to +70°C
ECL Reference Input Frequency	
CLKIN, CLKINN	4 to 50MHz
Synthesizer Output Frequency	40 to 200MHz
R_{EXT} Resistance (DAC current set)	1.25 to 5.0kΩ

DATA RECOVERY CIRCUITS

BLOCK DIAGRAM



FREQUENCY SYNTHESIZER

The frequency synthesizer is implemented using a charge pump type Phase-Lock Loop (PLL) with programmable reference clock and VCO feedback frequency dividers. The frequency synthesizer consists of a VCO, charge pump, phase/frequency detector, and two programmable frequency dividers. Refer to the block diagram.

The synthesizer reference clock signal that is used to drive the block comes into the chip through the CLKIN, CLKINN input pins. The Divide-by-N counter divides the incoming reference clock by a programmable integer value from 1 to 32. The output of the Divide-by-N becomes the reference clock for the synthesizer PLL. The Divide-by-M counter divides the CDCLK output by a programmable integer value from 1 to 256. The output of the Divide-by-M becomes the variable input to the synthesizer PLL. Both counters are programmed from the serial registers.

The phase/frequency detector block is a true frequency discriminating comparator with 2π radians per cycle usable for phase/frequency correction. An input pulse at the reference input initiates a pump-up signal to the Charge Pump and an input pulse at the variable input initiates a pump-down signal. When both pump-up and pump-down are true the circuit is reset. The minimum pump-up and pump-down pulse widths are determined by internal propagation delays and are about 5ns. In the locked condition, the pump-up and the pump-down signals are true for a short and equal period and are coincident in time. The pump-up and pump-down signals may be observed at the UP and DN test pins.

The charge pump sources and sinks correction current at the QPOUT pin when the pump-up and pump-down signals are true, respectively. An external RC network, connected between pin VCOIN and pin FREF, is used to set the PLL dynamic characteristics. The FREF pin connects to a low impedance loop filter reference node to minimize noise coupling into the VCO input. The voltage at this pin is about 2.5V. The charge pump current driven into the loop filter generates a differential voltage at pin VCOIN with respect to pin FREF. This voltage drives the VCO block inputs. The charge pump gain (the output current magnitude divided by 2π) is set by the current output from the internal DAC determined by R_{EXT} and the DAC setting.

The VCO block converts the differential voltage between pins VCOIN and FREF into a frequency. This frequency is output at the two differential (uncompensated) ECL pins VCOCLK and VCOCLKN and is also fed back to the Phase/Frequency Comparator through the Divide-by-M counter. Center frequency occurs when the voltage between the filter pins is zero. Center frequency is set by the R_{EXT} and the DAC setting. Adjusting the VCO center frequency with the DAC "X" output current changes the VCO gain constant in a proportional manner. A second current, the DAC "1-X" current, IQP is used to offset this change by adjusting the Charge Pump gain proportional to "1-X", thus maintaining a reasonably constant loop gain.

Table 1: Output clock frequencies (where m is the VCO divisor and n is the CLKIN divisor)

CLKIN	CDSEL	VCOCLK	IOCLK	CDCLK
f_i	0 (2,7)	$f_O = f_i$ (m/n)	$f_O/2$	f_O
f_i	1 (1,7)	$f_O = 2f_i$ (m/n)	$f_O/3$	$f_O/2$

REFERENCE DAC

The reference DAC is a five-bit, current output digital to analog converter. The DAC are driven in parallel from Parallel Register A.

The I_{REXT} reference current is used internally to set the VCO center frequency and the Charge Pump gain as described in the section above. The VCO center frequency f_o (the DAC's "X" output current), and the charge pump gain current (the "1-X" current, I_{QP}), are given by the expressions below. R_{EXT} is the resistance value in ohms from the REXT pin to VEE and X is the decimal equivalent of the DAC input bits A_5 through A_9, with A_9 being the most significant bit, f_o (MHz) is the VCO center frequency and K_{VCO} (MHz/V) is the VCO gain.

$$I_{QP}\ (\mu A) = 0.878 \bullet 10^6 \bullet (5/3 - X/32) / (R_{EXT}\ [ohms])$$

$$f_o\ (MHz) = 0.23 \bullet 10^6 \bullet\ (2/3 + X/32) / (R_{EXT}\ [ohms])$$

$$K_{VCO}\ (MHz/V) = 0.38 \bullet f_o\ (MHz)$$

SERIAL REGISTERS

Data to program the DAC and programmable counters of the Frequency Synthesizer are loaded into the circuit through an 11-bit serial input register which consists of 11 D-type flip-flops. Data at the SDATA input is loaded into the serial register on the rising edge of the serial clock at pin SCLK when the serial register enable pin SENBL is LO. Data bit S_{10} is the most significant bit and is shifted in first. When pin SENBL is HI, inputs at pin SDATA and pin SCLK are ignored. All three serial interface signals, SDATA, SCLK, and SENBL, are TTL level signals.

Parallel Register A and Parallel Register B are 10-bit and 8-bit transparent latch type registers, respectively. Data is transferred from the Serial Register to one of the Parallel Registers on the rising edge of the serial enable signal at pin SENBL. Parallel Register A is loaded if bit S_{10} is LO and Parallel Register B is loaded if S_{10} is HI. The data in the unselected parallel register is unchanged by the load operation. Parallel Register B bits B_{00} through B_{07} are used to program the Divide-by-M. Parallel Register A bits A_{00} through A_{04} program the Divide-by-N counter and bits A_{05} through A_{09} program the 5-bit DAC. Data is transferred from the Serial Register, through the Parallel Registers, to the Divide-by or DAC circuits according to the Bit Assignment Table below.

Register Bit Assignment Table

Input Order	Serial Bit	S_{10} = LO Parallel A Bit	S_{10} = HI Parallel B Bit
1	S_{12}	A_{12} --> Fault 1	
2	S_{11}	A_{11} -->Fault 0	
3	S_{10}	S_{10} = LO	S_{10} = HI
4	S_{09}	A_{09} --> DAC_4	x
5	S_{08}	A_{08} --> DAC_3	x
6	S_{07}	A_{07} --> DAC_2	B_{07} --> M_7
7	S_{06}	A_{06} --> DAC_1	B_{06} --> M_6
8	S_{05}	A_{05} --> DAC_0	B_{05} --> M_5
9	S_{04}	A_{04} --> N_4	B_{04} --> M_4
10	S_{03}	A_{03} --> N_3	B_{03} --> M_3
11	S_{02}	A_{02} --> N_2	B_{02} --> M_2
12	S_{01}	A_{01} --> N_1	B_{01} --> M_1
13	S_{00}	A_{00} --> N_0	B_{00} --> M_0

The value of the DAC bits, (DAC_4 - DAC_0), are the same as register bits A_{09} - A_{05}. So, if a DAC value of sixteen is desired (A_{09} - A_{05}) = 10000. The N and M values are different, however. Since divide-by-zero is not possible, the divide-by-N or M is the decimal value of register bits (A_{04} - A_{00}) or (B_{07} - B_{00}) plus 1. For example, if N = 4 and M = 6 are the desired divide values, then (A_{04} - A_{00}) = 00011 and (B_{07} - B_{00}) = 00000101. This gives N = 3 + 1 = 4 and M = 5 + 1 = 6.

PIN DESCRIPTIONS

DIGITAL INPUT PINS:

SCLK: Serial register clock input, data is loaded from pin SDATA on each rising edge of SCLK while SENBL is LO, standard TTL levels.

SDATA: Serial register data input, data on this pin is loaded into the serial register on each rising edge of SCLK while SENBL is LO, standard TTL levels.

SENBL: Serial register enable, standard TTL levels. A LO input enables the loading of the serial register using pins SCLK and SDATA. Data is transferred from the serial register to one of the parallel register on the rising edge of SENBL. Inputs at SCLK and SDATA are ignored while SENBL is HI.

CLKIN, CLKINN: Reference frequency input. The differential ECL clock at these pins will be the reference frequency of the frequency synthesizer.

PDIN, PDINN: Phase/Frequency detector input. These differential ECL inputs will normally originate from the MDIV, MDIVN outputs. PDIN, PDINN inputs are selected when MDIVSEL is LO. If unused tie to MDIV/MDIVN or bias HI/LO within VIN range (VCC - 2.3V) to avoid oscillation.

MDIVSEL: A TTL input used to select the feedback input to the phase/frequency detector. MDIVSEL LO selects PDIN, PDINN inputs, allowing external or additional divide-by-M-counters to be added externally. MDIVSEL HI selects the divide-by-M counter output internally.

CDSEL: A TTL input used to select the code option. CDSEL LO = (2,7) code: HI = (1,7) code (code formats for disk drive data channels).

OSCSEL: A TTL input used to enable a VCO test feature. A LO level allows an external VCO frequency to be input into the divider blocks through the XOSC pin. A HI level allows normal operation.

XOSC: A TTL test VCO input pin. This input replaces the on chip VCO when the OSCSEL input is LO.

CSTN: A TTL input used to enable/disable the phase/frequency detector. A HI level enables the phase/frequency detector. A LO level shuts off the phase frequency detector and allows the VCO to coast.

DIGITAL OUTPUT PINS:

VCOCLK, VCOCLKN: Frequency synthesizer VCO output pins, used as the 3f clock for 1,7 code or 2f clock for 2,7 code by the disk drive read/write channel. These pins are open emitter differential outputs, each requiring an external 511Ω pull-down resistor to VEE. The output levels are uncompensated ECL and should be used with a differential ECL receiver.

IOCLK, IOCLKN: VCO frequency divided output pins, used as the 1f reference clock by the disk drive read/write channel. These pins are open emitter differential outputs, each requiring an external 511Ω pull-down resistor to VEE. The output levels are uncompensated ECL and should be used with a differential ECL receiver.

CDCLK, CDCLKN: VCO frequency divided output pins, used as the code rate (1.5f for 1,7 code or 2f for 2,7 code) reference clock by the disk drive read/write channel. These pins are open emitter differential outputs, each requiring an external 511Ω pull-down resistor to VEE. The output levels are uncompensated ECL and should be used with a differential ECL receiver.

MDIV, MDIVM: CDCLK frequency divided by M. These pins are open emitter differential outputs, each requiring an external 511Ω pull-down resistor to VEE. This test output should be unconnected when not in use.

NDIV: Input frequency (CLKIN, CLKINN) divided by M. This pin is an open emitter ECL output, requiring an external 511Ω pull-down resistor to VEE. This test output should be unconnected when not is use.

UP: Active HI whenever the phase/frequency detector issues a pump-up to the charge pump. This pin is an open emitter ECL output requiring an external 511Ω pull-down resistor to VEE. This test output should be unconnected when not in use.

DN: Active HI whenever the phase/frequency detector issues a pump-down to the charge pump. This pin is an open emitter ECL output requiring an external 511Ω pull-down resistor to VEE. This test output should be unconnected when not in use.

SRUS: The shift register unsafe fault pin, TTL levels. This pin will go low if a fault in the programmable M and N counter latches occurs due to an inadvertent static discharge to the drive. This pin normally sits high.

ANALOG PINS:

FREF, VCOIN: Differential loop filter pins for the frequency synthesizer's phase locked loop. The filter RC network is connected between these pins as shown in the Typical Connection Diagram. Pin FREF is a low impedance reference node with a voltage of 2.5 volts at nominal supply voltage. The VCO center frequency occurs when the voltage between pin FREF and VCOIN is zero. The dynamic range on pin VCOIN relative to pin FREF is ±0.75 volts. The VCO frequency can be controlled directly by forcing the voltage on VCOIN.

QPOUT: Charge pump output pin, outputs current into the loop filter. The current is controlled by REXT and the DAC setting. Under normal operation, QPOUT is shorted to VCOIN.

REXT: I_{REXT} reference current, the resistor R_{EXT} connected between pin REXT and VEE1 sets the current reference for the internal DAC that drives the frequency synthesizer's VCO and Charge Pump circuits. The voltage at pin REXT is approximately 1.17V.

SUPPLY PINS:

VCC: Digital power, +5.0 volts

VCC0: ECL emitter follower collector power, +5.0 volts

VCC1: Analog power, +5.0 volts

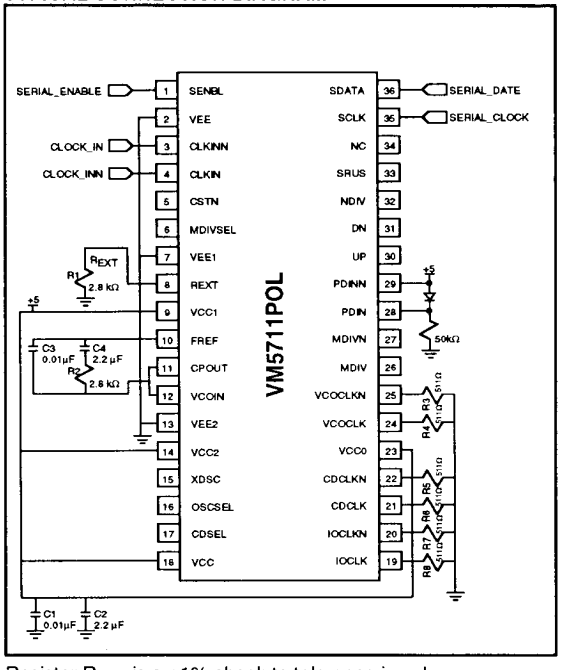
VCC2: VCO power, +5.0 volts

VEE: Digital ground

VEE1: Analog ground

VEE2: VCO ground

TYPICAL CONNECTION DIAGRAM



Resistor R_{EXT} is a ±1% absolute tolerance in value.

DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ, $V_{CC} = V_{CC0} = V_{CC1} = V_{CC2}$. Refer to typical connection diagram.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Currents:						
Total Current		All ECL outputs open			130	mA
Digital Supply	I_{CC}	All ECL outputs open		77		mA
Analog Supplies	I_{CC1},I_{CC2}			15		mA
TTL Inputs: (note 2)						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V, V_{CC} = 5.5V			20	µA
		V_{IH} = 7.0V, V_{CC} = 5.5V (Note 1)			100	
Input Low Current	I_{IL}	V_{IL} = 0.4V, V_{CC} = 5.5V			-0.6	mA
Input Clamp Volts	I_{IK}	I_{IN} = -18mA, V_{CC} = 4.5V			-1.5	V
Differential ECL Inputs:						
Common Mode Input Voltage	V_{CIM}		V_{CC} -2.3		V_{CC} -0.3	V
Differential Input Voltage	V_{INDIF}		200			mV
Input Current High	INH	V_{IH} maximum			25	µA
Input Current Low	INL	V_{IL} minimum			25	µA
Analog Pins:						
DAC Bias	V_{REXT}	R_{EXT} = 2.8kΩ		1.17		V
Filter Bias	V_{FREF}	V_{CC} = 4.5V		2.45		V
		V_{CC} = 5.0V		2.50		
		V_{CC} = 5.5V		2.55		
VCO Input Range	V_{VCOIN}		1.75		3.25	V
Charge Pump Output Range	V_{QPOUT}		1.75		3.25	V
Charge Pump Current	I_{QP}	R_{EXT} = 2.8kΩ, DAC Setting = 10000	328	365	402	µA
Differential ECL Outputs: (note 3)						
Output high voltage	V_{OH}	T_{amb} = 0°C MECL 10KH Compatible	V_{CC} -1.02		V_{CC} -0.78	V
			V_{CC} -1.00		V_{CC} -0.84	
		T_{amb} = 25°C MECL 10KH Compatible	V_{CC} -0.98		V_{CC} -0.75	
			V_{CC} -0.96		V_{CC} -0.81	
		T_{amb} = 70°C MECL 10KH Compatible	V_{CC} -0.92		V_{CC} -0.66	
			V_{CC} -0.90		V_{CC} -0.74	
Output low voltage	V_{OL}	T_{amb} = 0°C MECL 10KH Compatible	V_{CC} -1.95		V_{CC} -1.63	V
			V_{CC} -1.95		V_{CC} -1.65	
		T_{amb} = 25°C MECL 10KH Compatible	V_{CC} -1.95		V_{CC} -1.63	
			V_{CC} -1.95		V_{CC} -1.65	
		T_{amb} = 70°C MECL 10KH Compatible	V_{CC} -1.95		V_{CC} -1.60	
			V_{CC} -1.95		V_{CC} -1.65	

Note 1: All TTL inputs except PWRDN pin. PWRDN pin has ESD protection diodes to both rails where as standard TTL inputs have protection to V_{EE} rail only.
Note 2: TTL inputs will float to a logic HI if left unconnected.
Note 3: All outputs denoted as ECL are +5 Volt referenced track with the V_{CC} supply voltage. The following DC specifications assume V_{CC} is +5.0V. Limits are specified after thermal equilibrium has been established.

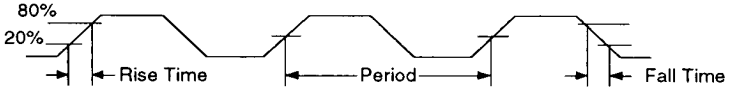
AC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; C_3 = 0.01µF, C_4 = 2.2µF, R_1 = 2.8kΩ, R_2 = 2.8kΩ, V_{CC} = V_{CC0} = V_{CC1} = V_{CC2} = 5.0V, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCO Center Frequency	f_o	R_{EXT} = 2.8kΩ, VCOIN and FREF pins connected together, DAC setting = 10000	86.4	96	105.6	MHz
VCO Dynamic Tuning Range			±28			%
VCO Gain	K_{VCO}	R_{EXT} = 2.8kΩ, DAC setting = 10000 (Note 4)	34.2	38	41.8	MHz/V
Output Rise Time	t_r	f_o = 100MHz	0.7		3.8	ns
Output Fall Time	t_f	f_o = 100MHz	0.7		4.4	ns
VCO Frequency Jitter	σ_{fVCO}	(Note 4 & 5), f_o = 100MHz		75		ps rms
Serial Registers:						
SCLK Clock Rate					10	MHz
SDATA Setup Time			40			ns
SDATA Hold Time			5			ns
SENBL Setup Time			40			ns
SENBL Hold Time			40			ns
SENBL Pulse Time			200			ns

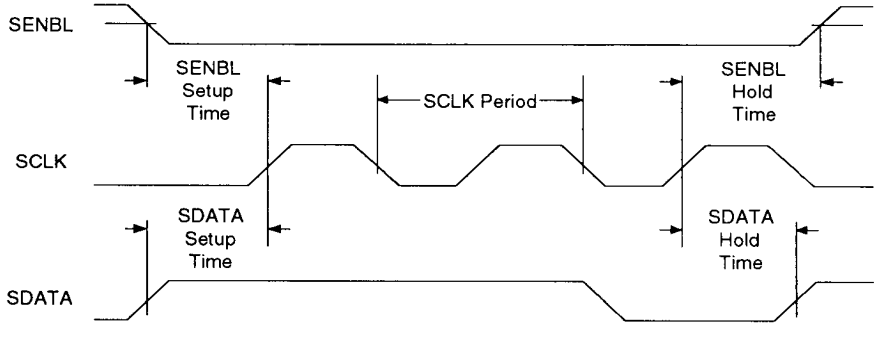
Note 4: Force VCOIN and measure frequency differentially between pins VCOCLK and VCOCLKN with the DAC register = 10,000. Calculate gain using KVCO = (f_1 - f_0) / [VCOIN (f_1) - VCOIN (f_0)].

Note 5: VCOCLK output 1σ point measured over 10,000 samples on an HP5370B Time Interval counter. $\sigma_{tcl} = \sqrt{\sigma_a^2 - \sigma_b^2}$, where σ_a = rms jitter measurement and σ_b = self jitter of HP5370B (see HP app. note 191-4).

PHASE LOCK LOOP TIMING DIAGRAM



SERIAL REGISTER TIMING DIAGRAM



DATA RECOVERY CIRCUITS