VTC Inc.
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VM5701

FREQUENCY SYNTHESIZER FOR ZONED DENSITY RECORDING

Refer to Application Note APN-5 and APN-9

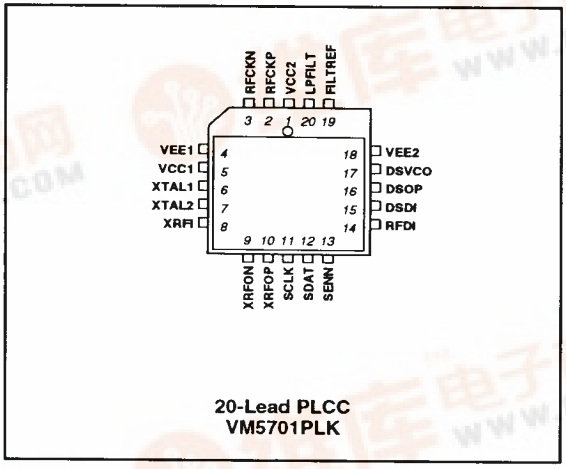
PRELIMINARY

July, 1992

FEATURES

- Designed for Zoned-Density Recording Operation with VTC's VM5601 and VM5355
- Compatible with Other Applications, Including Data Communications, Graphics, etc.
- Crystal Oscillator or External TTL Reference Frequency Input
- Differential ECL Output Frequency from 10 to 72 MHz
- User Determined PLL Loop Filter Network
- Power Dissipation Less Than 500 mW
- Operates on a Power Supply of +5V
- Available in a 20-Lead PLCC Package

CONNECTION DIAGRAM



20-Lead PLCC
VM5701PLK

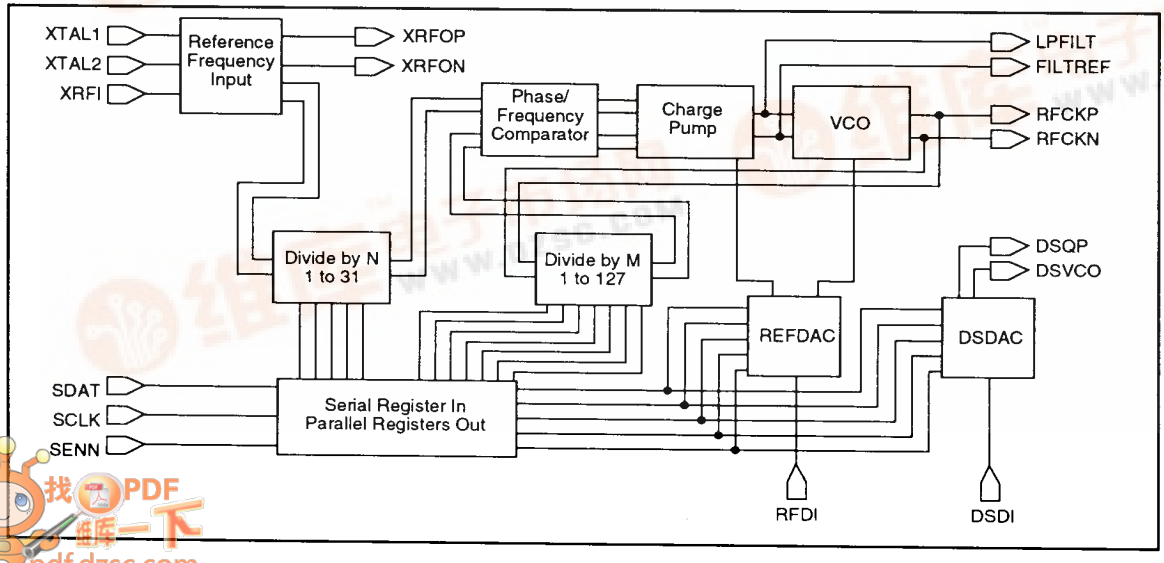
DESCRIPTION

The VM5701 is an integrated circuit designed to be used in high-performance zoned-density recording schemes with recording frequency ratios of up to 1:2.5. The VM5701 has three primary circuit functions:

1. A reference clock generator that is used to synthesize the write/reference frequency used by the data recording channel.
2. A current output DAC that is used to set the center frequency of the recording channel's data separator VCO (e.g. VTC's VM5355).
3. A crystal oscillator that can be used as the reference clock for the frequency synthesizer.

Parallel registers hold the data to program the synthesizer frequency, an internal DAC and the data separator DAC. The parallel registers are loaded through a 13-bit serial register and a series-to-parallel conversion.

BLOCK DIAGRAM



DATA RECOVERY CIRCUITS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage:
V_{CC}, (V_{EE} = 0V) ..... -0.5V to +7.0V
Ambient Operating Temperature ..... 0° to +70°C
Junction Operating Temperature ..... 0° to +130°C
Maximum Power Dissipation 980mW
Thermal Impedance, θ_{JA}
20-Lead PLCC ..... 59°C/W
Voltage Applied to TTL Inputs:
V_{EE} = 0V ..... -0.5V to V_{CC} +0.5V
ECL Output Current
Continuous 25mA
Surge 50mA
Storage Temperature ..... -65° to 150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage:
V_{CC1}, V_{CC2} ..... +4.5V to 5.5V
Operating Junction Temperature ..... 0° to 70°C
Crystal Oscillator Frequency ..... 4 to 50MHz
TTL Reference Input Frequency ..... 4 to 50MHz
Synthesizer Output Frequency ..... 15 to 72MHz
R_{DSDI} Resistance (DS DAC curent set) ..... 1.15 to 1.91kΩ
R_{RFDI} Resistance (Ref DAC current set) ..... 1.15 to 1.91kΩ

FREQUENCY SYNTHESIZER

The frequency synthesizer is implemented using a charge pump type Phase-Lock Loop (PLL) with programmable reference clock and VCO feedback frequency dividers. The frequency synthesizer consists of the VCO, the Charge Pump, and the Phase/Frequency Comparator, plus the two programmable dividers, Divide-by-M and Divide-by-N, as shown in the Block Diagram.

The Divide-by-N counter divides the incoming reference clock by a programmable integer value from 1 to 31. The output of the Divide-by-N becomes the reference clock for the synthesizer PLL. The Divide-by-M counter divides the synthesizer VCO output by a programmable integer value from 1 to 127. The output of the Divide-by-M becomes the variable input to the synthesizer PLL. Both counters are programmed from Parallel Register A which will be described in detail in the Series/Parallel Register section. The zero count is used to place each divider into a test mode. When integer value zero is programmed into Divide-by-N and/or Divide-by-M the respective output is held static. In this test mode the charge pump output currents can be measured on a static basis between the loop filter pins LPFILT and FILTREF.

The Phase/Frequency Comparator block is a true frequency discriminating comparator with 2π radians per cycle usable for phase/frequency correction. An input pulse at the reference input initiates a pump-up signal to the Charge Pump and an input pulse at the variable input initiates a pump-down signal. When both pump-up and pump-down are true the circuit is reset. The minimum pump-up and pump-down pulse widths are determined by internal propagation delays and are about 5nsec. In the locked condition, the pump-up and the pump-down signals are true for a short and equal period and are coincident in time.

The Charge Pump sources and sinks correction current at the LPFILT pin when the pump-up and pump-down signals are true, respectively. An external RC network, connected between pin LPFILT and pin FILTREF, is used to set the PLL dynamic characteristics. The FILTREF pin connects to a low impedance loop filter reference node to minimize noise coupling into the VCO input. The voltage at this pin is about 2.3 V. The Charge Pump current driven into the loop filter generates a differential voltage at pin LPFILT with respect to pin FILTREF. This voltage drives the VCO block inputs. Further, the Charge Pump gain (the output current magnitude divided by 2π) is set by the current output from the internal Reference DAC. The magnitude of the Charge Pump up and down currents are equal to 1/2 of the Reference DAC current I_{RFQP} and are of opposite polarity.

The VCO block converts the differential voltage between pins LPFILT and FILTREF into a frequency. This frequency is output at the two differential (uncompensated) ECL pins RFCKP and RFCKN and is also fed back to the Phase/Frequency Comparator through the Divide-by-M counter. Center frequency occurs when the voltage between the filter pins is zero. Center frequency is set by the I_{RFVCO} current from the internal Reference DAC and is equal to (37500 I_{RFVCO}) MHz. Adjusting the VCO center frequency with the DAC "X" output current changes the VCO gain constant in a proportional manner. A second current, the DAC "1-X" current, is used to offset this change by adjusting the Charge Pump gain proportional to "1-X", thus maintaining a reasonably constant loop gain.

In the locked condition the output frequency of the VCO is M/N times the input reference frequency, where M and N are the decimal equivalents of the Divide-by-M bits M_6 through M_0 and the Divide-by-N bits N_4 through N_0, respectfully.

REFERENCE AND DATA SEPARATOR DACs

The Reference and Data Separator DACs are each a five-bit, current output digital to analog converter. The two DACs are driven in parallel from Parallel Register B.

The Reference DAC is used internally to set the VCO center frequency and the Charge Pump gain as described in the section above. The magnitude of the VCO center frequency current (the DAC's "X" output current), I_{RFVCO} and the Charge Pump gain current (the "1-X" current), I_{RFQP} are given by the expressions below. The DAC gain constant has a slight current dependence due to the non-zero output impedance at pin RFDI. This impedance looks like a resistance in series with R_{RFDI} and is represented by the 93.2Ω term in the expressions below. In these equations, RRFDI is the resistance value in Ohms from the RFDI pin to VEE and X is the decimal equivalent of the DAC input bits B_0 through B_4, with B_4 being the most significant bit.

$$I_{RFVCO} = [1.21 \bullet (2/3 + X/31)] / (93.2 + R_{RFDI})$$

$$I_{RFQP} = [1.21 \bullet (5/3 - X/31)] / (93.2 + R_{RFDI})$$

Similarly, the Data Separator DAC is used to set the VCO center frequency and the Charge Pump gain on the recording channel's Data Separator circuit. The current outputs at pin DSVCO and pin DSQP sink the currents I_{DSVCO} and I_{DSQP}, respectively. These outputs are open collector NPN devices

and are designed to be compatible with VTC's VM5355 Data Separator circuit. The expressions for these DAC output currents are given below. In these equations, RDSDI is the resistance in Ohms from the DSDI pin to VEE and X is the decimal equivalent of the DAC input bits B_0 through B_4, with B_4 being the most significant. Also the non-zero output impedance at pin DSDI is represented by the 93.2Ω term in series with R_{DSDI}.

$$I_{DSVCO} = [1.21 \bullet (2/3 + X/31)] / (93.2 + R_{DSDI})$$

$$I_{DSQP} = [1.21 \bullet (5/3 - X/31)] / (93.2 + R_{DSDI})$$

REFERENCE FREQUENCY INPUT

The synthesizer reference clock signal that is used to drive the Divide-by-N block can be derived from one of two sources, a crystal oscillator or an externally generated TTL level reference clock. The TTL clock is applied to pin XRFI which is a Schmitt-trigger type input for improved false clock immunity.

The crystal oscillator circuit uses an external series mode crystal connected between pins XTAL1 and XTAL2 to generate a low phase noise reference clock XTALREF. The oscillator may be used with either fundamental mode or overtone mode crystals. In fundamental mode the oscillator will operate from 4 to 15 MHz with no additional external components required. For overtone type crystals the oscillator will operate from 15 to 50 MHz with an external RLC network required.

Selection of the desired frequency is source is accomplished by either grounding pin XRFI to select the crystal oscillator source or by connecting pin XTAL1 to VCC1 while leaving pin XTAL2 open to select the TTL reference clock. When the crystal oscillator is selected (pin XRFI grounded) the reference clock is also output at the differential (uncompensated) ECL pins XRFOP and XRFON. When the TTL frequency reference is selected the differential output is LO (XRFOP at ECL LO and XRFON at ECL HI). Further, a test mode to measure the TTL input hysterysis is provided by forcing pin XTAL1 to 2.0V leaving pin XTAL2 open. In this mode the complement of the signal TTLREF (denoted $\overline{\text{TTLREF}}$) will appear between pins XRFOP and XRFON. A truth table for the Reference Frequency block is given below.

Input At Pin XRFI	Internal Signal Input At Pin XTAL1	Reference CLOCK	Output Between XRFOP-XRFON
TTL LO	XTALREF	$\overline{\text{XTALREF}}$	$\overline{\text{XTALREF}}$
TTL HI	XTALREF	CML HI	ECL LO
TTLREF	VCC1	TTLREF	$\overline{\text{ECL LO}}$
TTLREF	2.0V	CML HI	$\overline{\text{TTLREF}}$

SERIAL AND PARALLEL REGISTERS

Data to program the two DACs and the programmable counters of the Frequency Synthesizer are loaded into the circuit through a 13-bit serial input register which consists of 13 D-type flip-flops. Data at the SDAT input is loaded into the serial register on the rising edge of the serial clock at pin SCLK when the serial register enable pin SENN is LO. Data bit S12 is the most significant bit and is shifted in first. When pin SENN is HI, inputs at pin SDAT and pin SCLK are ignored. All three serial interface signals, SDAT, SCLK, and SENN, are TTL level signals.

Parallel Register A and Parallel Register B are 12-bit and 5-bit transparent latch type registers, respectively. Data is transferred from the Serial Register to one of the Parallel Registers on the rising edge of the serial enable signal at pin SENN. Parallel Register A is loaded if bit S12 is LO and Parallel Register B is loaded if S12 is HI. The data in the unselected parallel register is unchanged by the load operation. Parallel Register A bits A00 through A11 are used to program the Divide-by-M and the Divide-by-N counters. Parallel Register B bits B00 through B04 program the Reference DAC and the Data Separator DAC in parallel (i.e. both DACs always have the same input count). Data is transferred from the Serial Register, through the Parallel Registers, to the Divide-by or DAC circuits according to the Bit Assignment Table below.

Register Bit Assignment Table

Input Order	Serial Bit	S_{12} = Lo Parallel A Bit	S_{12} = Hi Parallel B Bit
1	S_{12}		
2	S_{11}	A_{11} ----> N_4	
3	S_{10}	A_{10} ----> N_3	
4	S_{09}	A_{09} ----> N_2	
5	S_{08}	A_{08} ----> N_1	
6	S_{07}	A_{07} ----> N_0	
7	S_{06}	A_{06} ----> M_6	
8	S_{05}	A_{05} ----> M_5	
9	S_{04}	A_{04} ----> M_4	B_{04} ----> DAC4
10	S_{03}	A_{03} ----> M_3	B_{03} ----> DAC3
11	S_{02}	A_{02} ----> M_2	B_{02} ----> DAC2
12	S_{01}	A_{01} ----> M_1	B_{01} ----> DAC1
13	S_{00}	A_{00} ----> M_0	B_{00} ----> DAC0

PIN DESCRIPTIONS

DIGITAL INPUT PINS:

SCLK: Serial register clock input, data is loaded from pin SDAT on each rising edge of SCLK while SENN is LO, standard TTL levels.

SDAT: Serial register data input, data on this pin is loaded into the serial register on each rising edge of SCLK while SENN is LO, standard TTL levels.

SENN: Serial register enable, standard TTL levels. A LO input enables the loading of the serial register using pins SCLK and SDAT. Data is transferred from the serial register to one of the parallel registers on the rising edge of SENN. Inputs at SCLK and SDAT are ignored while SENN is HI.

XRFI: Reference frequency input. A TTL clock at this pin will be the reference frequency for the frequency synthesizer. This input is selected by connecting pin XTAL1 to VCC1 and leaving pin XTAL2 open. This is a Schmitt-trigger input to improve false clock immunity.

DIGITAL OUTPUT PINS:

RFCKP, RFCKN: Frequency synthesizer VCO output pins, used as the code rate reference clock by the disk drive read/write channel. These pins are open emitter differential outputs, each requiring an external 511Ω pull-down resistor to VEE1. The output levels are uncompensated ECL and should be used with a differential ECL receiver.

XRFOP, XRFON: Crystal oscillator output pins. These pins are open emitter differential outputs, each requiring an external 511Ω pull-down resistor to VEE1 when in active use. The output levels are uncompensated ECL and should be used with a differential ECL receiver. Or the outputs should be allowed to float when not used. These outputs are active only when the crystal oscillator frequency reference is selected (pin XRFI grounded) or in a test mode when pin XTAL1 is forced to 2.0 volts and pin XTAL2 is left open.

ANALOG PINS:

DSDI: Data Separator DAC current input, the resistor R_{DSDI} connected between pin DSDI and VEE2 sets the current reference for the DAC that drives currents at pins DSVCO and DSQP. The voltage at pin DSDI has a slight current dependence which is represented by an output impedance term in series with R_{DSDI} in the DAC current equations given previously in the section describing the DACs.

DSQP: Data Separator DAC charge pump current output. This pin sinks the "1-X" current set by the Data Separator DAC in an NPN open collector configuration. The expression for the current output at pin DSQP is given in the section describing the Data Separator DAC.

DSVCO: Data Separator DAC VCO current output. This pin sinks the "X" current set by the Data Separator DAC in an NPN open-collector configuration. The expression for the current output at pin DSVCO is given the the section describing the Data Separator DAC.

FILTREF, LPFILT: Differential loop filter pins for the frequency synthesizer's phase locked loop. The filter RC network is connected between these pins as shown in the Typical Connection Diagrams. Pin FILTREF is a low impedance reference node with a voltage of 2.34 volts at nominal supply voltage. This voltage moves with supply voltage at a rate of VCC2/2. Pin LPFILT, the Charge Pump output pin, drives the Charge Pump output current into the loop filter. The VCO center frequency occurs when the voltage between pin FILTREF and LPFILT is zero. The dynamic range on pin LPFILT relative to pin FILTREF is about ±1.0 volts. The VCO frequency can be controlled directly by forcing a differential voltage between the loop filter pins.

RFDI: Reference DAC current input, the resistor RRFDI connected between pin RFDI and VEE2 sets the current reference for the internal DAC the drives the frequency synthesizer's VCO and Charge Pump circuits. The voltage at pin RFDI has a slight current dependence which is represented by an output impedance term in series with RRFDI in the DAC current equations given previously in the section describing the DACs.

XTAL1, XTAL2: Crystal oscillator input pins. If the crystal oscillator frequency reference is desired, a series mode crystal (and an RLC network if an overtone crystal is used) is connected between pins XTAL1 and XTAL2. Pin XRFI must be grounded to select the crystal oscillator frequency reference and to activate the crystal oscillator output pins XRFOP and XRFON. To select the TTL reference frequency source, pin XTAL1 is connected to VCC1 and pin XTAL2 is left open. A test mode with pin XTAL1 force to 2.0 volts and pin XTAL2 open permits the complement of the TTL reference frequency to appear between pins XRFOP and XRFON.

SUPPLY PINS:

VCC1: Digital power, +5.0 volts

VCC2: Analog power, +5.0 volts

VEE1: Digital ground

VEE2: Analog ground

DC CHARACTERISTICS Unless otherwise specified, all parameters are measured over the specified operating ranges, all voltages are measured with respect to ground, positive current flows into the device pin, all ECL outputs are terminated to ground with 511Ω resistors, and resistors R_{DSDI} and R_{RFDI} are ±1.0% in value. Further, unless otherwise specified, the supply voltages V_{CC1} and V_{CC2} will always be equal and will be abbreviated as V_{CC} in the specifications below.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Current						
Total Current	I_{CC}				130	mA
Digital Supply	I_{CC1}			55		mA
		All ECL Outputs Open		65		mA
Analog Supply	I_{CC2}			15		mA
TTL Inputs (Note 1)						
Input HI Voltage	V_{IH}	Except pin XRFI	2.0			V
Input LO Voltage	V_{IL}	Except pin XRFI			0.8	V
Input HI Current	I_{IH}	V_{CC} = 4.5V, V_{IH} = 2.7V			20	µA
Input HI Current	I_{IH}	V_{CC} = 4.5V, V_{IH} = 6.0V			100	µA
Input LO Current	I_{IL}	V_{IL} = 0.4V			-0.4	mA
Input Clamp Volts	V_{IK}	I_{IN} = -18mA			-1.5	V
Rise Threshold	V_{TH+}	Pin XRFI Only	1.4		1.9	V
Fall Thresold	V_{TH-}	Pin XRFI Only	0.5		1.0	V
Hystersis	V_{TH+}	Pin XRFI Only	0.4			V
ECL Outputs (Note 2)						
Output HI Voltage	V_{OH}	V_{CC} = 4.5V, T_A = 0°C	3.98		4.16	V
Output HI Voltage	V_{OH}	V_{CC} = 4.5V, T_A = 25°C	4.02		4.19	V
Output HI Voltage	V_{OH}	V_{CC} = 4.5V, T_A = 70°C	4.08		4.26	V
Output LO Voltage	V_{OL}	V_{CC} = 5.0V	3.05		3.37	V
Analog Pins						
DAC Output Current Accuracy	I_{DSVCO}			±2.0		% Full Scale
DAC Output Current Accuracy	I_{DSQP}			±2.0		% Full Scale
Voltage Compliance DAC pin DCVCO			3.5		7.5	V
Voltage Compliance DAC pin DSQP			3.5		7.5	V
DS DAC Bias	V_{DSDI}	R_{DSDI} = 1.30KΩ		1.13		V
Ref DAC Bias	V_{RFDI}	R_{RFDI} = 1.30KΩ		1.13		V
Filter Bias	$V_{FILTREF}$	V_{CC} = 4.5V		2.09		V
Filter Bias	$V_{FILTREF}$	V_{CC} = 5.0V		2.34		V
Filter Bias	$V_{FILTREF}$	V_{CC} = 5.5V		2.60		V

Note 1: TTL inputs will float to a logic HI if left unconnected.
Note 2: All outputs denoted as ECL are +5 volt referenced MECL 10KH compatible and track with the VCC supply voltage.

AC CHARACTERISTICS Unless otherwise specified, all parameters are measured over the specified operating ranges, all voltages are measured with respect to ground, positive current flows into the device pin, all ECL outputs are terminated to ground with 511Ω resistors, and resistors R_{DSDI} and R_{RFDI} are ±1.0% in value. Further, unless otherwise specified, the supply voltages V_{CC1} and V_{CC2} will always be equal and will be abbreviated as V_{CC} in the specifications below.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Phase Lock Loop						
VCO Center Frequency	F_{CVCO}	$F_{CVCO} = (37500) I_{RFVCO}$		±15		%
VCO Gain	K_{VCO}	$K_{VCO} = 0.371\ F_{VCO}$		±15		%
VCO Dynamic Range			±25		±50	%
Phase Detector Gain	K_d	$K_d = (0.50) I_{RFQP}$		±10		%
Gain Product Accuracy	$K_{VCO}K_d$			±25		%
VCO Output Phase Noise		(Note 3)		75		psec rms
Output Rise Time	t_{ro}	At RFCKP, RFCKN	1.0		2.0	nsec
Output Fall Time	t_{fo}	At RFCKP, RFCKN	1.0		2.0	nsec
Crystal Oscillator						
Crystal Oscillator Phase Noise		(Note 4)		75		psec rms
Output Rise Time	t_{ro}	At XRFOP, XRFON	1.0		2.0	nsec
Output Fall Time	t_{fo}	At XRFOP, XRFON	1.0		2.0	nsec

Note 3: With pin XTAL1 connected to V_{CC}, 10MHz is forced into pin XRFI, M/N = 16/4, loop filter components C_{lf1} = 270pF, R_{lf} = 825Ω, C_{lf2} = 0.022μF. Phase noise is measured with an HP5370B or equivalent counter, set for 10,000 samples and 1σ limit.

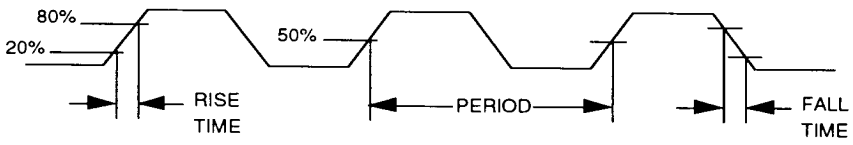
Note 4: Phase noise is measured with a HP5370B or equivalent counter, set for 10,000 samples, and 1σ limit.

SERIAL REGISTER

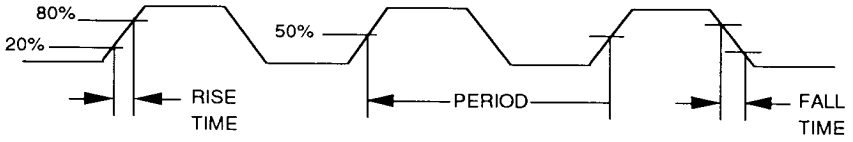
PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
SCLK Clock Rate					10	MHz
SDAT Setup Time			40			nsec
SDAT Hold Time			0			nsec
SENN Setup Time			40			nsec
SENN Hold Time			0			nsec
SENN Pulse Width			200			nsec

TIMING DIAGRAMS

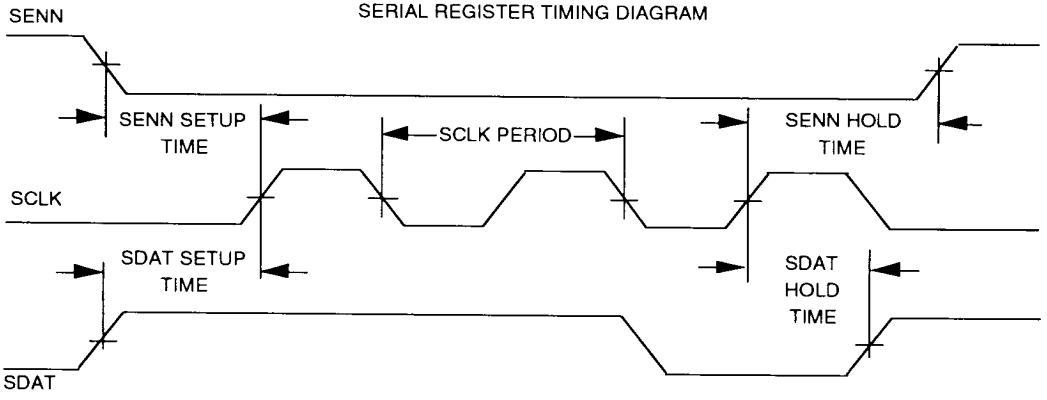
PHASE LOCK LOOP TIMING DIAGRAM



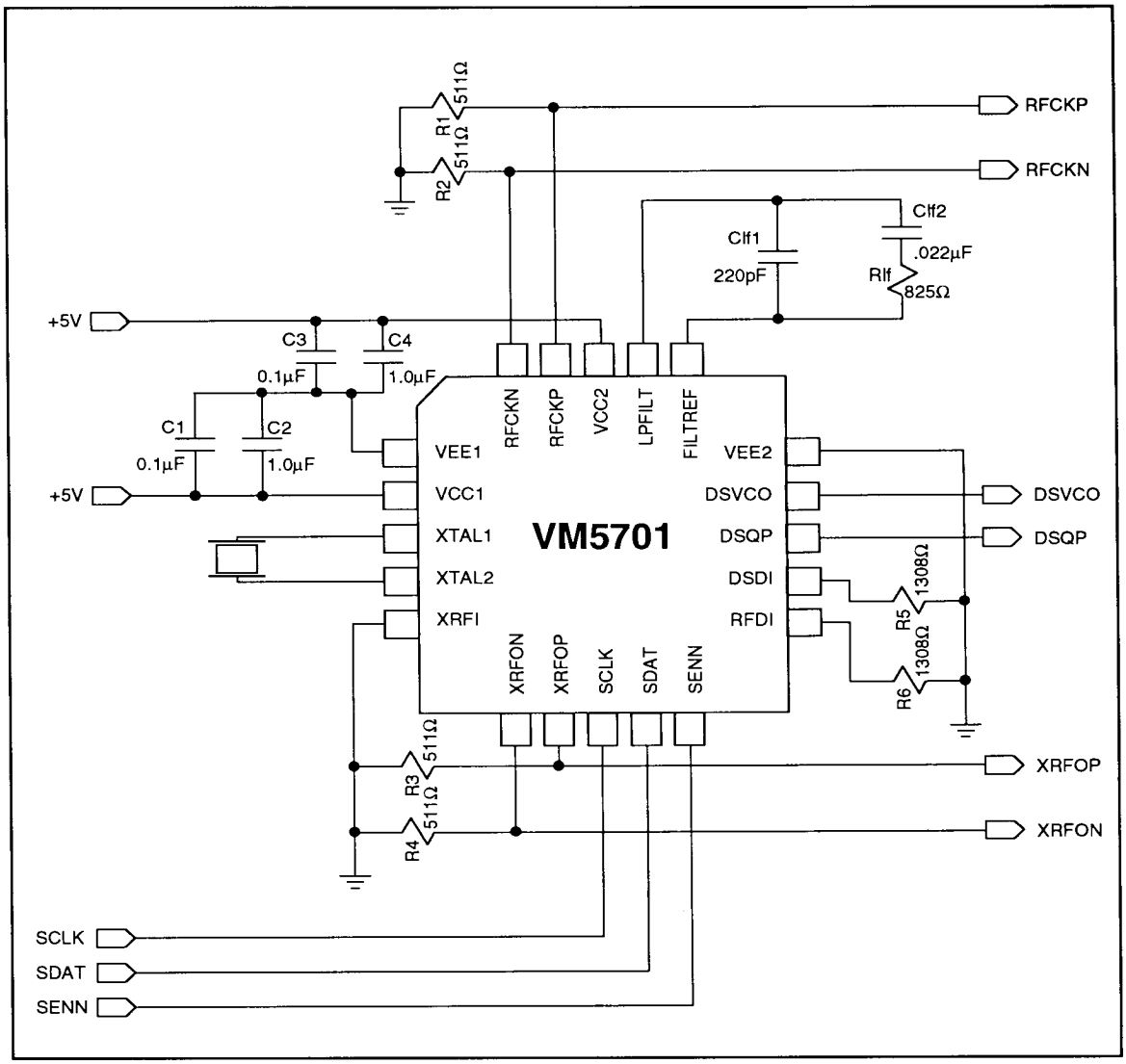
CRYSTAL OSCILLATOR TIMING DIAGRAM



SERIAL REGISTER TIMING DIAGRAM



TYPICAL CONNECTION DIAGRAM WITH TTL REFERENCE FREQUENCY



TYPICAL CONNECTION DIAGRAM WITH CRYSTAL OSCILLATOR