VLSI TECHNOLOGY, INC.

ADVANCE INFORMATION

VL82C113/VL82C113A

SCAMP™ COMBINATION I/O

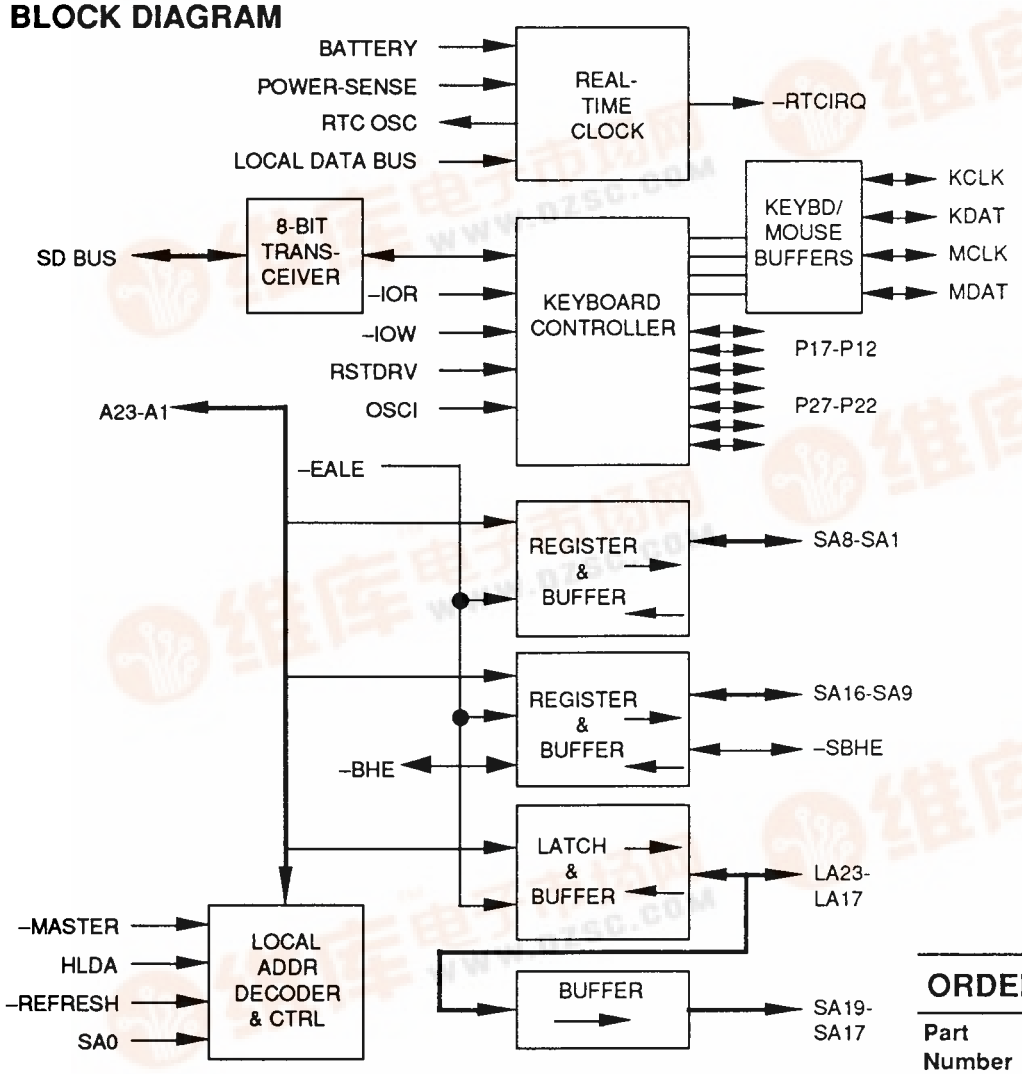
FEATURES

- Integrated peripheral controller for SCAMP™ VL82C310/VL82C311/ VL82C311L Single Chip PC/AT® Controllers
- 146818A-compatible real-time clock
- 64 additional bytes of battery-backed CMOS RAM
- AT-compatible keyboard controller with integrated PS/2® mouse support
- SCAMP-compatible processor to ISA bus address latches and buffers
- Real-time clock relocateable via SA15-SA0 address registers
- 1.0-micron CMOS in a 100-lead MQFP

DESCRIPTION

The VL82C113/VL82C113A SCAMP Combination I/O chip, when used with VLSI SCAMP chips, allows designers to implement a very cost-effective minimum chip count motherboard. This chip combines a keyboard controller and a real-time clock with the address registers/latches and buffers which are normally required in PC/AT-compatible systems. The VL82C113/VL82C113A features an AT-compatible keyboard controller with integrated PS/2 mouse support and a 146818A-compatible real-time clock. In addition, the VL82C113/VL82C113A has 64 additional bytes of battery-backed CMOS RAM for use in extended system setup.

BLOCK DIAGRAM

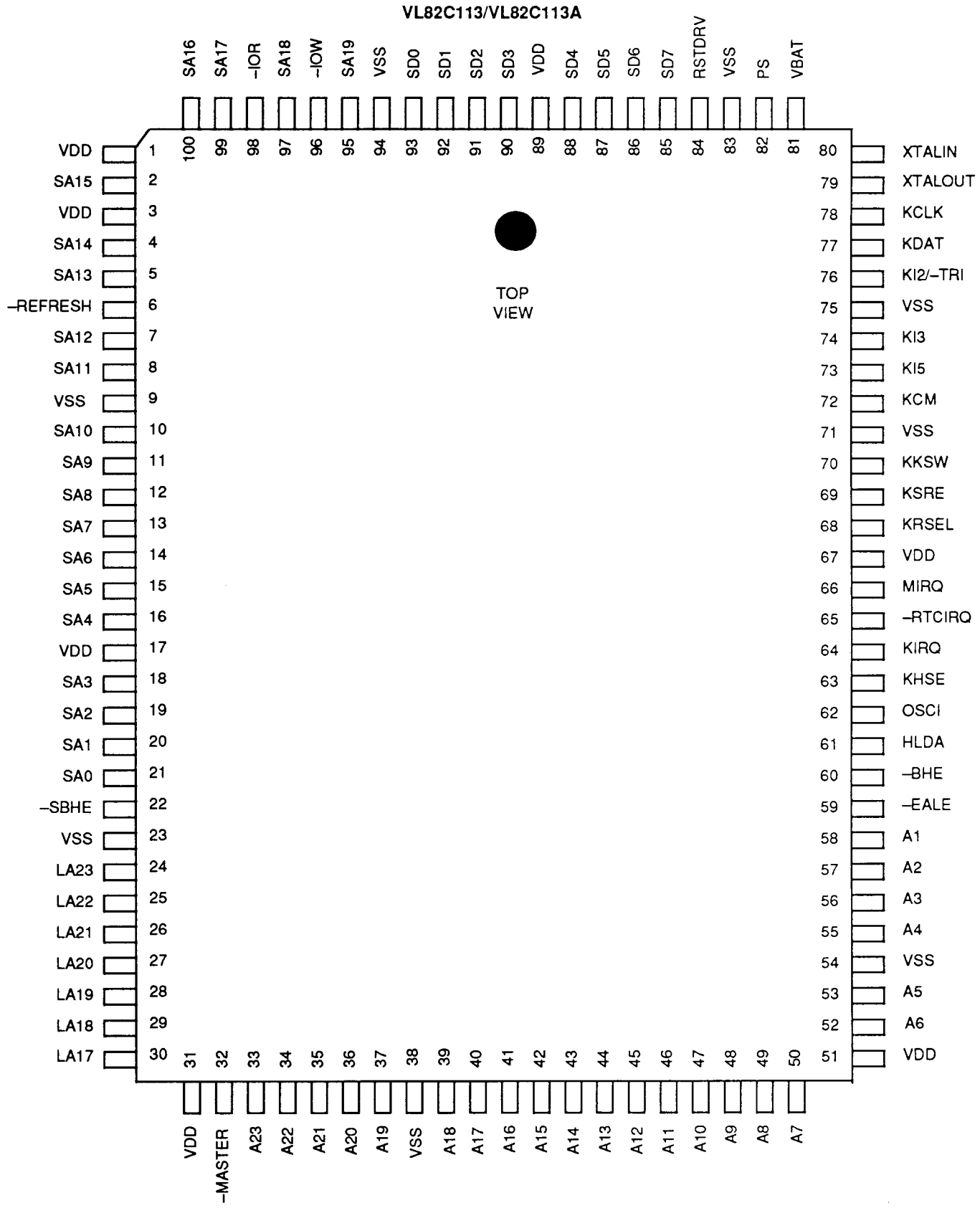


ORDER INFORMATION

Part Number	Package
VL82C113-FC	Metric Quad Flat Pack
VL82C113A-FC	Metric Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

PIN DIAGRAM


VL82C113/VL82C113A
TOP VIEW
1 VDD
2 SA15
3 VDD
4 SA14
5 SA13
6 –REFRESH
7 SA12
8 SA11
9 VSS
10 SA10
11 SA9
12 SA8
13 SA7
14 SA6
15 SA5
16 SA4
17 VDD
18 SA3
19 SA2
20 SA1
21 SA0
22 –SBHE
23 VSS
24 LA23
25 LA22
26 LA21
27 LA20
28 LA19
29 LA18
30 LA17
31 VDD
32 –MASTER
33 A23
34 A22
35 A21
36 A20
37 A19
38 VSS
39 A18
40 A17
41 A16
42 A15
43 A14
44 A13
45 A12
46 A11
47 A10
48 A9
49 A8
50 A7
51 VDD
52 A6
53 A5
54 VSS
55 A4
56 A3
57 A2
58 A1
59 –EALE
60 –BHE
61 HLDA
62 OSCI
63 KHSE
64 KIRQ
65 –RTCIRQ
66 MIRQ
67 VDD
68 KRSEL
69 KSRE
70 KKSW
71 VSS
72 KCM
73 KI5
74 KI3
75 VSS
76 KI2/–TRI
77 KDAT
78 KCLK
79 XTALOUT
80 XTALIN
81 VBAT
82 PS
83 VSS
84 RSTDRV
85 SD7
86 SD6
87 SD5
88 SD4
89 VDD
90 SD3
91 SD2
92 SD1
93 SD0
94 VSS
95 SA19
96 –IOW
97 SA18
98 –IOR
99 SA17
100 SA16

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS			
HLDA	61	I-TTL	Hold Acknowledge - This is the hold acknowledge pin directly from the CPU. It is used to control direction on address and to enable the –DACK decoder.
A23-A1	33-37, 39-50, 52, 53, 55-58	IO-TTL (8 mA)	Address bus bits 23 through 1 - When HLDA is high, –MASTER is low and –REFRESH is high these signals are outputs . They are inputs at all other times.
–BHE	60	IO-TTL (8 mA)	Byte High Enable - This pin is an output during Master Mode non-refresh cycles and it tracks the –SBHE input. It is an input at all other times.
ISA BUS SIGNALS			
RSTDRV	84	I-TTL	System Reset - This active high input is a system reset generated from the POWERGOOD input.
–IOR	98	I-TTL	I/O Read command.
–IOW	96	I-TTL	I/O Write command.
–MASTER	32	I-TTL	Master - This active low input is used by an external device to disable the internal DMA controllers and get access to the system bus. When asserted, it indicates that an external Bus Master has control of the bus.
–REFRESH	6	I-TTL	Refresh - This active low I/O signal is pulled low whenever a refresh cycle is initiated.
LA23-LA17	24-30	IO-TTL (24 mA)	Latchable Address bus bits 23 through 17 - This bus is an input when HLDA is high, –REFRESH is high and –MASTER is low. It is an output bus driven by the values from the A bus when HLDA is low and –REFRESH is high. It is three-stated when HLDA is high and –REFRESH is low. The LA bus is latched internally with the –EALE input.
SA19-SA9	95, 97, 99, 100, 2, 4, 5, 7, 8, 10, 11	IO-TTL (24 mA)	System Address bus bits 19 through 9 - This bus is an input when HLDA is high, –REFRESH is high and –MASTER is low. It is an output bus driven by the values from the A bus when HLDA is low and –REFRESH is high. It is three-stated when HLDA is high and –REFRESH is low. The SA19-SA9 bus is registered internally with the –EALE input.
SA8-SA1	12-16, 18-20	IO-TTL (24 mA)	System Address bus bits 8 through 1 - This bus is an input when HLDA is high, –REFRESH is high and –MASTER is low. It is an output bus driven by the values from the A bus at all other times. The SA8-SA1 bus is registered internally with the –EALE input. In the VL82C113A only, this bus is an output driven by the value of the internal refresh counter, rather than by the values on the A bus, when –REFRESH is low.
SA0	21	I-TTL	System Address bus least significant bit (LSB) - This is an input at all times and is used in the address decode of internal peripheral registers/ports.
–SBHE	22	IO-TTL (24 mA)	System Byte High Enable - This pin is controlled the same way as the SA bus. –SBHE is latched internally with the –EALE input.
OSCI	62	I-TTL	Oscillator Input - The input for the 14.318 MHz oscillator.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description			
KEYBOARD CONTROLLER SIGNALS						
			Keyboard Controller Mode			
			PC/AT Mode KBDCTRL1 = 1		**PS/2 Mode KBDCTRL1 = 0**	
KCLK	78	**PC/AT Mode** IO-TTL (12 mA) **PS/2 Mode** IO-TODS (12 mA)	T0/-P26	Kbd Clock	T0/-P26	Kbd Clock
KDAT	77	**PC/AT Mode** IO-TTL (12 mA) **PS/2 Mode** IO-TODS (12 mA)	T1/P27	Kbd Data	P10/-P27	Kbd Data
KCM	72	I-TPU	P16	Color Input	P16	Input
KKSW	70	I-TPU	P17	Key Switch	P17	Input
KHSE	63	IO-TODS (12 mA)	P22	High Speed	P11/-P22	Mouse Data
KSRE	69	IO-TODS (12 mA)	P23	Shadow RAM	T1/-P23	Mouse Clock
KIRQ	64	IO-TPU (4 mA)	P24	Kbd Int Req	P24	Kbd Int Req
			This pin is sampled on the high-to-low transition of RSTDRV. If KIRQ is low, the keyboard function within the VL82C113/VL82C113A is disabled. If KIRQ is high, the keyboard is enabled. This pin is internally pulled up to VDD.			
MIRQ	66	O (4 mA)	P25	General Purpose Output	P25	Mouse Int Req
KRSEL	68	I-TTL	P14	RAM Slct	P14	Input
KI2/–TRI	76	I-TPU	P12	Input	P12	Fuse Input
			This pin is sampled on the high-to-low transition of RSTDRV. If KI2/–TRI is low, all outputs will be three-stated. If KI2/–TRI is high, the chip will function normally. This pin is internally pulled up to VDD.			
KI3	74	IO-TPU (4 mA)	P13 MISC0	Input Output	P13 MISC0	Input Output
KI5	73	IO-TPU (4 mA)	P15 MISC1	Input Output	P15 MISC1	Input Output
SD DATA BUS SIGNALS						
SD7-SD0	85-88, 90-93	IO-TTL (24 mA)	System Data bus bits 7 through 0 - This bus connects directly to the slots. It is used to transfer data to/from the low byte of local and system devices.			
PERIPHERAL INTERFACE SIGNALS						
XTALIN	80	I-CMOS	The internal oscillator input for real-time clock crystal. It requires a 32.768 KHz external crystal or stand-alone oscillator.			
XTALOUT	79	O	The internal oscillator input for real-time clock crystal. See XTALIN. This pin is a "no connect" when an external oscillator is used.			
PS	82	I-TST	Power-Sense - An (active-high) input used to reset the status of the Valid RAM and Time (VRT) bit. This bit is used to indicate that the power has failed, and that the contents of the real-time clock may not be valid. This pin is connected to an external RC network.			

SIGNAL DESCRIPTION (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
VBAT	81	I-TTL	Connected to the real-time clock's hold up battery between 2.4 and 5 volts.
–RTCIRQ	65	IO-TODP (12 mA)	Real-Time Clock Interrupt Request output (active low) - This pin is an input when RSTDRV is high. It is sampled on the high-to-low transition of RSTDRV. If –RTCIRQ is low, the real-time clock's function within the VL82C113/VL82C113A is disabled. If –RTCIRQ is high, the real-time clock is enabled. Open drain output.
ADDRESS BUS CONTROL SIGNAL			
–EALE	59	I-TTL	Early Address Latch Enable - An active low pulse that is generated at the beginning of any bus cycle initiated from the CPU which is not directed at the on-board DRAM.
POWER AND GROUND PINS			
VDD	1, 3, 17, 31, 51, 67, 89	PWR	Power Connection, nominally +5 volts.
VSS	9, 23, 38, 54, 71, 75, 83, 94	GND	Ground Connection, 0 volts.

SIGNAL LEGEND

Signal Code	Signal Type
I-CMOS	CMOS level input
I-TTL	TTL level input
I-TPU	TTL level input with 30k ohm pull-up resistor
I-TST	TTL level Schmitt-trigger input
IO-TTL	TTL level input/output
IO-TOD	TTL level input/output open drain
IO-TODNP	TTL level input/output open drain with 3k ohm NMOS pull-up
IO-TODPU	TTL level input/output open drain with 30k ohm pull-up resistor
IO-TODS	TTL level with open drain output/Schmitt-trigger input
IO-TPU	TTL level input/output with 30k ohm pull-up resistor
O	CMOS and TTL level compatible output
GND	Ground
PWR	Power

GENERAL DESCRIPTION & PROGRAMMER'S MODEL

The VL82C113/VL82C113A SCAMP Combination I/O chip combines a keyboard controller and real-time clock (RTC) with the address registers/ latches buffers which are normally required in SCAMP-based systems. While the VL82C113/VL82C113A has been optimized for use with the VL82C310/VL82C311/VL82C311L SCAMP Controllers, its uses are not restricted to this device combination.

The keyboard controller and real-time clock are enabled/disabled through a combination of hardware and software accessible mechanisms. Software accessible registers are programmed through a series of indexing registers. In this scheme, one register (Index Register) is loaded with an 8-bit value which represents the address of the control/data register located within the VL82C113/VL82C113A which is to be read or written. The second register (Data Register) represents the datapath to the register pointed to by the Index Register. One pair of indexed registers are used with the VL82C113/ VL82C113A and are extensions of the registers used by the VL82C310/ VL82C311/VL82C311L SCAMP Controllers. These index/data registers are located at the same location within the VL82C310/VL82C311/VL82C311L SCAMP Controller as they are in the VL82C113/VL82C113A. The INDEX2 Register is write-only. DATA2 can be read as well as written. Table 1 details the ISA I/O address for the Index Registers as well as the default addresses for the real-time clock and keyboard controller.

Default values for these control registers have been selected so as to eliminate the need to change their values in typical system configurations when the VL82C113/VL82C113A is configured for Chip Select Mode of operation.

Table 2 shows the the INDEX2 addresses.

Table 3 details the Control, Status and Configuration Registers for the VL82C113/VL82C113A.

TABLE 1. ISA I/O ADDRESS MAP

I/O Address	Register Name	Description
0060 Hex	KBDAT	Keyboard Controller Input/Output Buffer
0064 Hex	KBDCTL	Keyboard Controller Status/Command Register
0070 Hex	RTCADD	Real-Time Clock Address Register
0071 Hex	RTCDAT	Real-Time Clock Data Registers
00EC Hex	INDEX2	Configuration INDEX2 Register
00ED Hex	DATA2	Configuration DATA2 Register

TABLE 2. INDEX2 ADDRESSES

(INDEX2 loc = 00ECh, DATA2 loc = 00EDh)

Index Address	Register Name	Description	Read/ Write
1B Hex	RTCLSB	RTC Register Address Register - Low Byte	R/W
1C Hex	RTCMSB	RTC Register Address Register - High Byte	R/W
1D Hex	KBDCTRL	Keyboard Controller Control Port	R/W
1F Hex	REVID	ID/Revision Register	R-O

RTC ADDRESS MAPPING REGISTER - LOW ADDRESS BYTE (RTCLSB)
Index Register: ECh
Index Address: 1Bh
Data Register: EDh
Default: 71h

Bit 0 RENA - RTC Enable: If set, when SA15-SA1 match the 15-bit compare value in RTCLSB and RTCMSB, an access to the RTC is generated. If cleared, all accesses to the RTC are disabled. Power-on reset default = 1.

Bits 1-7 Lower Seven bits of RTC Mapping Address: Combined with RTCMSB, this determines the address at which the RTC is accessed.

RTC ADDRESS MAPPING REGISTER - HIGH ADDRESS BYTE (RTCMSB)
Index Register: ECh
Index Address: 1Ch
Data Register: EDh
Default: 00h

Bits 0-7 Upper Byte of RTC Mapping Address: Combined with RTCLSB, this determines the address at which the RTC is accessed.

MISCELLANEOUS CONTROL REGISTER (KBDCTRL)
Index Register: ECh
Index Address: 1Dh
Data Register: EDh

Bit 0 Reserved: This bit must be written as 1. Power-on reset default = 1.

Bit 1 MODE - AT/PS2 Mode Select: If set, the keyboard operates in the AT compatibility mode. If cleared, the keyboard operates in the PS/2 keyboard and mouse mode. Power-on reset default = 1.

TABLE 3. CONTROL, STATUS AND CONFIGURATION REGISTERS BIT DEFINITIONS

Register Name	D7	D6	D5	D4	D3	D2	D1	D0
RTCLSB	A7	A6	A5	A4	A3	A2	A1	RENA
RTCMSB	A15	A14	A13	A12	A11	A10	A9	A8
KBDCTRL	RES	RES	INOROUT	MISC1	MISC0	PRV	MODE	RES
REVID	1	1	0	0	0	0	0	0

Bit 2 PRV - Private Controls Enable: If set, this bit prevents the KHSE, KSRE, and MIRQ pins from changing current state. If cleared, normal operation of these pins result. Power-on reset default = 0.

Bit 3 MISC0 - KI3 Output: If the INOROUT bit is set, then this bit controls the KI3 output pin directly. If the INOROUT bit is cleared, then this bit's state has no effect. This bit is typically used for Turbo Mode control.

Bit 4 MISC1 - KI5 Output: If the INOROUT bit is set, then this bit controls the KI5 output pin directly. If the INOROUT bit is cleared, then this bit's state has no effect.

Bit 5 INOROUT - If this bit is set to 1, then KI3 and KI5 will be outputs. If set to 0, then KI3 and KI5 will be inputs, read via Port 1 of the keyboard controller. Power-on reset default = 0.

Bit 6 Reserved: This bit is reserved for possible future use. It must be written as a 1.

Bit 7 Reserved: This bit is reserved for possible future use. It must be written as a 1.

REVISION/CHIP ID REGISTER (REVID)
Index Register: ECh
Index Address: 1Fh
Data Register: EDh

Bits 0-7 REVID - Revision/ID: Returns value based on the version of the VL82C113. The value for the VL82C113 is C0h.

ADDRESS BUFFERING AND AUXILIARY LOGIC

The address buffering and logic provide buffered addresses to and from the slot bus to the CPU. Depending on machine state, the SA and LA slot address lines can either be directly driven, driven from clocked data from the CPU A address lines, three-stated, or become inputs to drive the address back toward the CPU. These states are given in Table 6 as a function of the HLDA, –MASTER, and –REFRESH input lines.

Refresh Counter

In the VL82C113A, a counter is provided to drive the refresh address on SA8-SA1 when –REFRESH is low. The refresh address does not have to be provided on the local CPU A bus, thus allowing decoupled refresh operation when used with the VL82C486. The counter increments on the rising edge of –REFRESH and is cleared during reset.

TABLE 4. ADDRESS LINE DECODE

HLDA	–MASTER	–REFRESH	Cycle Type	SA1-SA8	SA9-SA16, –SBHE	SA17-SA19	LA17-LA23	CPU A Bus
0	0	0	Illegal					
0	0	1	Illegal					
0	1	0	Illegal					
0	1	1	CPU	Clocked	Clocked	Clocked	Latched	Input
1	0	0	Master Refresh	Direct/ Counter	Three-state	Three-state	Three-state	Input
1	0	1	Master	Input	Input	Three-state	Input	Output Direct
1	1	0	Normal Refresh	Direct/ Counter	Three-state	Direct	Direct	Input
1	1	1	DMA	Direct	Direct	Direct	Direct	Input

Clocked: The value of the CPU A address line is clocked into a flip-flop on the rising edge of the –EALE and output on the SA lines.

Latched: The value of the CPU A address line is latched when –EALE is high.

Direct: The value of the CPU A address line is buffered and output on the SA/LA lines.

Output Direct: The value of the SA/LA lines are buffered and output to the CPU.

Three-state: The SA lines are floating.

Counter: In the VL82C113A only, the contents of the internal refresh counter are driven onto SA8-SA1 when –REFRESH is low. The refresh counter is not in the VL82C113, thus A8-A1 are directly buffered and output on SA8-SA1 during refresh.

KEYBOARD CONTROLLER

The keyboard controller is accessed via internally decoded port 060h (read/write data) and port 064h (read status/write command).

PC/AT or PS/2 compatibility is controlled via bit 1 in the KBDCTRL Register.

KEYBOARD CONTROLLER FUNCTIONAL DESCRIPTION

The VL82C113/VL82C113A keyboard controller's microcontroller unit (MCU) offers a subset of the instruction set of the 8042, with 8042-like instructions. Enhancements have been made to conditional jumps (jumps may be made between pages). The on-chip ROM is loaded with the code that is required to support the PC/AT and PS/2 command sets and 128 bytes of conversion code. A small amount of scratch-pad RAM is provided as an extension of the MCU register set for the purpose of keyboard to host interfacing.

Keyboard serial I/O is handled with hardware implementations of the receiver and transmitter. Both functions depend on an 8-bit timer for time-out detection. Enhanced status reporting is provided in hardware to simpilify error handling in software. This logic is duplicated for the mouse interface.

User RAM support is provided. The program writes the 5-bit address (32-byte range) to a register, and then reads or writes the data through accesses to another register, port 60h DBB.

Parallel ports 1 and 2 are provided, but are restricted to inputs only for P1 and outputs only for P2. In the VL82C113/VL82C113A, the P10 and P11 input pins are shared with P27 and P22 outputs, and the P20 and P21 outputs are eliminated.

Support for port 60h DBB (reads and writes) and the Status Register (reads and writes) is provided in hardware for interface to the PC host.

Common PC/AT uses for the parallel I/O bits are shown below.

- P16 - Color/monochrome input
- P17 - Key switch input
- P22 - Speed select output

KEYBOARD CONTROLLER INTERFACE TO PC/AT

The interface to the PC/AT consists of one register pair (60h/64h) for the keyboard and mouse. Access to the registers is determined by the state of A2 and the chip select. For host control signals involved, the Command, Status and Data Registers are accessed as shown in Table 5.

Port 60h DBB read operations output the contents of the output buffer to D7-D0 (host bidirectional, three-state data bus), and clears the status of the Output Buffer Full (OBF/Status Register bit 0) bit.

Status read operations output the contents of the Status Register to D7-D0. No status is changed as a result of the read operation.

Port 60h DBB write operations cause the input buffer DBB to be changed. The state of the C/D bit is cleared (Status Register bit 3, a 0 indicates data) and the Input Buffer Full (IBF/ Status Register, bit 1) bit is set (1).

Command write operations are the same as DBB writes, except that the address is 64h. The C/D bit will be set (1) when a command has been written to address 64h.

KEYBOARD CONTROLLER INTERFACE PROTOCOL

Data transmission between the controller and the keyboard or mouse consist of a synchronous bit stream over the data and clock lines. The bits are defined as follows:

Bit	Function
1	Start bit (always 0)
2	Data bit (LSB)
3-8	Data bits 1-6
9	Data bit 7 (MSB)
10	Parity bit (odd)
11	Stop bit (always 1)

RECEIVE AND TRANSMIT OPERATIONS

The states that are implemented for receive and transmit operations are in shown in Figures 1 and 2.

TABLE 5. ACCESSING THE COMMAND, STATUS, AND DATA REGISTERS

–CS	–IOR	–IOW	–A2	Register
0	0	1	0	Read - Data DBB Output Buffer
0	0	1	1	Read - Status
0	1	0	0	Write - Data DBB Input Buffer
0	1	0	1	Write - Command
1	X	X	X	Not Valid

Note: –CS is an internal signal which is the decode of A0-A15 from the register pair 60h/64h.

FIGURE 1. CONTROLLER RECEIVES FROM KEYBOARD

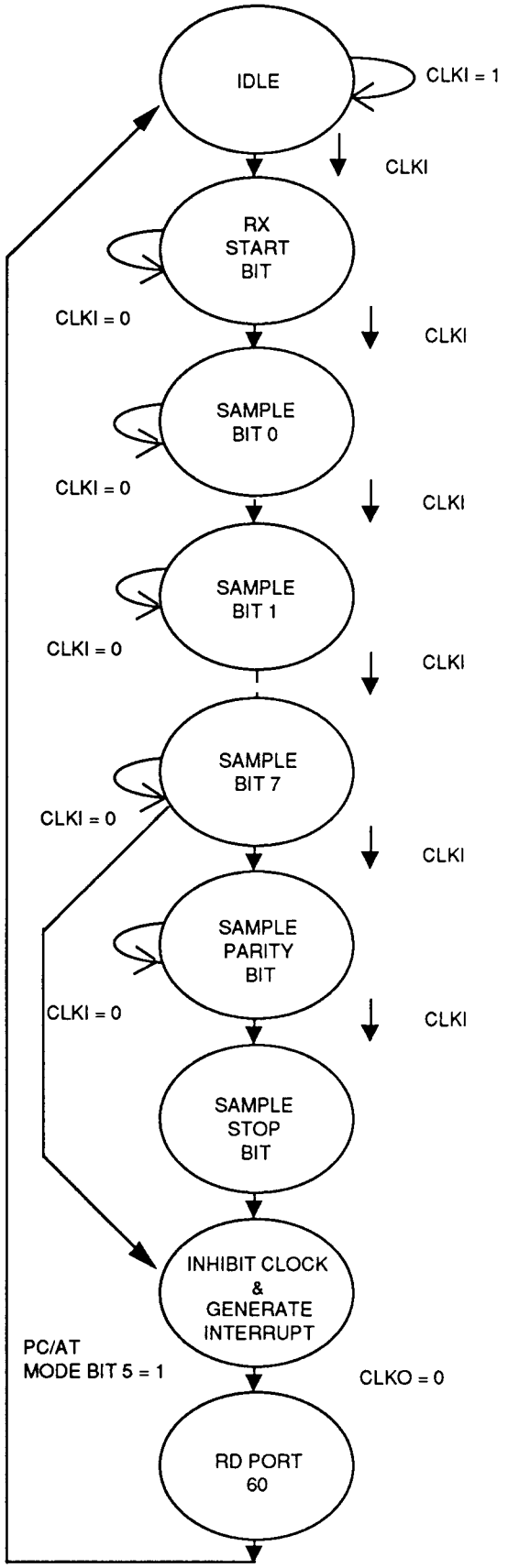
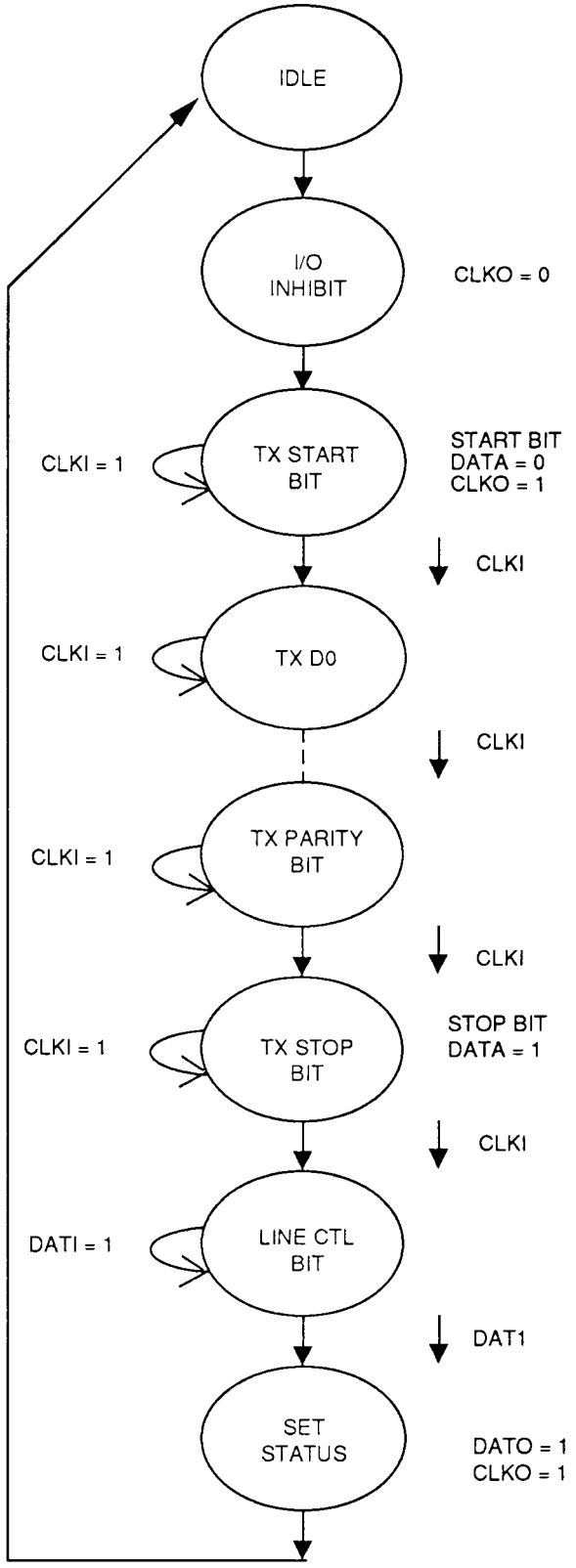


FIGURE 2. CONTROLLER TRANSMITS TO KEYBOARD



PROGRAMMER INTERFACE

The programmer interface to the keyboard controller is quite simple. It consists of the following four registers:

Register	R/W	I/O
Status	R	64h
Command	W	64h
Output Buffer	R	60h
Input Buffer	W	60h

The behavior of these registers differs according to the mode of operation (PC/AT or PS/2). There exists only one Status Register with different bit definitions for PC/AT Mode and PS/2 Mode. The bit definitions for the Status Register in each mode are listed in Tables 6 and 7.

PC/AT Status Register

Bit 0 OBF - Output Buffer Full: This flag is automatically set when the microcontroller loads DBBOUT. It is cleared on a read to port 60h.

Bit 1 IBF - Input Buffer Full: This flag is set on a write to port 60h or 64h. It is cleared when the microcontroller reads the DBBIN contents into the accumulator.

Bit 2 SYS - System Flag: When this bit is set (1), it indicates that the CPU has changed from Virtual to Real Mode.

Bit 3 C/D - Command/Data: When set (1), this bit indicates that a command has been placed into the input data buffer of the controller. A 0 indicates data. The controller uses this bit to determine if the byte written is a command to be executed. This bit is updated when the next byte is written to the input data buffer.

Bit 4 KBEN - Keyboard Enable: When set (1), this bit indicates that the keyboard is currently enabled. When reset, it indicates that the keyboard is inhibited.

Bit 5 TTIM - Transmit Time-Out: When set (1), it indicates that a transmission to the keyboard was not completed before the controller's internal timer timed-out.

Bit 6 RTIM - Receive Time-Out: When set (1), it indicates that a transmission from the keyboard was not completed before the controller's internal timer timed-out.

Bit 7 PERR - Parity Error: When set (1), it indicates that a parity error (even parity = error) occurred during the last transmission (received scan code) from the keyboard. When a parity error is detected, the output buffer is loaded with FFh, the OBF status bit is set, and the KIRQ pin is set (1 if the EKI bit/Mode Register bit 0 is set(1)).

TABLE 6. PC/AT STATUS REGISTER (Read-only, Port 64h)

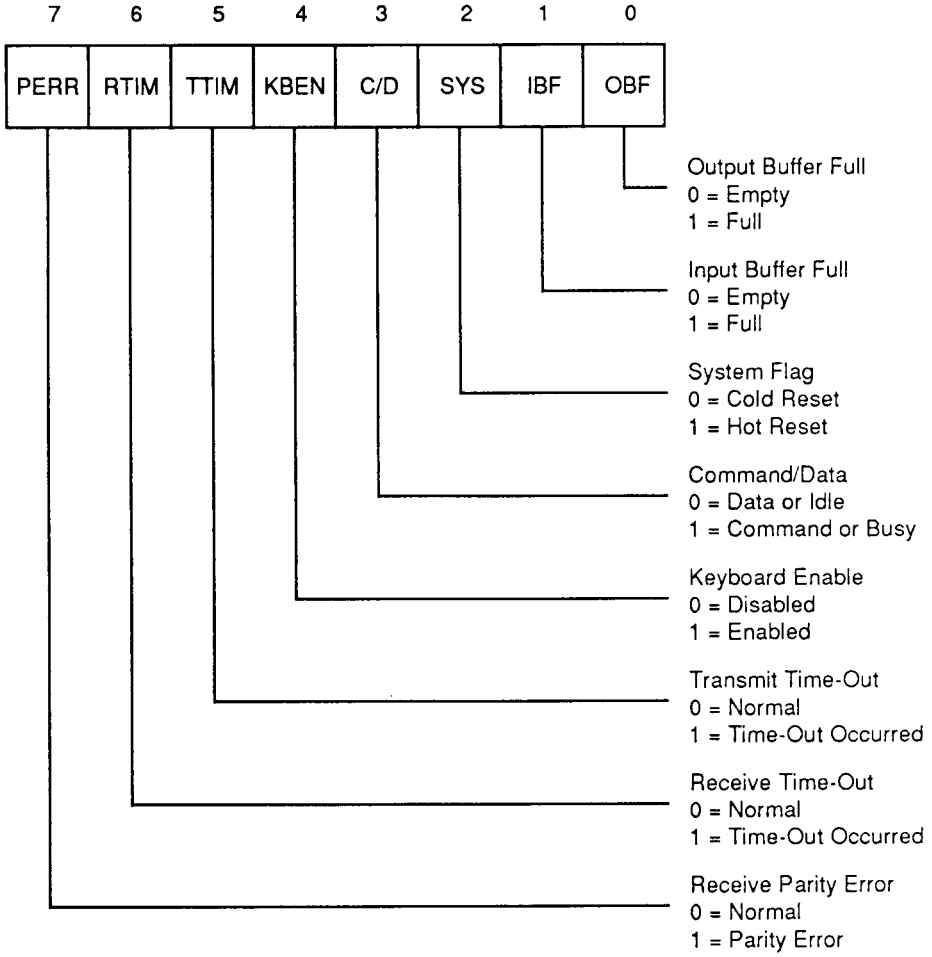
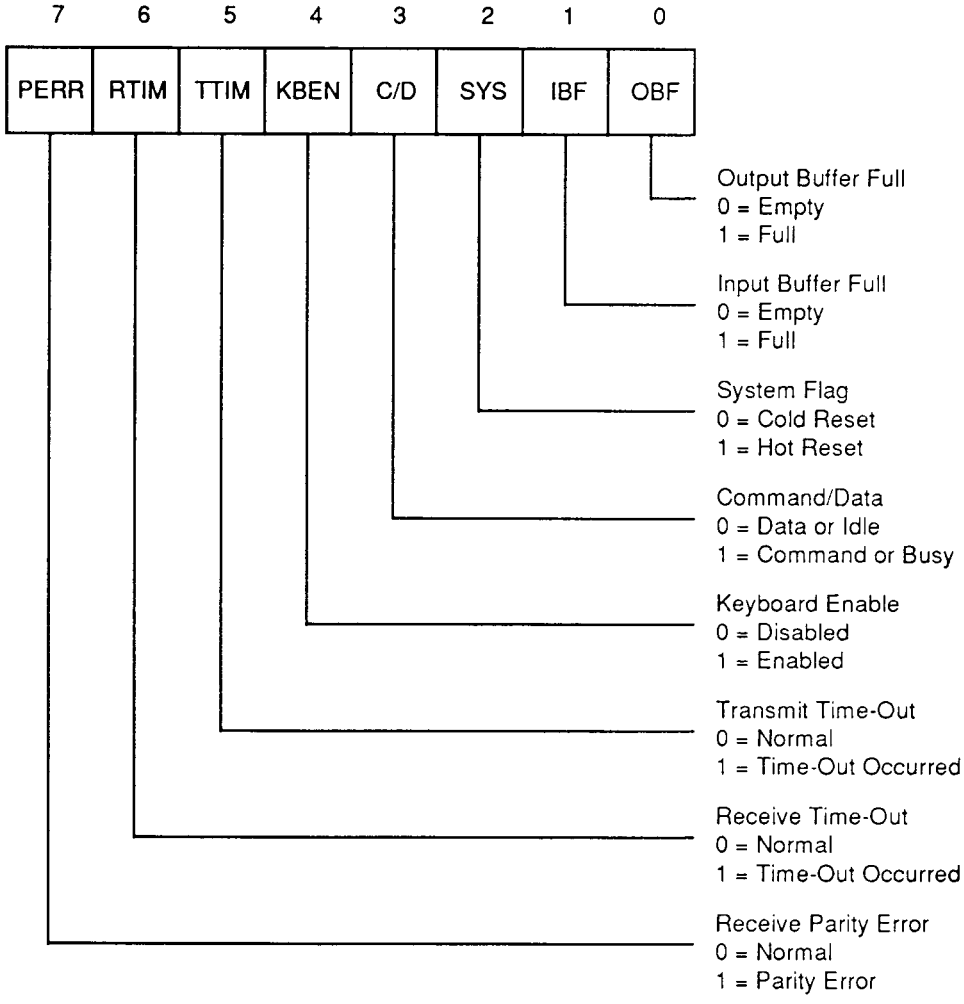


TABLE 7. PS/2 STATUS REGISTER (Read-only, Port 64h)



PS/2 Status Register

Bit 0 OBF - Output Buffer Full: This flag is automatically set when the microcontroller loads DBBOUT. It is cleared on a read to port 60h.

Bit 1 IBF - Input Buffer Full: This flag is set on a write to port 60h or 64h. It is cleared when the microcontroller reads the DBBIN contents into the accumulator.

Bit 2 SYS - System Flag: When set (1), it indicates that the CPU has changed from Virtual to Real Mode.

Bit 3 C/D - Command/Data: When set (1), it indicates that a command has been placed into the input data buffer of the controller. A 0 indicates data. The controller uses this bit to determine if the byte written is a command to be executed. This bit is updated when the next byte is written to the input data buffer.

Bit 4 KBEN - Keyboard Enable: When set (1), it indicates that the keyboard is currently enabled. When reset, it indicates that the keyboard is inhibited.

Bit 5 ODS - Output Buffer Data Source: When set (1), it indicates that the data in the output buffer is mouse data. When reset, it indicates the data is from the keyboard.

Bit 6 GTO - General Time-Out Error: When set (1), it indicates that a transmission was started and that it did not complete within the normal time taken (approximately 11 KCLK cycles). If the transmission originated from the controller, a FEh is placed in the output buffer. If the transmission originated from the keyboard, a FFh is placed in the output buffer.

Bit 7 PERR - Parity Error: When set (1), it indicates that a parity error (even parity = error) occurred during the last transmission from the keyboard. When a parity error is detected, the output buffer is loaded with FFH, the OBF status bit is set, and the KIRQ pin is set (1 if the EKI bit/ Mode Register bit 0 is set (1)).

KEYBOARD CONTROLLER COMMAND SET

This command supports two modes of operation and a set of extensions to the AT command set for the PS/2. In both modes, the command is implemented by writing the command byte to 64h. Any susequent data is read from 60h (see description for command 20 in Table 7) or written to 60h (see description of command 60, also in Table 7). The commands for each mode are shown in Tables 8 and 9.

Command Descriptions

The keyboard controller will support the following command set, which is described as the hex command code, followed by a description:

20 Read keyboard controller's Mode Register (PC/AT and PS/2). The keyboard controller sends its current mode byte to the output buffer (accessed by a read of port 60h).

60 Write keyboard controller's Mode Register (PC/AT and PS/2). The next byte of data written to the keyboard data port (60h) is placed in the controller's Mode Register.

The bit definitions of the Mode Register for each mode (PC/AT or PS/2) are described in Tables 10 and 11.

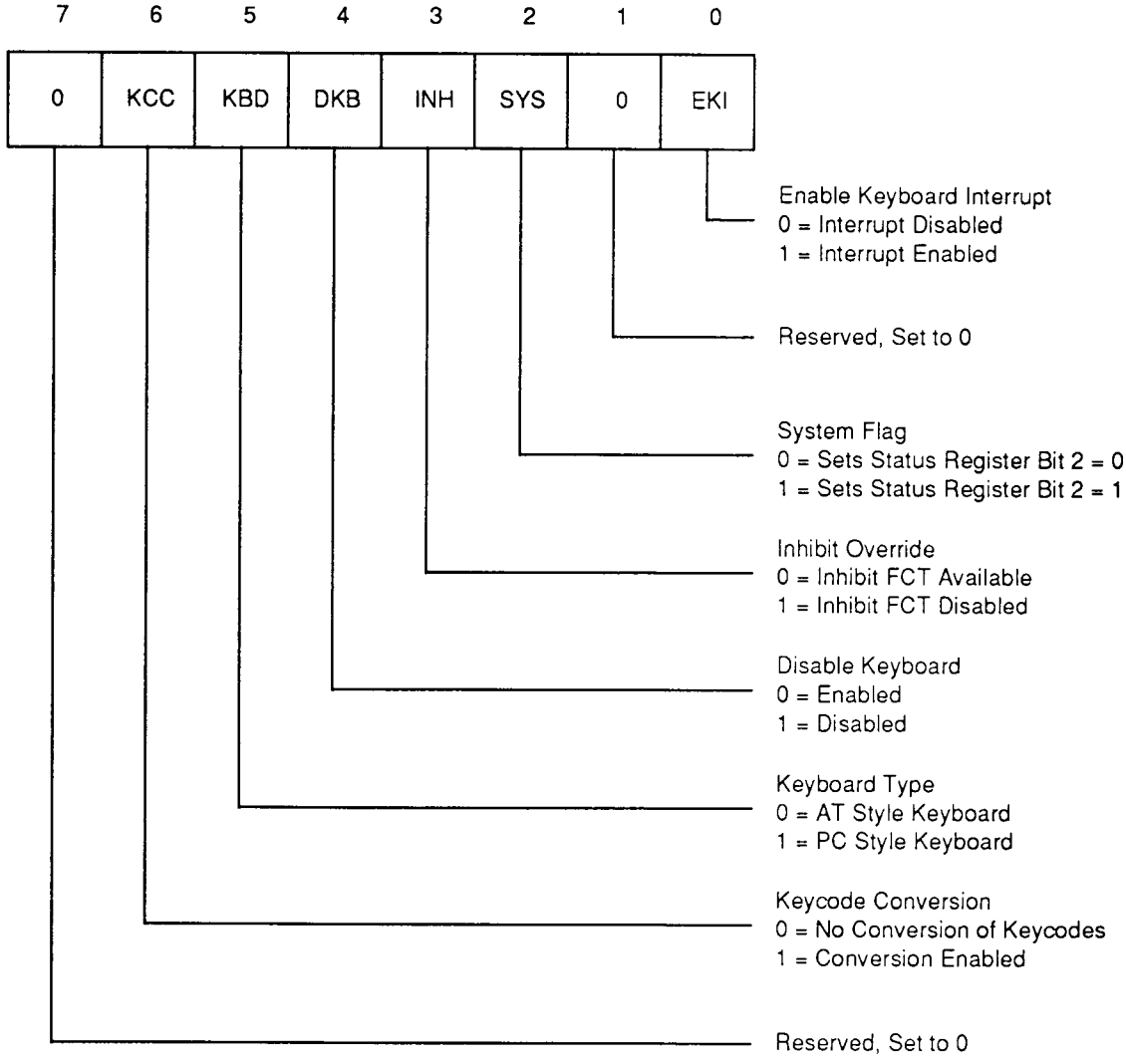
TABLE 8. PC/AT & PS/2 COMMANDS

Command	Description
20	Read Mode Register
60	Write Mode Register
21-3F	Read Keyboard Controller RAM (Byte 1-31)
61-7F	Write Keyboard Controller RAM (Byte 1-31)
AA	Self Test
AB	Keyboard Interface Test
AC	Diagnostic Dump
AD	Disable Keyboard
AE	Enable Keyboard
C0	Read Input Port (P10-P17)
D0	Read Output Port (P20-P27)
D1	Write Output Port (P20-P27)
E0	Read Test Inputs (T0, T1)
F0-FF	Pulse Output Port (P20-P27)

TABLE 9. ADDED PS/2 COMMANDS

Command	Description
A4	Test Password
A5	Load Password
A6	Enable Password
A7	Disable Mouse
A8	Enable Mouse
A9	Mouse Interface Test
C1	Poll Input Port Low (P10-P13 = S4-S7)
C2	Poll Input Port High (P14-P17 = S4-S7)
D2	Write Keyboard Output Buffer
D3	Write Mouse Output Buffer
D4	Write to Mouse

TABLE 10. PC/AT MODE REGISTER (R/W - Command 20h/60h to Port 60h)



PC/AT Mode Register

Bit 0 EKI - Enable Keyboard Interrupt: When set (1), it allows the controller to generate a keyboard interrupt whenever data (keyboard or controller) is written into the output buffer.

Bit 1 Reserved: This bit should be written as 0.

Bit 2 SYS - System Flag: When set (1), it writes the system flag bit 2 of the Status Register to 1. This bit is used to indicate a switch from Virtual to Real Mode when set.

Bit 3 INH - Inhibit Override: When set (1), it disables the keyboard inhibit function (P17 switch).

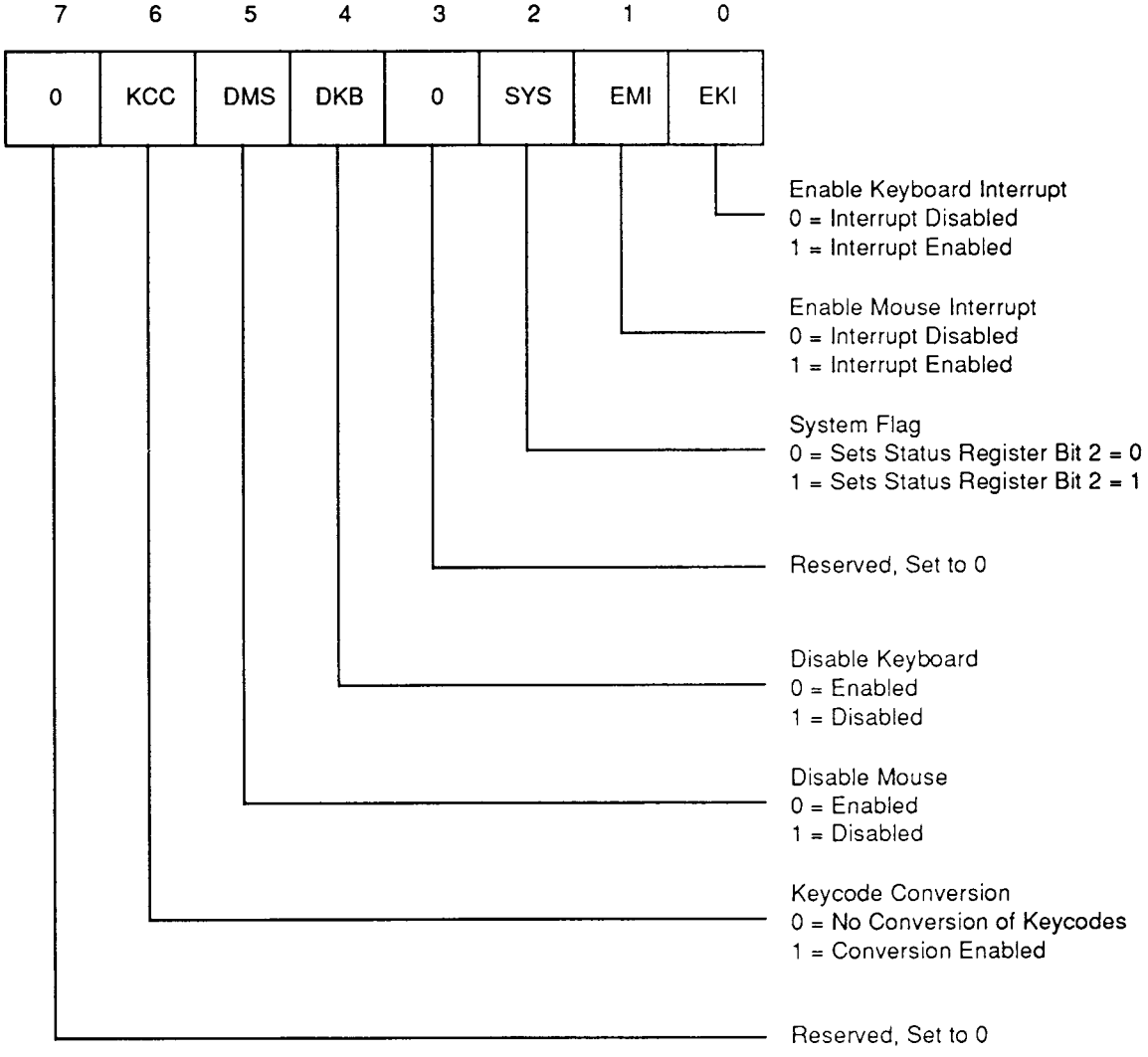
Bit 4 DKB - Disable Keyboard: When set (1), it disables the keyboard by holding the KCLK line high.

Bit 5 KBD - Keyboard Type: When set (1), it allows for compatibility with PC-style keyboards. In this mode, parity is not checked and scan codes are not converted.

Bit 6 KCC - Keycode Conversion: When set (1), it causes the controller to convert the scan codes to PC format. When reset, the codes are passed along unconverted.

Bit 7 Reserved: This bit should be written as 0.

TABLE 11. PS/2 MODE REGISTER (R/W - Command 20h/60h to Port 60h)



PS/2 Mode Register

Bit 0 EKI - Enable Keyboard Interrupt: When set (1), it allows the controller to generate a keyboard interrupt whenever data (keyboard or command) is written into the output buffer.

Bit 1 EMI - Enable Mouse Interrupt: When set (1), it allows the controller to generate a mouse interrupt when mouse data is available in the output buffer.

Bit 2 SYS - System Flag: When set (1), it writes the system flag bit 2 of the Status Register to 1. This bit is used to indicate a switch from Virtual to Real Mode when set.

Bit 3 Reserved: This bit should be written as 0.

Bit 4 DKB - Disable Keyboard: When set (1), it disables the keyboard by holding the KCLK output high.

Bit 5 DMS - Disable Mouse: When set (1), it disables the mouse by holding the KSRE output high in PS/2 Mode.

Bit 6 KCC - Keycode Conversion: When set (1), it causes the controller to convert the scan codes to PC format. When reset, the codes are passed along unconverted.

Bit 7 Reserved: This bit should be written as 0.

Command Descriptions (Cont.)

21-3F Read Keyboard Controller RAM (PC/AT and PS/2): Bits D4-D0 specify the address.

61-7F Write the Keyboard Controller RAM (PC/AT and PS/2): This command writes to the keyboard controller RAM with the address specified in bits D4-D0.

A4 Test Password Installed (PS/2 only): This command checks if there is currently a password installed in the controller. The test result is placed in the output buffer (the OBF bit is set) and KIRQ is asserted (if the EKI bit is set). Test result - FAh means that the password is installed, and F1h means that the password is not installed.

A5 Load Password (PS/2 only): This command initiates the password load procedure. Following this command, the controller will take data from the input buffer port (60h) until a 00h is detected or a full 8-byte password, including a delimiter (00h), is loaded into the password latches.

Note: This means that during password validation, the password can be a maximum of seven bytes plus a delimiter such as 00h.

A6 Enable Password (PS/2 only): This command enables the security feature. The command is valid only when a password pattern is written into the controller (see A5 command). All keyboard or mouse characters will be discarded until the correct security sequence is completed. System commands are still accepted.

A7 Disable Mouse (PS/2 only): This command sets bit 5 of the Mode Register which disables the mouse by driving the KSRE line (mouse clock) high.

A8 Enable Mouse (PS/2 only): This command resets bit 5 of the Mode Register, thus enabling the mouse again.

A9 Mouse Interface Test (PS/2 only): This command causes the controller to test the mouse clock and data lines. The results are placed in the output buffer (the OBF bit is set) and the KIRQ line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No Error
01	Mouse Clock Line Stuck Low
02	Mouse Clock Line Stuck High
03	Mouse Data Line Stuck Low
04	Mouse Data Line Stuck High

AA Self Test (PC/AT and PS/2): This commands the controller to perform internal diagnostic tests. A 55h is placed in the output buffer if no errors were detected. The OBF bit is set and KIRQ is asserted (if the EKI bit is set).

AB Keyboard Interface Test (PC/AT and PS/2): This command causes the controller to test the keyboard clock and data lines. The test result is placed in the output buffer (the OBF bit is set) and the KIRQ line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No Error
01	Keyboard Clock Line Stuck Low
02	Keyboard Clock Line Stuck High
03	Keyboard Data Line Stuck Low
04	Keyboard Data Line Stuck High

AC Diagnostic Dump (PC/AT only, reserved on PS/2): Sends 16 bytes of the controller's RAM, the current state of the input port, and the current state of the output port to the system.

AD Disable Keyboard (PC/AT and PS/2): This command sets bit 4 of the Mode Register to a 1. This disables the keyboard by driving the clock line (KCLK) low. Data will not be received. The keyboard will be enabled after the system sends data to be transmitted to the keyboard.

AE Enable Keyboard (PC/AT and PS/2): This command resets bit 4 of the mode byte to a 0. This enables the keyboard again by allowing the keyboard clock to free-run.

C0 Read P1 Input Port (PC/AT and PS/2): This command reads the keyboard input port and places it in the output buffer. This command overwrites the data in the buffer.

C1 Poll Input Port Low (PS/2 only): P1 bits 0-3 are written into Status Register bits 4-7. The bits are restored to their original status upon a write to port 64h.

C2 Poll Input Port High (PS/2 only): P1 bits 4-7 are written into Status Register bits 4-7. The bits are restored to their original status upon a write to port 64h.

D0 Read Output Port (PC/AT and PS/2): This command causes the controller to read the P2 output port and place the data in its output buffer. The definitions of the bits are as follows:

Bit	Pin	PC/AT Mode	PS/2 Mode
0	P20		
1	P21		
2	P22	Speed Sel (ENMOD)	Mouse Data
3	P23	Shadow Enable	Mouse Clk
4	P24	Output Buffer Full	KIRQ
5	P25		MIRQ
6	P26	-KCKOUT	-KCKOUT
7	P27	KDOUT	-KDOUT

D1 Write Output Port (PC/AT and PS/2): The next byte of data written to the keyboard data port (60h) will be written to the controller's output port. The definitions of the bits are as defined previously stated. In PC/AT Mode, P26 and P27 will not be altered. In PS/2 Mode, P22, P23, P26, and P27 cannot be altered.

D2 Write Keyboard Output Buffer (PS/2 only): The next byte written to the data buffer (60h) is written by the output buffer (60h) as if initiated by the keyboard (the OBF bit is set (1) and KIRQ will be set if the EKI bit is set (1)).

D3 Write Mouse Output Buffer (PS/2 only): The next byte written to the data buffer (60h) is written to the output buffer as if initiated by the mouse (the OBF bit is set (1), and MIRQ will be set if the EMI bit is set (1)).

D4 Write to Mouse (PS/2 only): The next byte written to the data buffer (60h) is transmitted to the mouse.

Note: If data is written to the data buffer (60h) and the command preceding it did not expect data from the port (60h), the data will be transmitted to the keyboard.

E0 Read Test Inputs (PC/AT and PS/2): This command causes the controller to read the T0 and T1 input bits. The data is placed in the output buffer with the following meanings:

Bit	PC/AT Mode	PS/2 Mode
0	Keyboard Clk	Keyboard Clk
1	Keyboard Data	Mouse Clk
3-7	Read as 0s	Read as 0s

F0-FF Pulse Output Port (PC/AT and PS/2): Bits 2 and 3 of the controller's output port may be pulsed low for approximately 6 µs. Bits 2 and 3 of the command specify which bit will be pulsed. A 0 indicates that the bit should be pulsed, a 1 indicates that the bit should not be modified. FF is treated as a special case (Pulse Null Port).

Note: In PS/2 Mode, bits P22 and P23 will not be pulsed.

REAL-TIME CLOCK DESCRIPTION

The real-time clock (RTC) portion of the VL82C113/VL82C113A performs the following functions:

- Time of day clock
- Alarm function
- 100 year calendar function
- Programmable periodic interrupt output
- Programmable square wave output
- 50 bytes of user RAM
- User RAM preset feature

The RTC memory consists of ten RAM bytes which contain the time, calendar, and alarm data, four control and status bytes, and 50 general purpose RAM bytes. The address map of the real-time clock is shown as follows:

Addr	Function	Range
0	Seconds (time)	0-59
1	Seconds (alarm)	0-59
2	Minutes (time)	0-59
3	Minutes (alarm)	0-59
4	Hours (time)	0-11, 12 Hr Mode
4	Hours (time)	0-23, 24 Hr Mode
5	Hours (alarm)	0-23
6	Day of Week	1-7
7	Date of Month	1-31
8	Month	1-12
9	Year	0-99
10	RTC Register A	(R/W/)
11	RTC Register B	(R/W)
12	RTC Register C	(R-O)
13	RTC Register D	(R-O)
14-127	User RAM (standby)	

All 64 bytes are directly readable and writeable by the processor program except for the following:

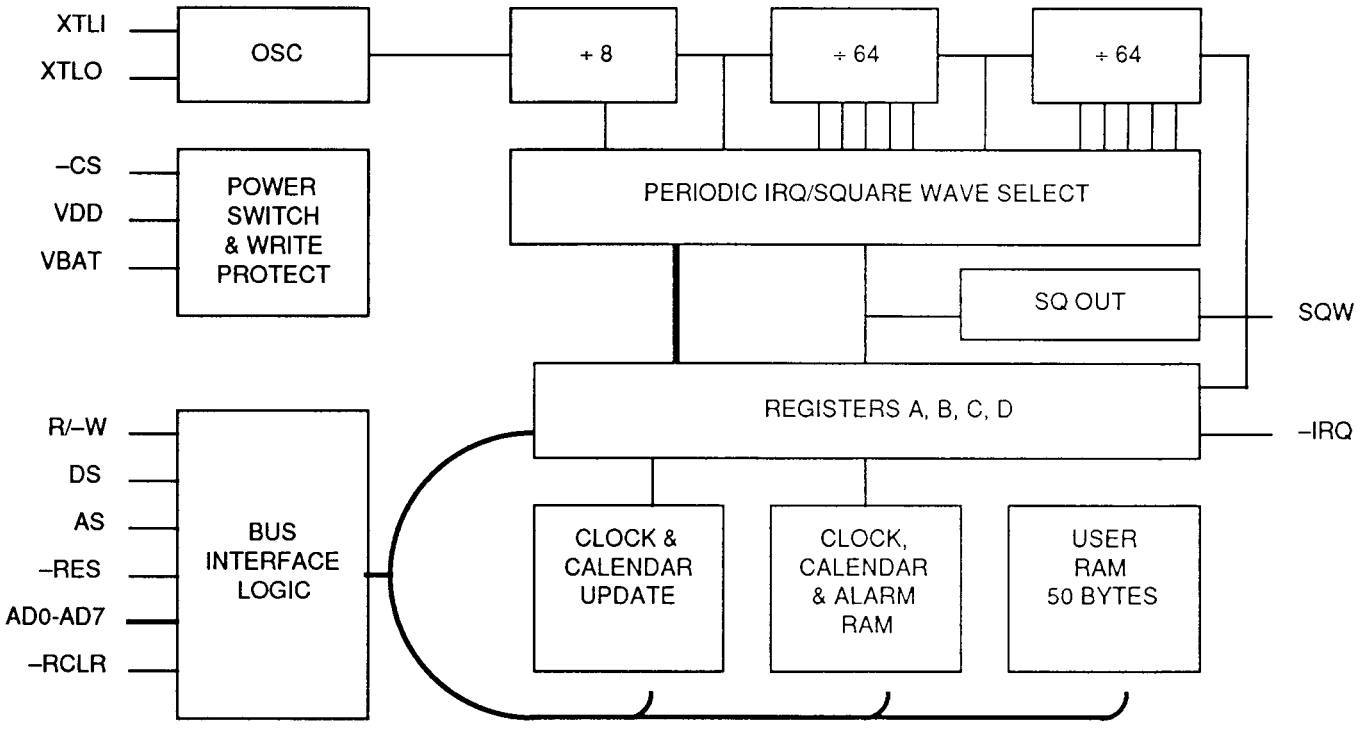
1) Registers C and D are read-only.
2) Bit 7 of Register A is read-only.
3) Bit 7 of the seconds byte is read-only.

The total address map is shown below:

Addr	Function
0-13	Time portion
14-63	Scratch-pad RAM portion
64-127	Additional scratch-pad RAM

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the ten time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

FIGURE 3. REAL-TIME CLOCK BLOCK DIAGRAM



TIME OF DAY REGISTER DESCRIPTIONS

The contents of the Time of Day Registers can be either in binary or BCD format. They are relatively straight-forward, but are detailed here for completeness. The address map of these registers is shown below:

Addr	Function	Range
0	Seconds (time)	0-59
1	Seconds (alarm)	0-59
2	Minutes (time)	0-59
3	Minutes (alarm)	0-59
4	Hours (time)	0-11, 12 Hr Mode
4	Hours (time)	0-23, 24 Hr Mode
5	Hours (alarm)	0-23
6	Day of Week	1-7
7	Date of Month	1-31
8	Month	1-12
9	Year	0-99

Address 0 - Seconds:
The range of this register is 0-59 in BCD Mode and 0-3Bh in Binary Mode.

Address 1 - Seconds Alarm:
The range of this register is 0-59 in BCD Mode and 0-3Bh in Binary Mode.

Address 2 - Minutes:
The range of this register is 0-59 in BCD Mode and 0-3Bh in Binary Mode.

Address 3 - Minutes Alarm:
The range of this register is 0-59 in BCD Mode and 0-3Bh in Binary Mode.

Address 4 - Hours:
The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01h-0Ch	Binary	AM
81h-8Ch	Binary	PM

Address 5 - Hours Alarm:
The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01h-0Ch	Binary	AM
81h-8Ch	Binary	PM

Address 6 - Day of Week:
The range of this register is 1-7 in BCD Mode and 1-7h in Binary Mode.

Address 7 - Date:
The range of this register is 1-31 in BCD Mode and 1-1Fh in Binary Mode.

Address 8 - Month:
The range of this register is 1-12 in BCD Mode and 1-0Ch in Binary Mode.

Address 9 - Year:
The range of this register is 0-99 in BCD Mode and 0-63h in Binary Mode.

RTC CONTROL REGISTER DESCRIPTIONS

The VL82C113/VL82C113A has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Addr	Function	Type
10	RTC Register A	R/W
11	RTC Register B	R/W
12	RTC Register C	R-O
13	RTC Register D	R-O
14-63	User RAM (Standby)	R/W

Register A Description

This register contains control bits for the selection of periodic interrupt, input divisor, and the update-in-progress (UIP) status bit. The bits in the register are defined as follows:

Bit	Description	Abbr
0	Rate Select Bit 0	RS0
1	Rate Select Bit 1	RS1
2	Rate Select Bit 2	RS2
3	Rate Select Bit 3	RS3
4	Divisor Bit 0	DV0
5	Divisor bit 1	DV1
6	Divisor bit 2	DV2
7	Update-in-Progress	UIP

Bits 0-3 RS0-RS3 - Rate Selection: These bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate a periodic interrupt. These four bits are read/write bits which are not affected by reset. The periodic interrupt rate that results from the selection of various tap values is as follows:

RS Value	Periodic Interrupt Rate	
0	None	
1	3.90625	ms
2	7.8125	ms
3	122.070	µs
4	244.141	µs
5	488.281	µs
6	976.562	µs
7	1.953125	ms
8	3.90625	ms
9	7.8125	ms
0Ah	15.625	ms
0Bh	31.25	ms
0Ch	62.5	ms
0Dh	125	ms
0Eh	250	ms
0Fh	500	ms

Bits 4-6 DV0-DV2 - Divisor: These divisor selection bits are fixed to provide for only a five-state divider chain, which would be used with a 32 kHz external crystal. Only bit 6 of this register can be changed allowing control of the reset for the divisor chain. When the divider reset is removed, the first update cycle begins one-half second later. These bits are not affected by power-on reset (external pin).

DV Value	Condition
2	Operation Mode, divider running
6	Reset Mode, divider in reset state

Bit 7 UIP - Update-In-Progress: This bit is a status flag that may be monitored by the program. When UIP is a 1, the update cycle is in progress or will soon begin. When UIP is a 0, the update cycle is not in progress and will not be for at least 244 µs. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is 0. The UIP bit is a read-only bit, and is not affected by reset. Writing the SET bit in Register B to a 1 will inhibit any update cycle and then clear the UIP status bit.

Register B Description

Register B contains command bits to control various modes of operations and interrupt enables for the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Daylight Savings Enable	DSE
1	24/12-Hour Mode	24/12
2	Data Mode (Binary or BCD)	DM
3	Reserved	
4	Update-End Interrupt Enable	UIE
5	Alarm Interrupt Enable	AIE
6	Periodic Interrupt Enable	PIE
7	Set Command	SET

Bit 0 DSE - Daylight Savings Enable: A read/write bit which allows the program to enable two special updates (when DSE is 1). On the last Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a 0. DSE is not changed by any internal operations or reset.

Bit 1 24/12 - 24/12-Hour Mode: This control bit establishes the format of the hours bytes as either in 24-Hour Mode (1) or in 12-Hour Mode (0). This is a read/write bit, which is affected only by software.

Bit 2 DM - Data Mode: This bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or reset. A 1 in DM signifies binary data, while a 0 in specifies BCD data.

Bit 3 Reserved: This bit is unused in this version of the RTC.

Bit 4 UIE - Update-End Interrupt Enable: A read/write bit which enables the update-end flag (UF) bit in Register C to assert an –RTCIRQ. The RSTDRV pin being asserted or the SET bit going high clears the UIE bit.

Bit 5 AIE - Alarm Interrupt Enable: This bit is a read/write bit which when set to a 1 permits the alarm flag (AF) bit in Register C to assert an –RTCIRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of 11XXXXXXb). When the AIE bit is a 0, the AF bit does not initiate an –RTCIRQ signal. The RSTDRV pin clears AIE to 0. The internal functions do not affect the AIE bit.

Bit 6 PIE - Periodic Interrupt Enable: This bit is a read/write bit which allows the periodic-interrupt flag (PF) bit in Register C to cause the –RTCIRQ pin to be driven low. A program writes a 1 to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3-RS0 bits in Register A. A 0 in PIE blocks –RTCIRQ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal functions, but is cleared to 0 by a reset.

Bit 7 SET - Set Command: When this bit is a 0, the update cycle functions normally by advancing the counts once-per-second. When written to a 1, any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not modified by reset or internal functions.

Register C Description

Register C contains status information about interrupts and internal operation of the real-time clock. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Reserved, Read as 0	
1	Reserved, Read as 0	
2	Reserved, Read as 0	
3	Reserved, Read as 0	
4	Update-Ended Flag	UF
5	Alarm Interrupt Flag	AF
6	Periodic Interrupt Flag	PF
7	–RTCIRQ Pending Flag	IRQF

Bits 0-3 Reserved: These bits are read as 0s and cannot be written.

Bit 4 UF - Update-Ended Interrupt Flag: The UF bit is set after each update cycle. When the UIE bit is a 1, the 1 in UF causes the IRQF bit to be a 1, asserting –RTCIRQ. UF is cleared by a Register C read or a reset.

Bit 5 AF - Alarm Interrupt Flag: A 1 indicates that the current time has matched the alarm time. A 1 also causes the –RTCIRQ pin to go low, and a 1 to appear in the IRQF bit, when the AIE bit also is a 1. A reset or a read of Register C clears AF.

Bit 6 PF - Periodic Interrupt Flag: This a read-only bit which is set to a 1 when a particular edge is detected on the selected tap of the divider chain. The RS3-RS0 bits establish the periodic rate. PF is set to a 1 independent of the state of the PIE bit. PF being a 1, initiates an –RTCIRQ signal and sets the IRQF bit when PIE is also a 1. The PF bit is cleared by a reset or a software read of Register C.

Bit 7 IRQF - Interrupt Request Flag: IRQF is set to a 1 when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

The logic can be expressed in equation form as:

IRQF = PF • PIE + AF • AIE + UF • UIE

Any time the IRQF bit is a 1, the –RTCIRQ pin is asserted. All flag bits are cleared after Register C is read by the program or when the RSTDRV pin is asserted.

Register D Description
This register contains a bit that indicates the status of the on-chip standby RAM. The contents of the registers are described as the following:

Bit	Description	Abbr
0	Reserved, Read as 0	
1	Reserved, Read as 0	
2	Reserved, Read as 0	
3	Reserved, Read as 0	
4	Reserved, Read as 0	
5	Reserved, Read as 0	
6	Reserved, Read as 0	
7	Valid RAM Data & Time	VRT

Bits 0-6 Reserved: These bits are read as 0s and cannot be written.

Bit 7 VRT - Valid RAM Data and Time: This bit indicates the condition of the contents of the RAM, provided the power-sense (PS) pin is satisfactorily connected. A 0 appears in the VRT bit when the PS pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read-only bit which is not modified by the reset pin. The VRT bit can only be set by reading Register D.

RTC CMOS STANDBY RAM DESCRIPTION

In addition to the 50 dedicated general purpose RAM bytes that are dedicated within the RTC, the VL82C113 provides an additional 64 bytes of battery-backed RAM for general purpose uses. They can be used by the system BIOS or user program, and are available during the RTC update cycle.

GENERAL OPERATION NOTES

Set Operation

Before initializing the internal registers, the SET bit in Register B should be set to a 1 to prevent time/calendar updates from occurring. The program initializes the ten locations in the selected format (binary or BCD), then indicates the format in the Data Mode (DM) bit of Register B. All ten time, calendar, and alarm bytes must use the same Data Mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized, the real-time clock makes all updates in the selected Data Mode. The Data Mode cannot be changed without re-initializing the ten data bytes.

24/12-Hour Modes

The 24/12 bit in Register B establishes whether the hour locations represent 0-11 or 0-23. The 24/12 bit cannot be changed without re-initializing the hour locations. When the 12-Hour Mode is selected, the high-order bit of the hours byte represents PM when it is set a 1.

Update Operation

The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the ten bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the ten bytes are read at this time, the data outputs are undefined. The update lock-out time is 1948 µs for the 32.768 kHz time base. The update cycle section shows how to accommodate the update cycle in the processor program.

Alarm Operation

The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any byte from 0C0h-0FFh. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Interrupts

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from one-per-second to one-a-day. The periodic interrupt may be selected for rates from one-half second to 30.517 µs. The update-ended interrupt may be used to indicate to the program that an update cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A 0 in the interrupt-enable bit prohibits the –RTCIRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the –RTCIRQ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, a flag bit is set to a 1 in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

Divider Control

The divider control bits are fixed for only 32.768 kHz operation. The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one-half second later. The divider control bits are also used to facilitate testing the VL82C113/VL82C113A.

Square Wave Output Selection

This version of the VL82C113/VL82C113A does not support the square wave output function.

Periodic Interrupt Selection

The periodic interrupt allows the –RTCIRQ pin to be triggered from once every 500 ms to once every 30.517 µs. The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Update Cycle

The VL82C113/VL82C113A executes an update cycle one-per-second, assuming one of the proper time bases is in place, the DV0-DV2 divider is not clear, and the SET bit in Register B is clear. The SET bit in the 1 state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 32.768 kHz time base update cycle takes 1984 µs, during which, the time, calendar, and alarm bytes are not accessible by the processor program. The 146818 protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete, the output will be undefined. The update-in-progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating non-availability during update are usable by the program. In discussing the three methods it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes high, the update cycle begins 244 µs later. Therefore, if a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. If a 1 is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C.

To properly setup the internal counters for daylight savings time operation, the user must set the time at least two seconds before the roll-over will occur. Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

Power-Down Mode

The passive components that are critical for low-power operation are shown in Figure 4.

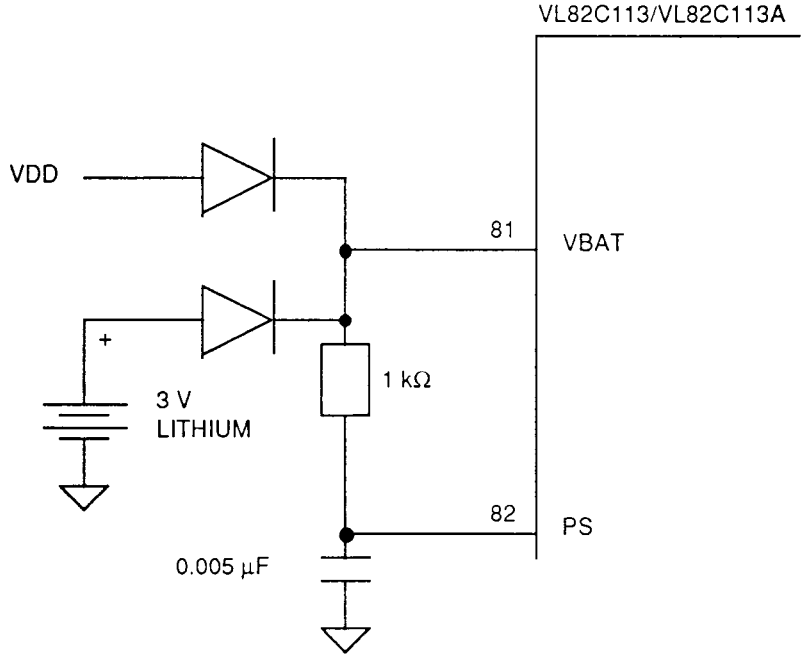
Figure 4 is an example only. A NiCad battery can be used also. The power-sense signal is used to reset the state of of the valid RAM and time bit (VRT) and clear all internal RAM. This input must be asserted after power is applied to the RTC to set the state of the VRT bit properly. With a power consumption target specification of 5 µA, and a lithium battery with a capacity of 100 mA-Hr, time will be properly kept for approximately 2.25 years.

BOARD TESTING FEATURES

The VL82C113/VL82C113A is designed to make system board testing as easy as possible. When the –CE/–CS0/–TRI input is held low at POR (power-on reset, i.e., the falling edge of RSTDRV), it causes all pins on the VL82C113/VL82C113A to go to a high impedance state. This can be used to electrically isolate the VL82C113/VL82C113A so that other components in the system may be tested.

Exit from the high impedance state is accomplished by a normal reset with RSTDRV.

FIGURE 4. LOW-POWER OPERATION CIRCUIT



AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
I/O Read/Write Timing					
t5	Command Pulse Width	125		ns	
tSU6	Write Data Setup	60		ns	
tH7	Write Data Hold	20		ns	
tD8	Read Data Delay	0	130	ns	CL = 200 pF
tH9	Read Data Hold	5	60	ns	CL = 50 pF
WC	Write Cycle	280		ns	
RC	Read Cycle	280		ns	
tSU1	Address Valid to –EALE Rising	23		ns	
tSA	SA Valid from –EALE Rising		35	ns	CL = 200 pF
tLA	Address Valid to LA Valid		36	ns	CL = 200 pF
Master Mode Timing					
tAM	A bus Valid from SA/LA Input (Master Mode)		15	ns	CL = 200 pF
Real-Time Clock Timing					
tPSPW	Power-Sense Pulse Width	2		µs	
tPSD	Power-Sense Delay	2		µs	
tVRTD	VRT Bit Delay		2	µs	

FIGURE 5. WRITE CYCLE

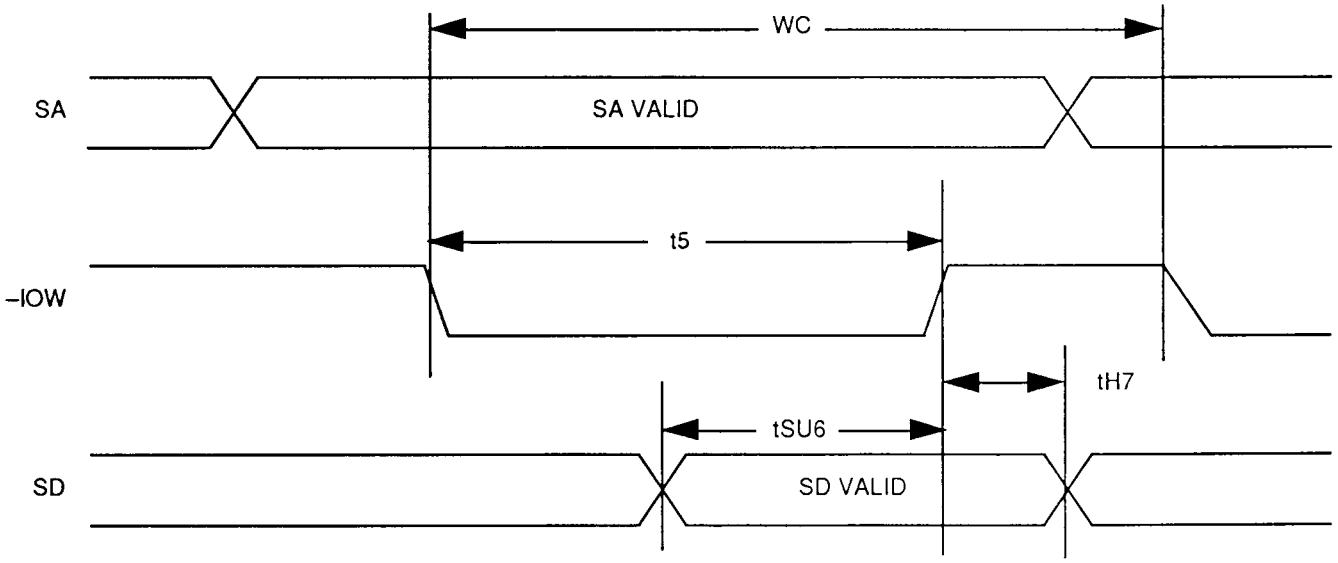


FIGURE 5A. WRITE CYCLE

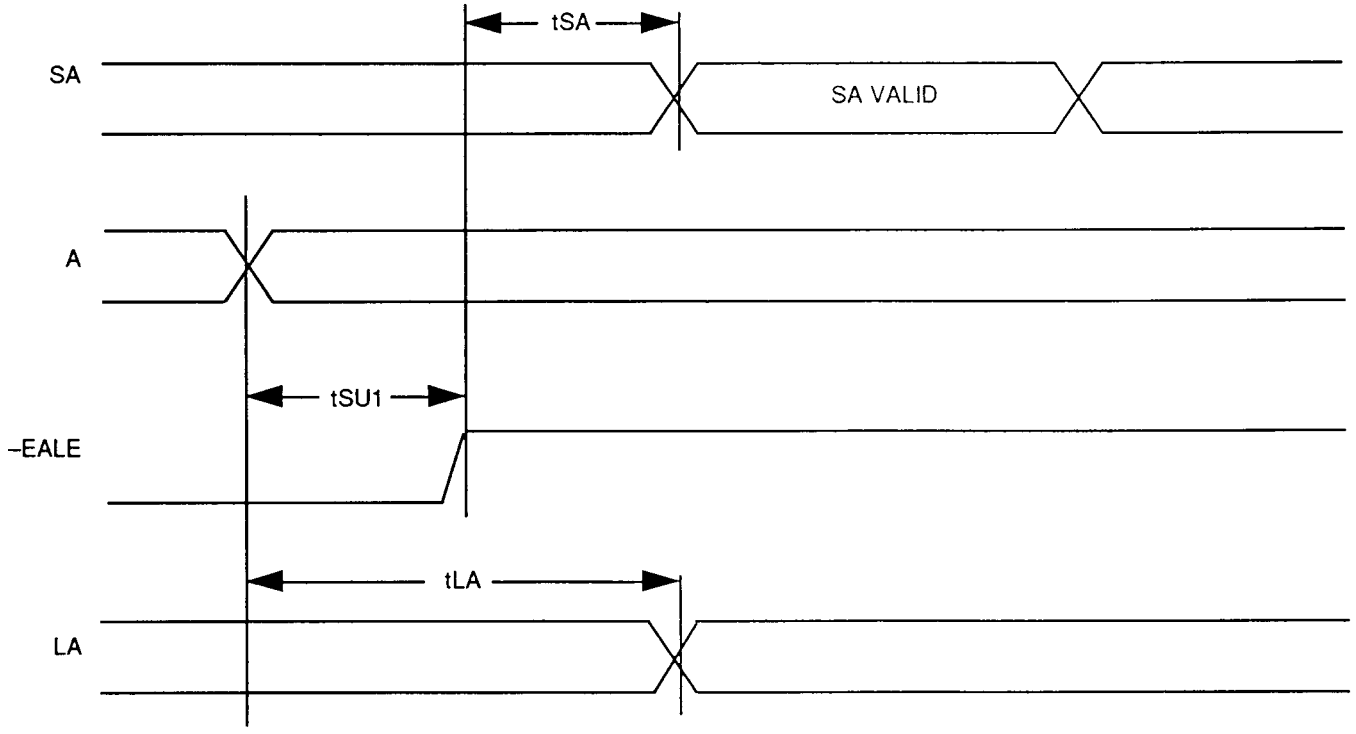


FIGURE 6. READ CYCLE

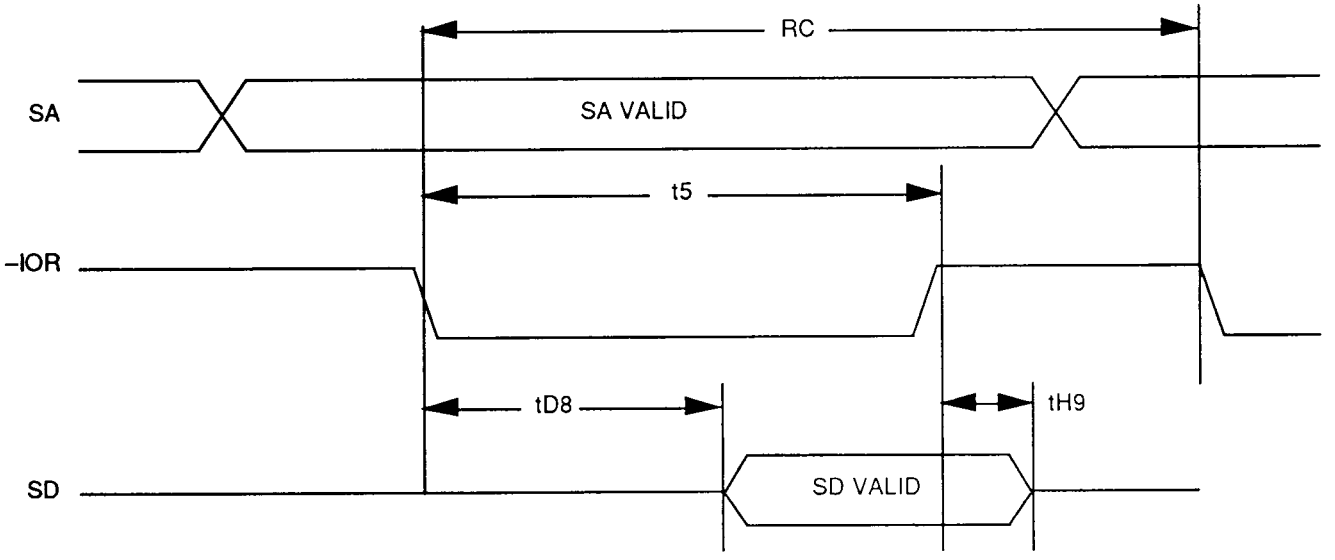


FIGURE 7. MASTER MODE BUS TIMING

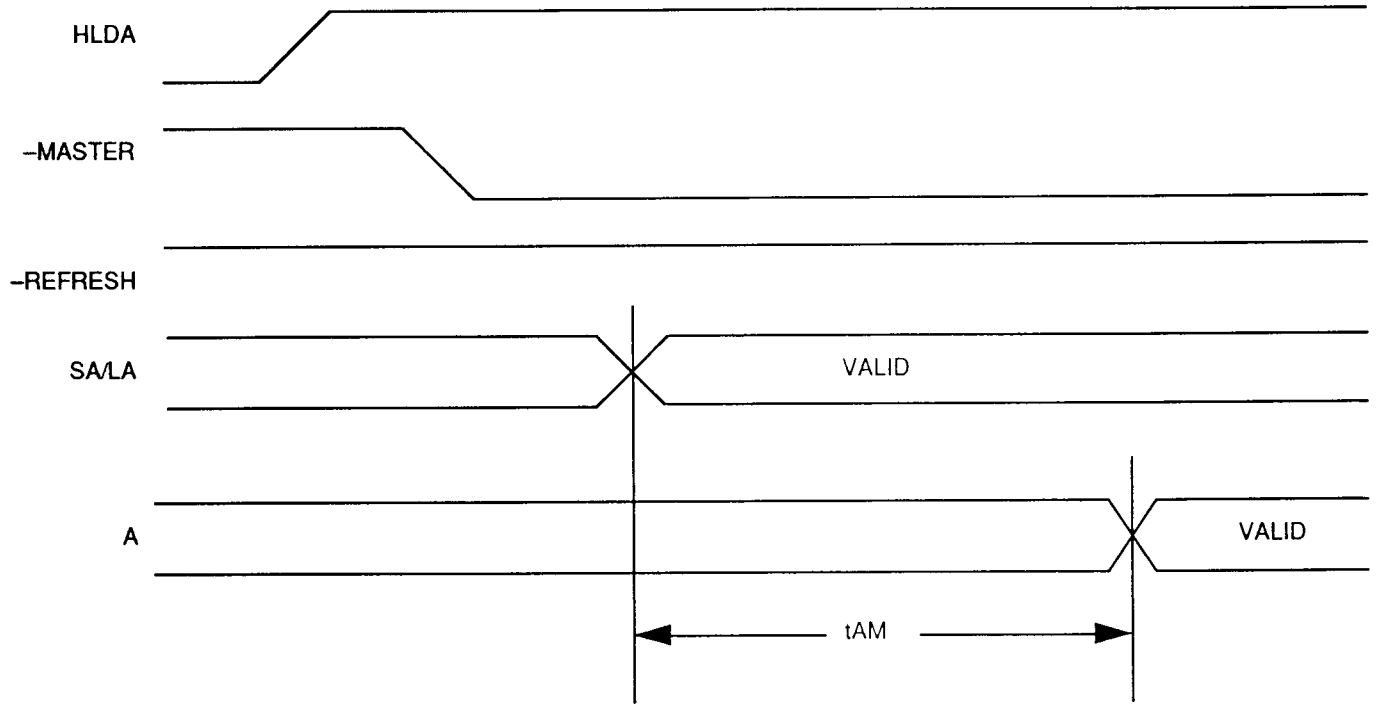
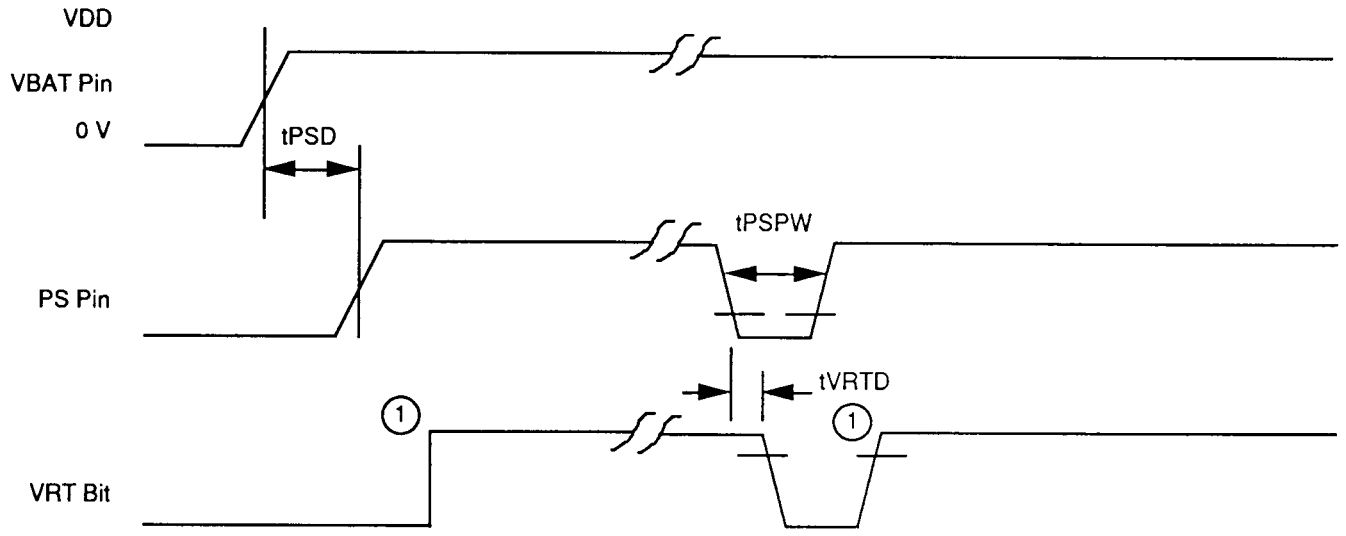
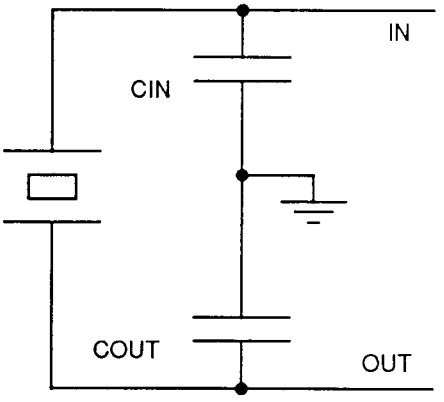


FIGURE 8. REAL-TIME CLOCK TIMING



(1) The VRT bit is set a "1" by reading Register D. The VRT bit can only be cleared by pulling the PS pin low (see REGISTER D($0D)).

FIGURE 9. CRYSTAL OSCILLATOR CONFIGURATION



Notes: Frequency = 32.768 kHz
CIN = COUT = 10-22 pF
CIN may be a trimmer for precision timekeeping applications.

Recommended Crystal Parameters:
Rs (max) ≤ 40 kΩ
Co (max) ≤ 1.7 pF
Ci (max) ≤ 12.5 pF
Parallel Resonance

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature –10°C to +70°C

Storage Temperature –65°C to +150°C

Supply Voltage to Ground Potential –0.5 V to VDD + 0.3 V

Applied Output Voltage –0.5 V to VDD + 0.3 V

Applied Input Voltage -0.5 V to 7.0 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
VIL	Input Low Voltage	–0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0 2.4	VDD + 0.5 VDD + 0.5	V V	TTL Level Inputs, Note 1 TTL Level Inputs, Note 2
VOL	Output Low Voltage		0.4 0.4 0.4 0.4	V V V V	IOL = 4.0 mA, Note 3A IOL = 8.0 mA, Note 4A IOL = 12.0 mA, Note 5 IOL = 24.0 mA, Note 6
VOH	Output High Voltage	2.4 2.4 2.4		V V V	IOH = 0.8 mA, Note 3B IOH = 1.4 mA, Note 4B IOH = 2.4 mA, Note 6
IIH	Input High Current		10	µA	VIN = VDD, Note 7
IIL	Input Low Current	–10 –500	50	µA µA	VIN = VSS + 0.2 V, Note 8 VIN = 0.8 V, Note 9
ILOL	Three-state Leakage Current	–50	50	µA µA	VOUT = VSS + 0.2 V, Note 10 VOUT = VDD, Note 11
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
IDD	Operating Supply Current		40	mA	
IBAT	Supply Current, Standby Mode		5.0 5.0 50.0	µA µA µA	VBAT = 2.4 V VBAT = 3.0 V VBAT = 5.0 V
IDDQ	Static Supply Current		5.0	mA	

(Notes on next page.)

DC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Notes:

1. Pins: –REFRESH, SA0, –SBHE, –MASTER, –EALE, –BHE, HLDA, OSCI, KRSEL, KKSW, KCM, KI2/–TRI, –IOW, –IOR, SA19-SA1, A23-A1, LA23-LA17, SD7-SD0, KIRQ, –RTCIRQ, KI3, KI5.
2. Pins: KHSE, KSRE, KDAT, KCLK, RSTDRV, PS.

3A. Pins: KIRQ, MIRQ, KI5, KI3.

3B. Pins: KIRQ, MIRQ, KI5, KI3, –RTCIRQ.

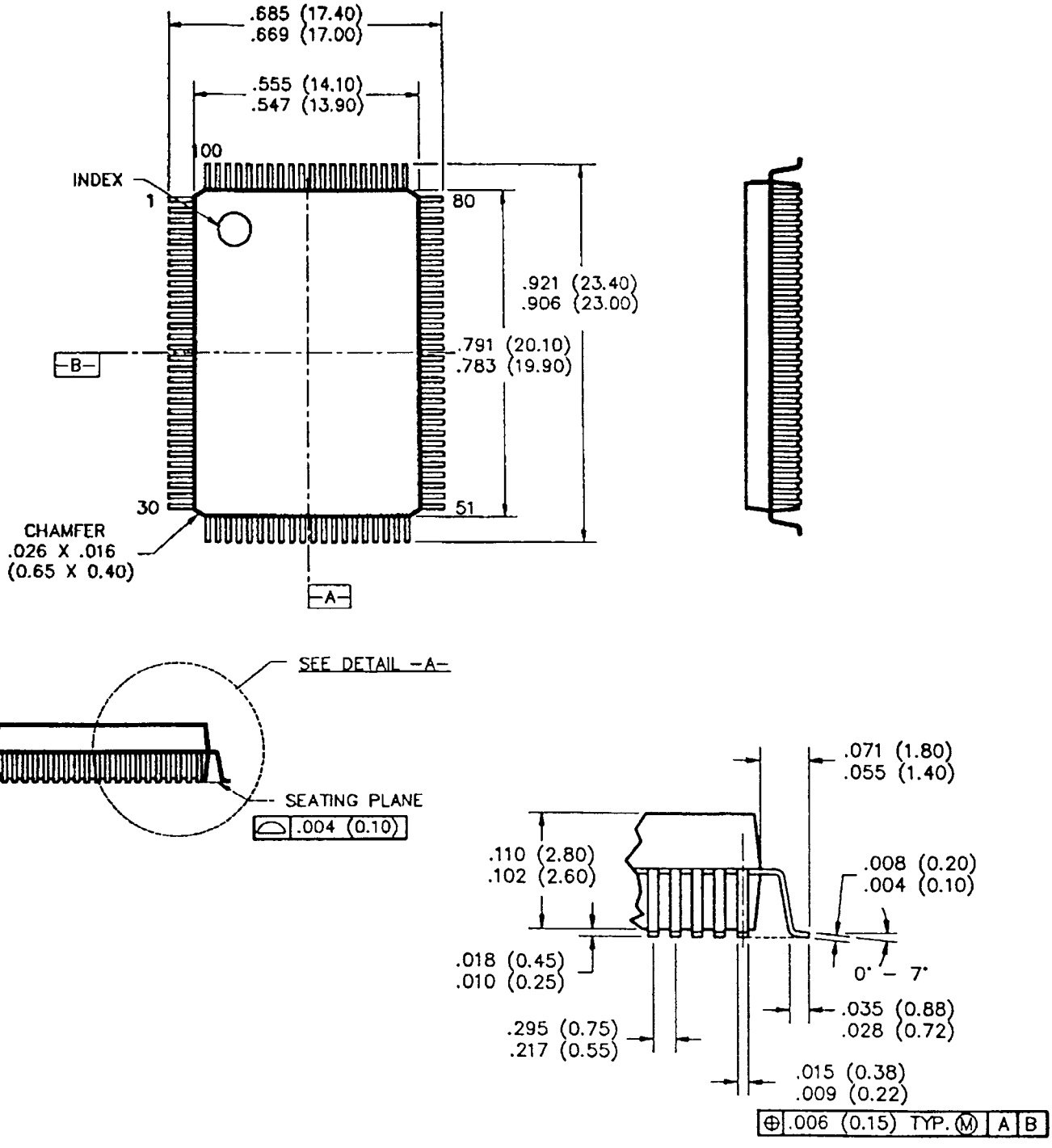
4A. Pins: A23-A1, –BHE.

4B. Pins: A23-A1, –BHE, KHSE/MDAT (PC/AT Mode only), KSRE/MCLK (PC/AT Mode Only).

5. Pins: KHSE, –RTCIRQ, KSRE, KDAT, KCLK.
6. Pins: –SBHE, SA19-SA1, LA23-LA17, SD7-SD0.
7. Pins: –REFRESH, SA0, –MASTER, –EALE, HLDA, OSCI, KRSEL, KKSW, KCM, KI2/–TRI, PS, RSTDRV, –IOW, –IOR.
8. Pins: –REFRESH, SA0, –MASTER, –EALE, HLDA, OSCI, KRSEL, PS, RSTDRV, –IOW, –IOR.
9. Pins: KIRQ, KKSW, KCM, KI5, KI3, KI2/–TRI.
10. Pins: SA19-SA1, –SBHE, LA23-LA17, A23-A1, SD7-SD0, KHSE/MDAT, KSRE/MCLK, MIRQ, KDAT, KCLK, –BHE, XTALIN, –RTCIRQ.
11. Pins: SA19-SA1, –SBHE, LA23-LA17, A23-A1, –BHE, KIRQ, KI5, KI3, SD7-SD0, –RTCIRQ, MIRQ, KHSE/MDAT, KSRE/MCLK, KDAT, KCLK.

PACKAGE OUTLINE

100-PIN METRIC (PLASTIC) QUAD FLAT PACK



DETAIL -A-

Notes: 1. Controlling dimension is MM.
2. Dimensions are shown in inches (millimeters).

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