VLSI TECHNOLOGY, INC.

ADVANCE INFORMATION

VL82C107

SCAMP™ COMBINATION I/O

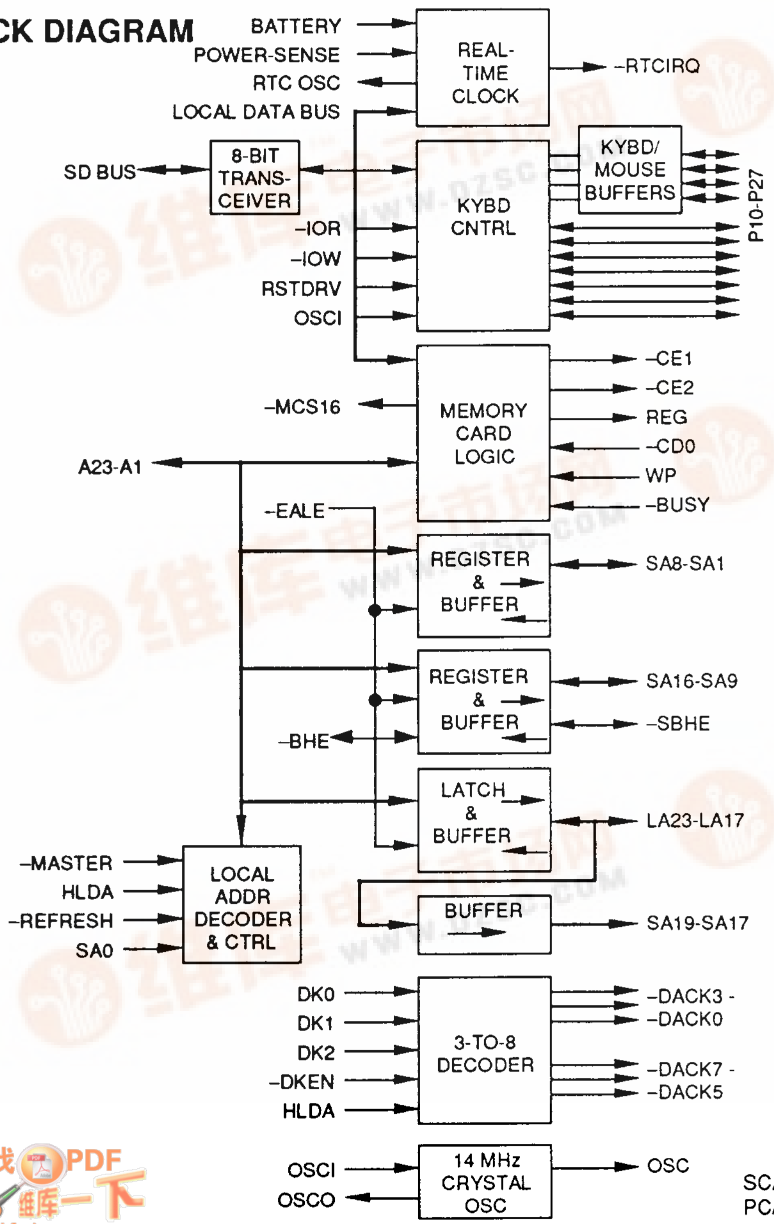
FEATURES

- Integrated peripheral controller for SCAMP™ VL82C310/VL82C311 Single Chip PC/AT® Controllers
- 146818A-compatible real-time clock
- 128 additional bytes of battery-backed CMOS RAM
- AT-compatible keyboard controller with integrated PS/2® mouse support
- SCAMP-compatible processor to ISA bus address registers/latches and buffers
- DMA acknowledge decoder
- PC memory card interface
- 8- or 16-bit PC memory card support
- Optional support for IDE, floppy, and VL16C452 chip selects
- XIP (Execute-In-Place) provisions
- Integrated oscillator for 14.3181 MHz clock
- 1.5-micron CMOS in a 128-lead MQFP

DESCRIPTION

The VL82C107 SCAMP Combination I/O chip, when used with other VLSI SCAMP chips, allows designers to implement a very cost-effective minimum chip count motherboard. This chip combines a keyboard controller, a real-time clock with the address registers/latches and buffers, and DMA acknowledge decoders which are normally required in SCAMP-based systems. Additionally, the VL82C107 contains the circuitry necessary to interface PC memory cards to the system or provide the chip select and control signals for an external VL16C552 UART I/O device, FDC and IDE interface.

BLOCK DIAGRAM



ORDER INFORMATION

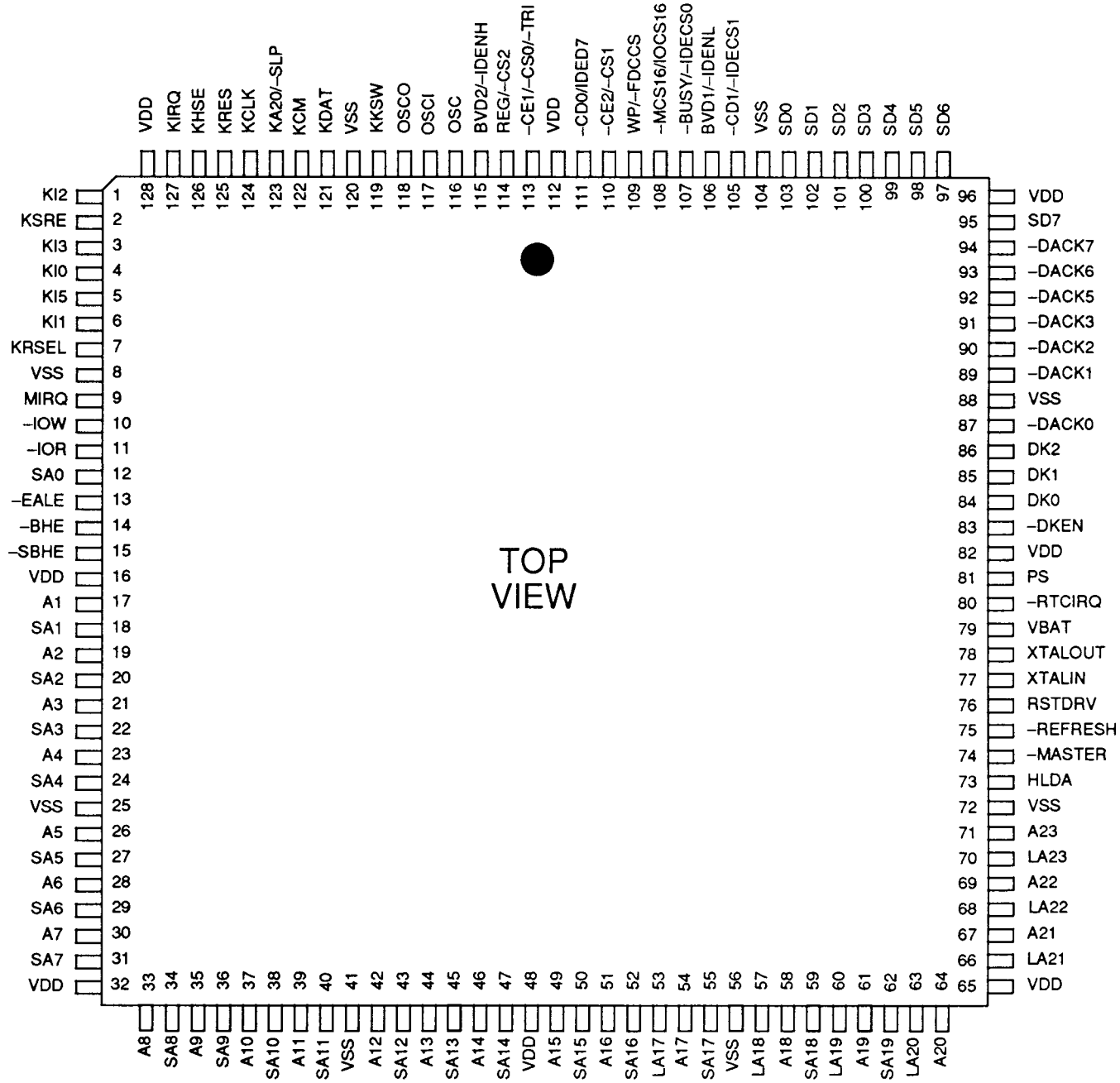
Part Number	Package
VL82C107-FC	Metric Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

SCAMP is a trademark of VLSI Technology, Inc.
PC/AT and PS2 are registered trademarks of IBM Corp.

PIN DIAGRAM

VL82C107



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS			
HLDA	73	I-TTL	Hold Acknowledge - This is the hold acknowledge pin directly from the CPU. It is used to control direction on address and to enable the –DACK decoder.
A23-A1	71, 69, 67, 64, 61, 58, 54, 51, 49, 46, 44, 42, 39, 37, 35, 33, 30, 28, 26, 23, 21, 19, 17	IO-TTL (8 mA)	Address bus bits 23 through 21 - When HLDA is high, –MASTER is low, and –REFRESH is high, these signals are outputs. They are inputs at all other times.
–BHE	14	IO-TTL (8 mA)	Byte High Enable - This pin is an output during Master Mode non-refresh cycles and it tracks the –SBHE input. It is an input at all other times.
ISA BUS SIGNALS			
RSTDRV	76	I-TTL	System Reset - This active high input is system reset that is generated from the POWERGOOD input.
–IOR	11	I-TTL	I/O Read command.
–IOW	10	I-TTL	I/O Write command.
–MASTER	74	I-TTL	Master - This active low input is used by an external device to disable the internal DMA controllers and get access to the system bus. When asserted, it indicates that an external Bus Master has control of the bus.
–REFRESH	75	I-TTL	Refresh - This active low input signal is pulled low whenever a refresh cycle is initiated.
LA23-LA17*	70, 68, 66, 63, 60, 57, 53	IO-TTL (12/24 mA)	Latchable Address bus bits 23 through 17 - This bus is an input when HLDA is high, –REFRESH is high, and –MASTER is low. It is an output bus driven by the values from the A bus when HLDA is low and –REFRESH is high. It is three-stated when HLDA is high and –REFRESH is low. The LA bus is latched internally with the –EALE input. The output drive strength of these pins is selectable between 12 mA and 24 mA. This is set by the state of the –CE2/–CS1 pin at power-on reset; if –CE2/–CS1 is sampled high on the falling edge of RSTDRV, these are 24 mA outputs. If –CE2/–CS1 is sampled low, these are 12 mA outputs.
SA19-SA9*	62, 59, 55, 52, 50, 47, 45, 43, 40 38, 36	IO-TTL (12/24 mA)	System Address bus bits 19 through 9 - This bus is an input when HLDA is high, –REFRESH is high, and –MASTER is low. It is an output bus driven by the values from the A bus when HLDA is low and –REFRESH is high. It is three-stated when HLDA is high and –REFRESH is low. The SA19-SA9 bus is registered internally with the –EALE input. The output drive strength of these pins is selectable similarly to LA23-LA17.
SA8-SA1*	34, 31, 29, 27, 24, 22 20, 18	IO-TTL (12/24 mA)	System Address bus bits 8 through 1 - This bus is an input when HLDA is high, –REFRESH is high, and –MASTER is low. It is an output bus driven by the values from the A bus at all other times. The SA8-SA1 bus is registered internally with the –EALE input. The output drive strength of these pins is selectable similarly to LA23-LA17.
SA0	12	I-TTL	System Address bus least significant bit (LSB) - This is an input at all times and is used in the address decode of internal peripheral registers/ports.

*The output drive of LA-23-LA17, SA19-SA1 and –SBHE is always 24 mA and –CE2/–CS1 is an output only for parts that were manufactured before January 1992.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–SBHE*	15	IO-TTL (12/24 mA)	System Byte High Enable - This pin is controlled the same way as the SA bus. –SBHE is registered internally with the –EALE input. The output drive strength of this pin is selectable similarly to LA23-LA17.
–DACK7 - –DACK5 –DACK3 - –DACK0	94-92, 91-89, 87	O (8 mA)	DMA Acknowledge - These active low outputs are the acknowledge signals for the corresponding DMA requests.
OSC	116	O (24 mA)	Oscillator - The buffered output of the internal 14.318 MHz oscillator.
–MCS16/ –IOCS16	108	O (24 mA)	Memory Chip Select 16 bit - When the VL82C107 is configured with a PC memory card interface, this signal is used as the memory chip select. I/O Chip Select 16 bit - When the VL82C107 is configured for Chip Select Mode and the IDE interface is enabled, this signal is used as I/O chip select.

KEYBOARD CONTROLLER SIGNALS

			Keyboard Controller Mode			
			PC/AT Mode KBDCTRL = 1		PS/2 Mode KBDCTRL = 0	
KCLK	124	IO-TODS	T0/-P26	Kbd Clock	T0/-P26	Kbd Clock
KDAT	121	IO-TODS	T1/P27	Kbd Data	P10/-P27	Kbd Data
KCM	122	I-TPU	P16	Color Input	P16	Input
KKSW	119	I-TPU	P17	Key Switch	P17	Input
KA20/–SLP	123	IO-TPU (4 mA)	P21	A20 Gate Out	P21	A20 Gate Out This signal is configured as the –SLP input if KRES is sampled low on the falling edge of RSTDRV. –SLP is used to disable the clock to the keyboard controller to minimize power consumption. If KRES is sampled high on the falling edge of RSTDRV, this signal is configured as the KA20 keyboard output. When configured as the –SLP input, the HSLP bit in the KBDCTRL Register must be set in order for the operation of the –SLP pin to be enabled.
KRES	125	IO-TPU (4 mA)	P20	Reset Command	P20	Reset Command This signal is sampled on the falling edge of RSTDRV. If this input is low it will remain an input and not be driven. If sampled high, this signal will be the KRES output of the keyboard controller.
KHSE	126	IO-TODS (12 mA)	P22	High Speed	P11/-P22	Mouse Data
KSRE	2	IO-TODS (12 mA)	P23	Shadow RAM	T1/-P23	Mouse Clock
KIRQ	127	IO-TPU	P24	Kbd Int Req	P24	Kbd Int Req This pin is sampled on the high-to-low transition of RSTDRV. If KIRQ is low, the keyboard function within the VL82C107 is disabled. If KIRQ is high, the keyboard function is enabled. This pin is internally pulled up to VDD.
MIRQ	9	O	P25	Output	P25	Mouse Int Req
KRSEL	7	I-TPU	P14	RAM Select	P14	Input

*The output drive of LA-23-LA17, SA19-SA1 and –SBHE is always 24 mA and –CE2/–CS1 is an output only for parts that were manufactured before January 1992.

SIGNAL DESCRIPTION (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description			
KI0	4	IO-TPU (8 mA)	P10	Input	MISCOUT1	Output
KI1	6	IO-TPU (8 mA)	P11	Input	MISCOUT2	Output
KI2	1	I-TPU	P12	Input	P12	Fuse Input
KI3	3	I-TPU	P13	Input	P13	Input
KI5	5	I-TPU	P15	Input	P15	Input
SD DATA BUS						
SD7-SD0	95, 97-103	IO-TTL (24 mA)	System Data bus bits 7 through 0 - This bus connects directly to the slots. It is used to transfer data to/from the low byte of local and system devices.			
PERIPHERAL INTERFACE SIGNALS						
–DKEN	83	I-TTL	Decoder Enable - An active low input which enables an internal 3-to-8 decoder for the generation of the DMA acknowledge signals from DK2-DK0. The following table details the relationship between DK2-DK0, –DKEN, and HLDA.			

–DKEN	DK2-DK0	HLDA	Active DMA Acknowledge
X	X	L	None
H	X	H	None
L	0	H	None
L	1	H	–DACK0
L	2	H	–DACK1
L	3	H	–DACK2
L	4	H	–DACK3
L	5	H	–DACK5
L	6	H	–DACK6
L	7	H	–DACK7

DK0	84	I-TTL	This is an input signal which along with DK1 and DK2 represents the encoded channel number being serviced during DMA acknowledge cycles.
DK1	85	I-TTL	This is an input signal which along with DK0 and DK2 represents the encoded channel number being serviced during DMA acknowledge cycles.
DK2	86	I-TTL	This is an input signal which along with DK0 and DK1 represents the encoded channel number being serviced during DMA acknowledge cycles.
XTALIN	77	I-CMOS	Internal oscillator input for real-time clock crystal. Requires a 32.768 KHz external crystal or stand-alone oscillator.
XTALOUT	78	O	Internal oscillator output for real-time clock crystal. See XTALIN. This pin is a "no connect" when an external oscillator is used.
PS	81	I-TST	Power-Sense - An active high input used to reset the status of the valid RAM and time (VRT) bit. This bit is used to indicate that the power has failed, and that the contents of the real-time clock may not be valid. This pin is connected to an external RC network.
VBAT	79	I-TTL	Connected to the real-time clock's hold-up battery, between 2.4 and 5 volts.
–RTCIRQ	80	IO-TODPU (12 mA)	Real-Time Clock Interrupt Request output (active low) - This pin is an input when RSTDRV is high. It is sampled on the high-to-low transition of RSTDRV. If –RTCIRQ is low when sampled, the real-time clock function within the VL82C107 is disabled. If –RTCIRQ is high, the RTC is enabled. Open drain output.
OSCI	117	I-CMOS	Internal oscillator input for the 14.3181 MHz crystal.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
OSCO	118	O	Internal oscillator output for the 14.3181 MHz crystal.
ADDRESS BUS CONTROL SIGNAL			
–EALE	13	I-TTL	Early Address Latch Enable - An active low pulse which is generated at the beginning of any bus cycle initiated from the CPU which is not directed at on-board DRAM.
PC MEMORY CARD INTERFACE SIGNALS			
–CE1/–CS0/ –TRI	113	IO-TPU (8 mA)	Card Enable 1 - When in PC Memory Card Mode, this signal is the memory card enable 1 output. Chip Select 0 - When in Chip Select Mode, this signal is chip select 0. Three-State Mode - This signal is sampled on the high-to-low transition of the RSTDRV signal. If sampled low, the VL82C107 enters the three-state mode.
–CE2/–CS1*	110	I/O (8 mA)	Card Enable 2 - When in PC Memory Card Mode, this signal is the memory card enable 2 output. Chip Select 1 - When in Chip Select Mode, it is the chip select 1 signal. –CE2/–CS1 is sampled on the falling edge of RSTDRV. If sampled low, the output drive strength of –SBHE, SA19-SA1, and LA23-LA17 will be set to 12 mA. If sampled high, the outputs will be set to 24 mA drive. This signal has an internal pull-up resistor so that if unconnected, the output drives will default to 24 mA.
REG/–CS2	114	O (8 mA)	Register Select - When in PC Memory Card Mode, this is the register select output signal. Chip Select 2 - When in Chip Select Mode, it is the chip select 2 signal.
–CD0/IDED7	111	IO-TPU (24 mA)	Card Detect 0 - When in PC Memory Card Mode, this is the card detect 0 input signal. IDE Data bit 7 - In Chip Select Mode, it is the bidirectional IDE data bit 7 signal.
WP/–FDCCS	109	IO-TPU (8 mA)	Write Protect - When in PC Memory Card Mode, this signal is the write protect input. When high, all of the memory area is protected. If any of the memory area is allowed to be written (programmed), WP will be low. Floppy Disk Chip Select - When the VL82C107 is configured in the Chip Select Mode, this pin is an output for the floppy disk chip select.
–BUSY/ –IDECS0	107	IO-TPU (8 mA)	Busy - When in PC Memory Card Mode, this is the active low busy input signal . IDE Chip Select 0 - In Chip Select Mode, it is the (active low) IDE chip select 0 output signal.
–CD1/–IDECS1	105	IO-TPU (8 mA)	Card Detect 1 - When in PC Memory Card Mode, this is the card detect 1 input signal. It is sampled on the falling edge of RSTDRV. If sampled low, the VL82C107 is configured for PC Memory Card Mode. If sampled high, the VL82C107 is configured for Chip Select Mode. IDE Chip Select 1- In Chip Select Mode, it is the active low IDE chip select 1 signal.

*The output drive of LA-23-LA17, SA19-SA1 and –SBHE is always 24 mA and –CE2/–CS1 is an output only for parts that were manufactured before January 1992.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
BVD2/–IDENH	115	IO-TTL (8 mA)	Battery Voltage Detect 2 - When in PC Memory Card Mode, it is the battery voltage detect 2 input. IDE High Data Byte Enable - In Chip Select Mode, it is the IDE high data byte enable output.
BVD1/–IDENL	106	IO-TTL (8 mA)	Battery Voltage Detect 1 - When in PC Memory Card Mode, it is the battery voltage detect 1 input. IDE Low Data Byte Enable - In Chip Select Mode, it is the IDE low data byte enable output.
POWER AND GROUND PINS			
VDD	16, 32, 48, 65, 82, 96, 112, 128	PWR	Power Connection, nominally 5 volts.
VSS	8, 25, 41, 56, 72, 88, 104, 120	GND	Ground Connection, 0 volts.

SIGNAL LEGEND

Signal Code	Signal Type
I-CMOS	CMOS level input
I-TTL	TTL level input
I-TPU	TTL level input with 30k ohm pull-up resistor
I-TST	TTL level Schmitt-trigger input
IO-TTL	TTL level input/output
IO-TOD	TTL level input/output open drain
IO-TODNP	TTL level input/output open drain with 3k ohm NMOS pull-up
IO-TODPU	TTL level input/output open drain with 30k ohm pull-up resistor
IO-TODS	TTL level with open drain output/Schmitt-trigger input
IO-TPU	TTL level input/output with 30k ohm pull-up resistor
O	CMOS and TTL level compatible output
GND	Ground
PWR	Power

GENERAL DESCRIPTION & PROGRAMMER'S MODEL

The VL82C107 SCAMP Combination I/O chip combines a keyboard controller and a real-time clock with the address register/latches, buffers and DMA acknowledge decoders which are normally required in SCAMP-based systems. The VL82C107 additionally contains the circuitry necessary to interface PC memory cards to the system or to provide the chip select and control signals for an external VL16C452 UART I/O device, FDC, and IDE interface. While the VL82C107 has been optimized for use with the VL82C310/VL82C311 SCAMP Controllers, its uses are not restricted to this device combination.

The PC memory card interface, keyboard controller, and real-time clock are enabled/disabled through a combination of hardware and software accessible mechanisms. Software accessible registers are programmed through a series of indexing registers. In this scheme, one register (Index Register) is loaded with an 8-bit value which represents the address of the control/data register located within the VL82C107 which is to be read or written. The second register (Data Register) represents the datapath to the register pointed to by the Index Register. Two pairs of indexed registers are used with the VL82C107 and are extensions of the registers used by the VL82C310/VL82C311 SCAMP Controllers. INDEX1 is located at I/O address E8 hex with its corresponding DATA1 Register being located at I/O address EA hex. INDEX2 is located at EC hex and DATA2 is located at ED hex. These index/data registers are located at the same location within the VL82C310/VL82C311 SCAMP Controllers as they are in the VL82C107. INDEX1, INDEX2, and DATA1 Registers are write-only. DATA2 can be read as well as written. Table 1 details the ISA I/O address for the Index Registers as well as the default addresses for the real-time clock and keyboard controllers.

Default values for these control registers have been selected so as to eliminate the need to change their values in typical system configurations when the VL82C107 is configured for Chip Select Mode of operation.

Table 2 details the PC Memory Card Page Address Register accessible through INDEX1 and DATA1 Registers.

Table 3 shows the bit assignment of each Page Registers.

TABLE 1. ISA I/O ADDRESS MAP

I/O Address	Register Name	Description
0060 Hex	KBDAT	Keyboard Controller Input/Output Buffer
0064 Hex	KBDCTL	Keyboard Controller Status/Command Register
0070 Hex	RTCADD	Real-Time Clock Address Register
0071 Hex	RTCDAT	Real-Time Clock Data Registers
00E8 Hex	INDEX1	Configuration INDEX1 Register
00EA Hex	DATA1	Configuration DATA1 Register
00EC Hex	INDEX2	Configuration INDEX2 Register
00ED Hex	DATA2	Configuration DATA2 Register

TABLE 2. PC MEMORY CARD PAGE REGISTERS

(INDEX1 loc = 00E8, DATA1 loc = 00EA. Write-only register.)

I/O Address	Register Name	Description
30 Hex	PAGE0	6-Bit Match Address for Memory Card Page 0
32 Hex	PAGE1	6-Bit Match Address for Memory Card Page 1
34 Hex	PAGE2	6-Bit Match Address for Memory Card Page 2
36 Hex	PAGE3	6-Bit Match Address for Memory Card Page 3

TABLE 3. PC MEMORY CARD PAGE REGISTERS BIT DEFINITIONS

Register	D7	D6	D5	D4	D3	D2	D1	D0
PAGE0-PAGE3	1	1	SA19	SA18	SA17	SA16	SA15	SA14

Table 4 details the Control, Status, and Configuration Registers for the VL82C107 accessible through INDEX2 and DATA2 Registers.

The following is a detailed listing of the Control, Status, and Configurations Registers bit definitions. Table 5 is a summary of those registers.

Memory Card Status Register (MCSTAT)
Index Register: ECh
Index Address: 1Ah
Data Register: EDh

Bit 0 –BSY - Memory Card Busy (active low): This bit reflects the state of the –BUSY pin which is normally the –BUSY output of the memory card. It is sampled on reads from this register.

Bit 1 –CD - Memory Card Card Detect (active low): This bit is active when both of the debounced –CD0 and –CD1 pins are active low. If active, a memory card is present.

Bit 2 WP - Memory Card Write Protect: This bit reflects the state of the WP pin and is sampled on reads of this register.

Bit 3 REG - Memory Card Register Select: The state of this bit is reflected on the REG output pin.

Bit 4 –EN8 - Memory Card 8-Bit Enable (active low): If set, all memory card accesses will be byte accesses controlled by the –CE1 pin.

Bit 5 BVD1 - Memory Card Battery Voltage Detect 1: This bit reflects the state of the BVD1 output of the memory card which is sampled on reads of this register.

Bit 6 BVD2 - Memory Card Battery Voltage Detect 2: This bit reflects the state of the BVD2 output of the memory card which is sampled on reads of this register.

Bit 7 Reserved: This bit is reserved for possible future use (read as 1). Do not use this bit.

TABLE 4. PC MEMORY CARD PAGE REGISTERS

(INDEX2 loc = 00Ec, DATA1 loc = 00ED.)

I/O Addr	Register Name	Description	Read/Write
1A Hex	MCSTAT	Memory Card Status Register	R/W
0A Hex	MCCTRL	Memory Card Control Register	W-O
1B Hex	RTCLSB	RTC Address Register - Low Byte	R/W
1C Hex	RTCMSB	RTC Address Register - High Byte	R/W
1D Hex	KBDCTRL	Keyboard Controller Control Port	R/W
1E Hex	CSCTRL	IDE/Chip Select Control Port	R/W
1F Hex	REVID	ID/Revision Register	R-O

TABLE 5. CONTROL, STATUS, AND CONFIGURATION REGISTERS BIT DEFINITIONS

Register	D7	D6	D5	D4	D3	D2	D1	D0
MCSTAT	1	BVD2	BVD1	–EN8	REG	WP	–CD	–BSY
MCCTRL	1	1	1	1	ENA3	ENA2	ENA1	ENA0
RTCLSB	A7	A6	A5	A4	A3	A2	A1	RENA
RTCMSB	A15	A14	A13	A12	A11	A10	A9	A8
KBDCTRL	–KISLP	HSLP	RAMEN	MISC1	MISC0	PRV	MODE	SLP
CSCTRL	FDCEN	LPTEN	LPT2	LPT1	COMB	COMA	COMS	IDEN
REVID	0	1	1	1	0	0	0	1

Memory Card Control Register (MCCTRL)
Index Register: ECh
Index Address: 0Ah
Data Register: EDh

Bit 0 ENA0 - Enable Page 0: Enables page 0 of the memory card. If SA19-SA14 match the 6-bit compare value in the Page 0 Address Register and this bit is set, an access to the memory card will be generated. Power-on reset default = 0.

Bit 1 ENA1 - Enable Page 1: Enables page 1 of the memory card. If SA19-SA14 match the 6-bit compare value in the Page 0 Address Register and this bit is set, an access to the memory card will be generated. Power-on reset default = 0.

Bit 2 ENA2 - Enable Page 2: Enables page 2 of the memory card. If SA19-SA14 match the 6-bit compare value in the Page 0 Address Register and this bit is set, an access to the memory card will be generated. Power-on reset default = 0.

Bit 3 ENA3 - Enable Page 3: Enables page 3 of the memory card. If SA19-SA14 match the 6-bit compare value in the Page 0 Address Register and this bit is set, an access to the memory card will be generated. Power-on reset default = 0.

Bits 4-7 Reserved: These bits are reserved for possible future use (read as 1s). Do not use these bits.

RTC Address Mapping Register - Low Address Byte (RTCLSB)
Index Register: ECh
Index Address: 1Bh
Data Register: EDh

Bit 0 RENA - RTC Enable: If set, when SA15-SA1 match the 15-bit compare value in RTCLSB and RTCMSB, an access to the RTC is generated. If cleared, all accesses to the RTC are disabled. Power-on reset default = 1.

Bits 1-7 Lower Seven Bits of RTC Mapping Address: Combined with RTCMSB, this determines the address at which the RTC is accessed. Default = 70h.

RTC Address Mapping Register - High Address Byte (RTCMSB)
Index Register: ECh
Index Address: 1Ch
Data Register: EDh

Bits 0-7 Upper Byte of RTC Mapping Address: Combined with RTCLSB, this determines the address at which the RTC is accessed. Default = 00h.

Miscellaneous Control Register (KBDCTRL)
Index Register: ECh
Index Address: 1Dh
Data Register: EDh

Bit 0 SLP - Keyboard Sleep (active low): If HSLP is cleared, the clock to the keyboard controller is disabled if the SLP bit is cleared. Clock is resumed if any I/O read or write operation to the VL82C107 occurs, on the falling edge of the keyboard clock, or on the falling edge of the mouse clock input, if in PS/2 Mode. Power-on reset default = 1.

Bit 1 MODE - AT/PS2 Mode Select: If set, the keyboard operates in the AT Mode. If cleared, the keyboard operates in the PS/2 (keyboard and mouse) Mode. Power-on reset default = 1.

Bit 2 PRV - Private Controls Enable: If set, this bit prevents the KHSE, KSRE, and MIRQ pins from changing their current state. If cleared, normal operation of these pins results. Power-on reset default = 0.

Bit 3 MISC0 - KI0 Output: If the MODE bit is cleared (PS/2 Mode), this bit controls the KI0 output pin directly.

Bit 4 MISC1 - KI1 Output: If the MODE bit is cleared (PS/2 Mode), this bit controls the KI1 output pin directly.

Bit 5 RAMEN - PMU RAM Enable: Enables accesses to the alternate set of 64 bytes of battery-backed RAM in the RTC. If this bit is set, accesses to RTC addresses from 64-127h accesses the second 64 bytes of battery-backed RAM. Power-on reset default = 0.

Bit 6 HSLP - Hardware Sleep Enable: Enables the –SLP pin to enable or disable the clock to the keyboard controller. When set, –SLP control is enabled and the SLP bit operation is disabled. Power-on reset default = 1.

Bit 7 –KISLP - Keyboard in Sleep (active low): Reflects the state of the keyboard controller's Sleep Mode. If high, the keyboard is operating in Normal Mode. If low, the keyboard is in Sleep Mode. Power-on reset default = 1.

IDE/Chip Select Control Register (CSCTRL)
Index Register: ECh
Index Address: 2Eh
Data Register: EDh

Bit 0 IDEN - IDE Enable: When operating in the Chip Select Mode (see pin –CD1/–IDECS1 description), this bit, if set high, enables the generation of the –IDECS1, –IDENH, –IDENL, and IDED7 signals for the IDE interface. Power-on reset default = 1.

Bit 1 COMS - Communications Port Default Address: When operating in the Chip Select Mode (see pin –CD1/–IDECS1 description), this bit determines the I/O address at which the –CS0 and –CS1 signals are generated if the COMA and COMB bits are enabled, respectively. If set, –CS0 is activated for 3F8h-3FFh and –CS1 for 2F8h-2FFh, otherwise they are activated for addresses 3E8h-3EFh and 2E8h-2EFh, respectively.

Bit 2 COMA - Communications Port A Enable: When operating in the Chip Select Mode (see pin –CD1/–IDECS1 description), this bit, if set high, enables the generation of the –CS0 signal when COMA I/O address is accessed. Power-on reset default = 1.

Bit 3 COMB - Communications Port B Enable: When operating in the Chip Select Mode (see pin –CD1/–IDECS1 description), this bit, if set high, enables the generation of the –CS1 signal when COMB I/O address is accessed. Power-on reset default = 1.

Bits 4, 5 LPT1, LPT2 - Line Printer Address Selects: When operating in the Chip Select Mode (see pin –CD1/–IDECS1 description), these bits determine the I/O address at which the –CS2 signal is generated if LPTEN is enabled. The address is determined according to the table below:

LPT2	LPT1	–CS2
0	0	03BCh-03BFh
0	1	0378h-037Bh
1	0	0278h-027Bh
1	1	Reserved

Power-on reset default = 00h.

Bit 6 LPTEN - Line Printer Enable: When operating in the Chip Select Mode (see pin –CD1/–IDECS1 description), this bit, if set high, enables the generation of the –CS2 signal when the address determined by LPT1 and LPT2 is accessed. Power-on reset default = 1.

Bit 7 FDCEN - Floppy Disk Chip Select Enable: When operating in the Chip Select mode (see pin –CD1/–IDECS1 description), this bit, if set high, enables the generation of the –FDCCS signal when 3F0-3F7h I/O addresses are accessed. Power-on reset default = 1.

Revision/Chip ID Register (REVID)
Index Register: ECh
Index Address: 1Fh
Data Register: EDh

Bits 0-7 Returns value based on the version of the VL82C107. For the 3067-0000, this value is 70h. For 3067-1000, the value is 71h.

PC MEMORY CARD INTERFACE
The VL82C107 contains circuitry to minimize the interface logic needed to connect a PC memory card to a system. The interface memory card is implemented through a combination of dedicated hardware pins and software Control and Status Registers.

The location of the memory card within the system address space is determined by values written to the Memory Card Page Registers. The 6-bit values in these registers are compared to address values for all but refresh cycles and the appropriate card enable(s) is (are) generated when address bits 14-19 match the register value and the access is below 1 MB. This allows the memory card to be located on any 16K boundary. Four independent page registers are provided to allow mapping to four different base addresses. To set up a memory card page location, the 6-bit address value must be written to the appropriate page register, and the corresponding enable bit set in the Memory Card Control Register. A memory card enable is generated if any enabled page is matched.

The memory card enables are generated to allow 8- or 16-bit accesses to the memory card. The data width of the access is determined by the –EN8 bit in the Memory Card Status Register. –CE2 enables accesses to the high byte, –CE1 to the low byte. The enables are generated as shown in the following table.

–EN8	SA0	–SBHE	–CE1	–CE2
Low	Low	X	Low	High
Low	High	Low	Low	High
High	Low	Low	Low	Low
High	High	Low	High	Low
High	Low	High	Low	High
X	High	High	High	High

In 16-bit Mode, –MCS16 will be generated whenever an address match occurs.

The Memory Card Status Register contains bits that set or reflect the status of memory card pins. The operation of these bits are as follows:

Output Bits:
REG - Accesses to the register space of the memory card are performed by setting this bit high and then reading from or writing to the memory card.

–EN8 - Sets 8- or 16-bit Mode. Described above.

Input Bits:
All input bits reflect the status of the pins at the time of a read. The input pin values are latched during the read and any changes of status during the read will not be seen until the next read of the Status Register.

BVD1, BVD2 - Battery Voltage Detect: These reflect the status of the memory card battery and are interpreted as follows:

BVD1	BVD2	Register
Low	Low	Battery fail - memory card data invalid
Low	High	Battery fail - memory card data invalid
High	Low	Battery needs replacing - data OK
High	High	Battery OK - normal operation

WP - Write Protect: If the write protect switch is set on the memory card, this bit is set. All memory, including the register space, is protected on the memory card.

–BSY - Memory Card Busy: Indicates that the memory is busy and cannot be accessed. Primarily used for EPROM based cards to indicate a programming cycle is in progress.

–CD - Card Detect: This bit indicates that a memory card is present in the system. The bit is the OR of the two card detect input pins. These inputs are debounced using the XTAL clock to eliminate glitches of less than 5 ms as the card is being inserted.

ADDRESS BUFFERING AND AUXILIARY LOGIC

The address buffering and logic provide buffered addresses to and from the slot bus to the CPU. Depending on machine state, the SA and LA slot address lines can either be directly driven, driven from clocked data from the CPU A address lines, three-stated, or become inputs to drive the address back toward the CPU. These states are given in Table 6 as a function of the HLDA, –MASTER, and –REFRESH input lines.

TABLE 6. ADDRESS LINE DECODE

HLDA	–MASTER	–REFRESH	Cycle Type	SA1-SA8	SA9-SA16, –SBHE	SA17-SA19	LA17-LA23	CPU A Bus
0	0	0	Illegal					
0	0	1	Illegal					
0	1	0	Illegal					
0	1	1	CPU	Clocked	Clocked	Clocked	Latched	Input
1	0	0	Master Refresh	Direct	Three-state	Three-state	Three-state	Input
1	0	1	Master	Input	Input	Three-state	Input	Output Direct
1	1	0	Normal Refresh	Direct	Three-state	Direct	Direct	Input
1	1	1	DMA	Direct	Direct	Direct	Direct	Input

Clocked: The value of the CPU A address line is clocked into a flip-flop on the rising edge of the –EALE and output on the SA lines.

Latched: The value of the CPU A address line is latched when –EALE is high.

Direct: The value of the CPU A address line is buffered and output on the SA/LA lines.

Output Direct: The value of the SA/LA lines are buffered and output to the CPU.

Three-state: The SA lines are floating.

KEYBOARD CONTROLLER

The keyboard controller is accessed via internally decoded port 060h (read/write data) and port 064h (read status/write command).

PC/AT or PS/2 compatibility is controlled via bit 1 in the Keyboard Control (KBDCTRL) Register.

KEYBOARD CONTROLLER FUNCTIONAL DESCRIPTION

The VL82C107 keyboard controller's microcontroller unit (MCU) offers a subset of the instruction set of the 8042, with 8042-like instructions. Enhancements have been made to conditional jumps (jumps may be made between pages). The on-chip ROM is loaded with the code that is required to support both PC/AT and PS/2 command sets, and the 128 bytes of conversion code. A small amount of scratch-pad RAM is provided as an extension of the MCU register set for the purpose of keyboard to host interfacing.

Keyboard serial I/O is handled with hardware implementations of the receiver and transmitter. Both functions depend on an 8-bit timer for time-out detection. Enhanced status reporting is provided in hardware to simplify error handling in software. This logic is duplicated for the mouse interface.

User RAM support is provided. The program writes the 5-bit address (32-byte range) to a register, and then reads or writes the data through accesses to another register, port 60h DBB.

Parallel ports 1 and 2 are provided, but are restricted to inputs only for P1 and outputs only to P2.

Support for port 60h DBB (reads and writes) and the Status Register (reads and writes) is provided in hardware for interface to the PC host.

Common PC/AT uses for the parallel I/O bits are shown below:

- P16 - Color/monochrome input
- P17 - Key switch input
- P20 - Reset CPU output
- P21 - A20 Gate output
- P22 - Speed select output

KEYBOARD CONTROLLER INTERFACE TO PC/AT

The interface to the PC/AT consists of 1 register pair (60h/64h) for the keyboard and mouse. Access to the registers is determined by the state of A2 and the chip select. For host control signals involved, the Command, Status, and Data Registers are accessed as shown in Table 7.

The port 60h DBB read operation outputs the contents of the output buffer to D7-D0 (host bidirectional, three-state data bus), and clears the status of the Output Buffer Full (OBF/Status Register bit 0) bit.

Status read operations output the contents of the Status Register to D7-D0. No status is changed as a result of the read operation.

The port 60h DBB write operations cause the input buffer DBB to be changed. The state of the C/D bit is cleared (Status Register bit 3, 0 indicates data) and the Input Buffer Full (IBF/Status Register bit 1) bit is set (1).

Command write operations are the same as DBB writes, except that the address is 64h. The C/D bit will be set (1) when a command has been written to address 64h.

KEYBOARD CONTROLLER INTERFACE PROTOCOL

Data transmission between the controller and the keyboard or mouse consist of a synchronous bit stream over the data and clock lines. The bits are defined as follows:

Bit	Function
1	Start bit (always 0)
2	Data bit (LSB)
3-8	Data bits 1-6
9	Data bit 7 (MSB)
10	Parity bit (odd)
11	Stop bit (always 1)

KEYBOARD CONTROLLER RECEIVE AND TRANSMIT OPERATIONS

The states that are implemented for receive and transmit operations are shown in Figures 1 and 2.

TABLE 7. ACCESSING THE COMMAND, STATUS, AND DATA REGISTERS

–CS	–IOR	–IOW	–A2	Register
0	0	1	0	Read - Data DBB Output Buffer
0	0	1	1	Read - Status
0	1	0	0	Write - Data DBB Input Buffer
0	1	0	1	Write - Command
1	X	X	X	Not Valid

FIGURE 1. CONTROLLER RECEIVES FROM KEYBOARD

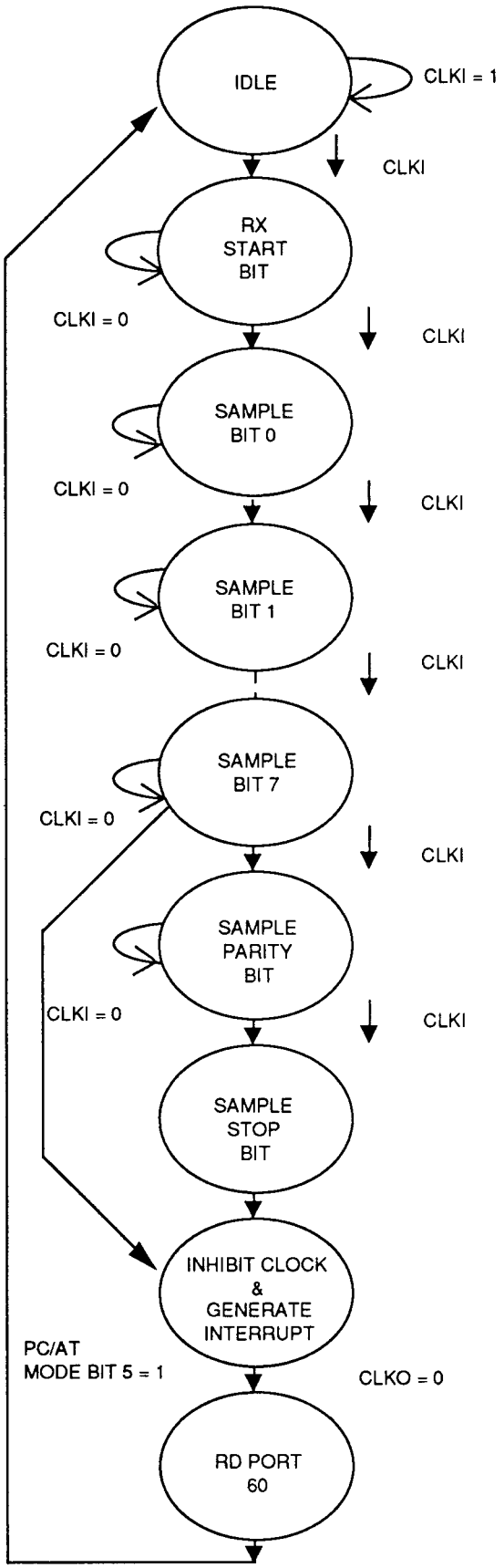
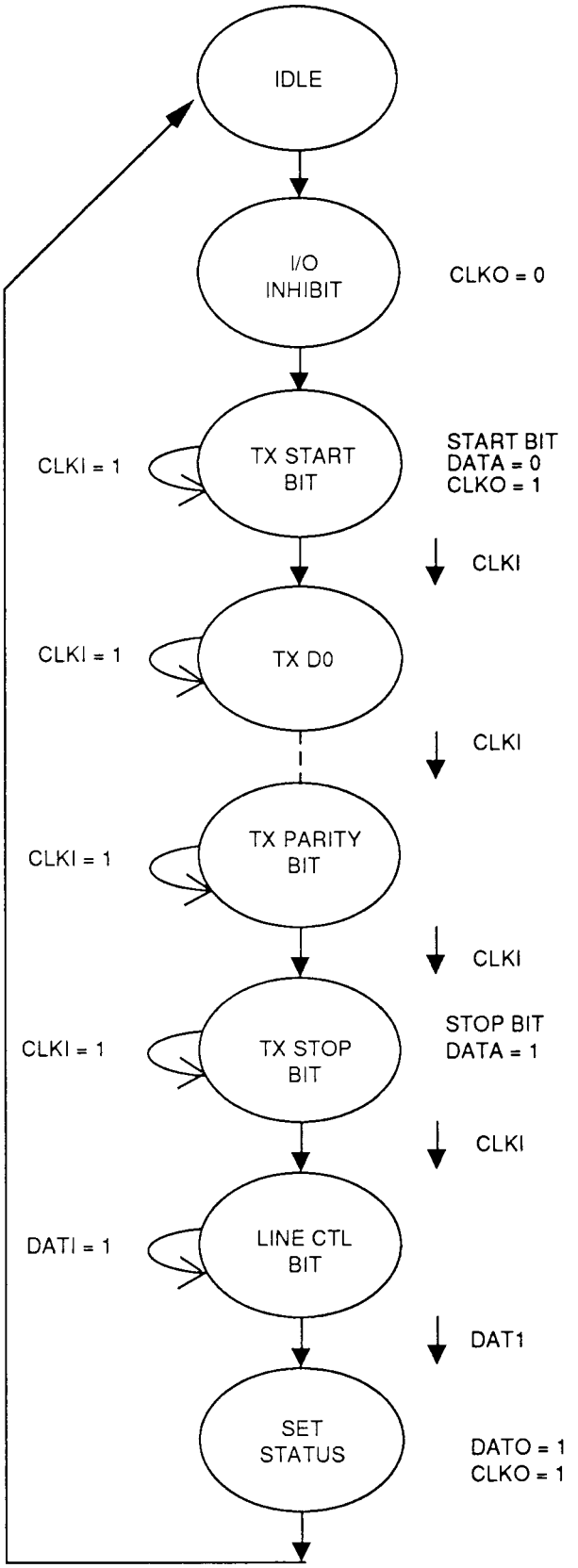


FIGURE 2. CONTROLLER TRANSMITS TO KEYBOARD



PROGRAMMER INTERFACE

The programmer interface to the keyboard controller is quite simple. It consists of the following four registers:

Register	R/W	I/O
Status	R	64h
Command	W	64h
Output Buffer	R	60h
Input Buffer	W	60h

The behavior of these registers differs according to the mode of operation (PC/AT or PS/2). There exists only one Status Register with different bit definitions for PC/AT Mode and PS/2 Mode. The bit definitions for the Status Register in each mode are listed in Tables 8 and 9.

PC/AT Status Register

Bit 0 OBF - Output Buffer Full: This flag is automatically set when the microcontroller loads DBBOUT. It is cleared on a read to port 60h.

Bit 1 IBF - Input Buffer Full: This flag is set on a write to port 60h or 64h. It is cleared when the microcontroller reads the DBBIN contents into the accumulator.

Bit 2 SYS - System Flag: When set (1), this indicates that the CPU has changed from Virtual to Real Mode.

Bit 3 C/D - Command/Data: When set (1), this indicates that a command has been placed into the input data buffer of the controller. A 0 indicates data. The controller uses this bit to determine if the byte written is a command to be executed. This bit is updated when the next byte is written to the input data buffer.

Bit 4 KBEN - Keyboard Enable: When set (1), it indicates that the keyboard is currently enabled. When reset, it indicates that the keyboard is inhibited.

Bit 5 TTIM - Transmit Time-Out: When set (1), it indicates that a transmission to the keyboard was not completed before the controller's internal timer timed out.

Bit 6 RTIM - Receive Time-Out: When set (1), it indicates that a transmission from the keyboard was not completed before the controller's internal timer timed out.

Bit 7 PERR - Parity Error: When set (1), it indicates that a parity error (even parity = error) occurred during the last transmission (received scan code) from the keyboard. When a parity error is detected, the output buffer is loaded with FFh, the OBF status bit is set and the KIRQ pin is set (1 if the EKI bit/Mode Register bit 0 is set(1)).

TABLE 8. PC/AT STATUS REGISTER (Read-only - Port 64h)

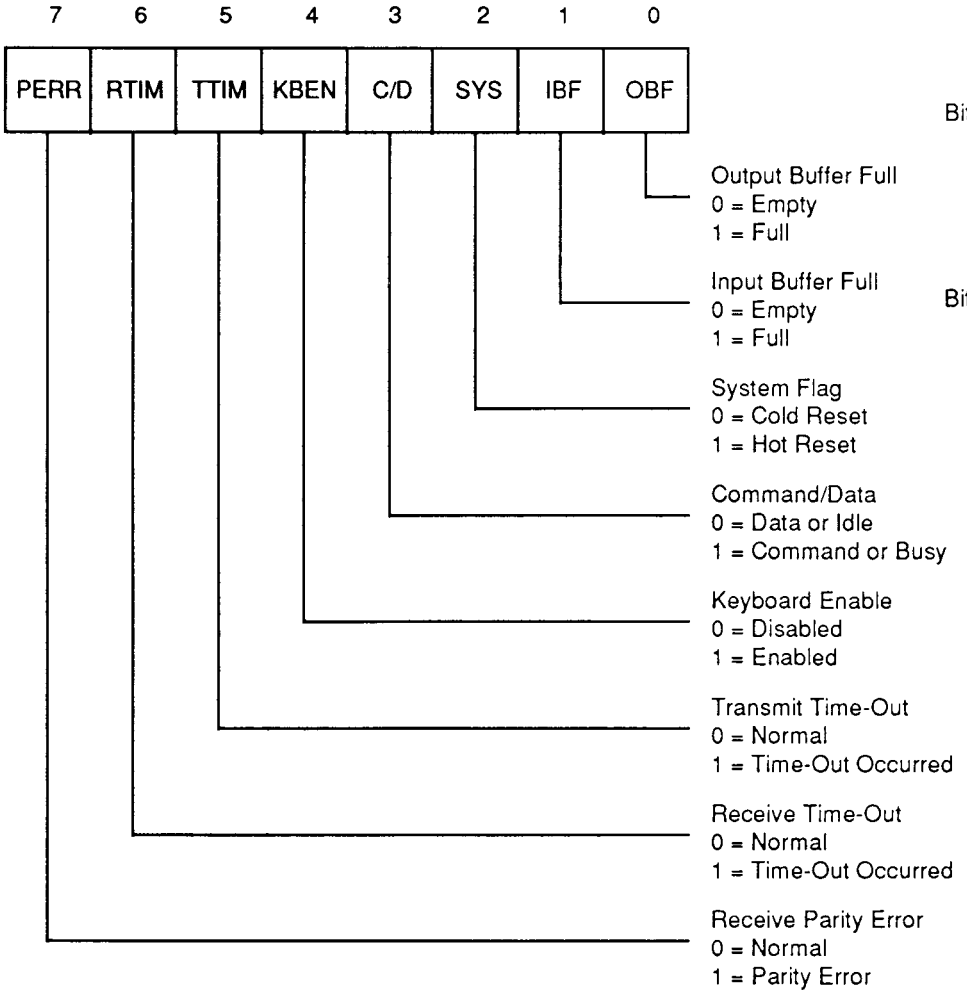
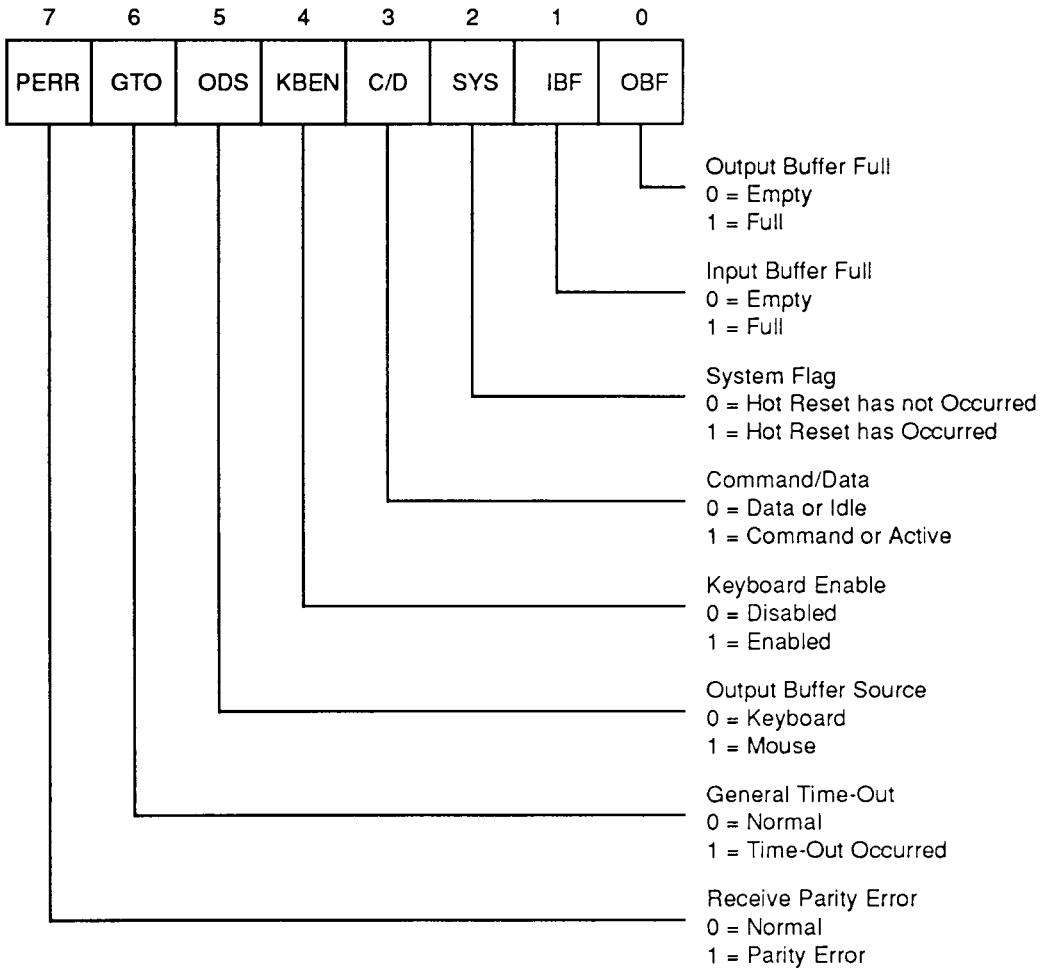


TABLE 9. PS/2 STATUS REGISTER (Read-only - Port 64h)



PS/2 Status Register

Bit 0 OBF - Output Buffer Full: This flag is automatically set when the microcontroller loads the output data buffer. It is cleared on a read to port 60h.

Bit 1 IBF - Input Buffer Full: This flag is set on a write to port 60h or 64h. It is cleared when the microcontroller reads the input data buffer contents into the accumulator.

Bit 2 SYS - System Flag: When set (1), it indicates that the CPU has changed from Virtual to Real Mode.

Bit 3 C/D - Command/Data: When set (1), it indicates that a command has been placed into the input data buffer of the controller, a 0 indicates data. The controller uses this bit to determine if the byte written is a command to be executed. This bit is updated when the next byte is written to the input data buffer.

Bit 4 KBEN - Keyboard Enable: When set (1), it indicates that keyboard is currently enabled. When cleared (0), it indicates that the keyboard is inhibited.

Bit 5 ODS - Output Buffer Data Source: When set (1), it indicates that the data in the output buffer is mouse data. When cleared (0), it indicates the data is from the keyboard.

Bit 6 GTO - General Time-Out Error: When set (1), it indicates that a transmission was started and that it did not complete within the normal time taken (approximately 11 KCLK cycles). If the transmission originated from the controller, a FEh is placed in the output buffer. If the transmission originated from the keyboard, a FFh is placed in the output buffer.

Bit 7 PERR - Parity Error: When set (1), it indicates that a parity error (even parity = error) occurred during the last transmission from the keyboard. When a parity error is detected, the output buffer is loaded with FFh, the OBF status bit is set and the KIRQ pin is set (1 if the EKI bit/ Mode Register bit 0 is set (1)).

KEYBOARD CONTROLLER COMMAND SET

This command set supports two modes of operation and a set of extensions to the AT command set for the PS/2. In both modes, the command is implemented by writing the command byte to 64h. Any subsequent data is read from 60h (see description of command 20) or written to 60h (see description of command 60). The commands for each mode are shown in the Tables 10 and 11.

Command Descriptions

The keyboard controller will support the following command set, which is described as the hex command code, followed by a description:

20 Read Keyboard Controller's Mode Register (PC/AT and PS/2): The keyboard controller sends its current mode byte to the output buffer (accessed by a read of port 60h).

60 Write Keyboard Controller's Mode Register (PC/AT and PS/2): The next byte of data written to the keyboard data port (60h) is placed in the controller's Mode Register.

The bit definitions of the Mode Register for each mode (PC/AT or PS/2) are described in Tables 12 and 13.

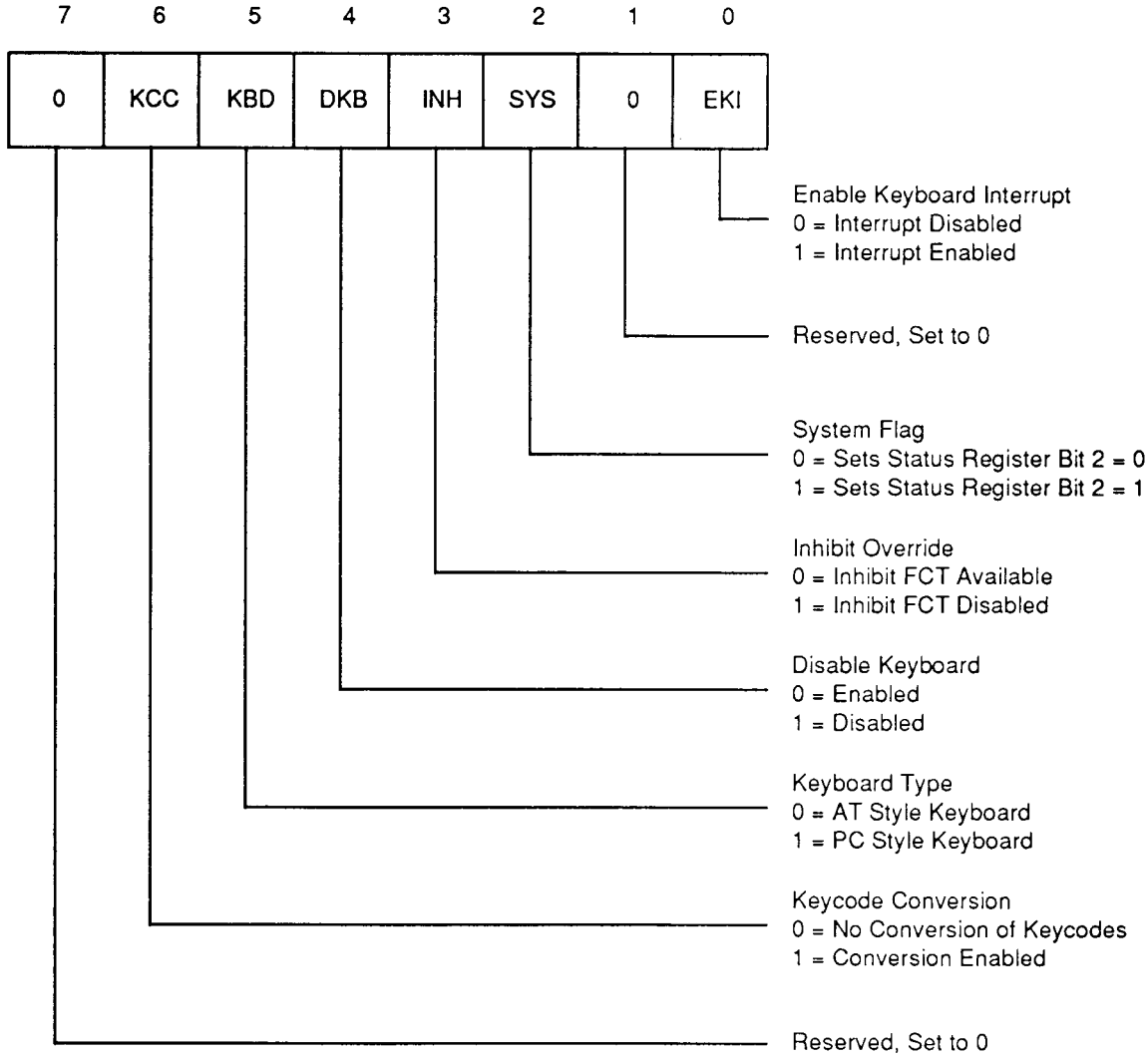
TABLE 10. PC/AT & PS/2 COMMANDS

Command	Description
20	Read Mode Register
60	Write Mode Register
21-3F	Read Keyboard Controller RAM (Byte 1-31)
61-7F	Write Keyboard Controller RAM (Byte 1-31)
AA	Self Test
AB	Keyboard Interface Test
AC	Diagnostic Dump
AD	Disable Keyboard
AE	Enable Keyboard
C0	Read Input Port (P10-P17)
D0	Read Output Port (P20-P27)
D1	Write Output Port (P20-P27)
E0	Read Test Inputs (T0, T1)
F0-FF	Pulse Output Port (P20-P27)

TABLE 11. ADDED PS/2 COMMANDS

Command	Description
A4	Test Password
A5	Load Password
A6	Enable Password
A7	Disable Mouse
A8	Enable Mouse
A9	Mouse Interface Test
C1	Poll Input Port Low (P10-P13 = S4-S7)
C2	Poll Input Port High (P14-P17 = S4-S7)
D2	Write Keyboard Output Buffer
D3	Write Mouse Output Buffer
D4	Write to Mouse

TABLE 12. PC/AT MODE REGISTER (R/W - Command 20h/60h to Port 60h)



PC/AT Mode Register

Bit 0 EKI - Enable Keyboard Interrupt: When set (1), it allows the controller to generate a keyboard interrupt whenever data (keyboard or controller) is written into the output buffer.

Bit 1 Reserved: This bit should be written as 0.

Bit 2 SYS - System Flag: When set (1), it writes the system flag bit 2 of the Status Register to 1. This bit is used to indicate a switch from Virtual to Real Mode when set.

Bit 3 INH - Inhibit Override: When set (1), it disables the keyboard inhibit function (P17 switch).

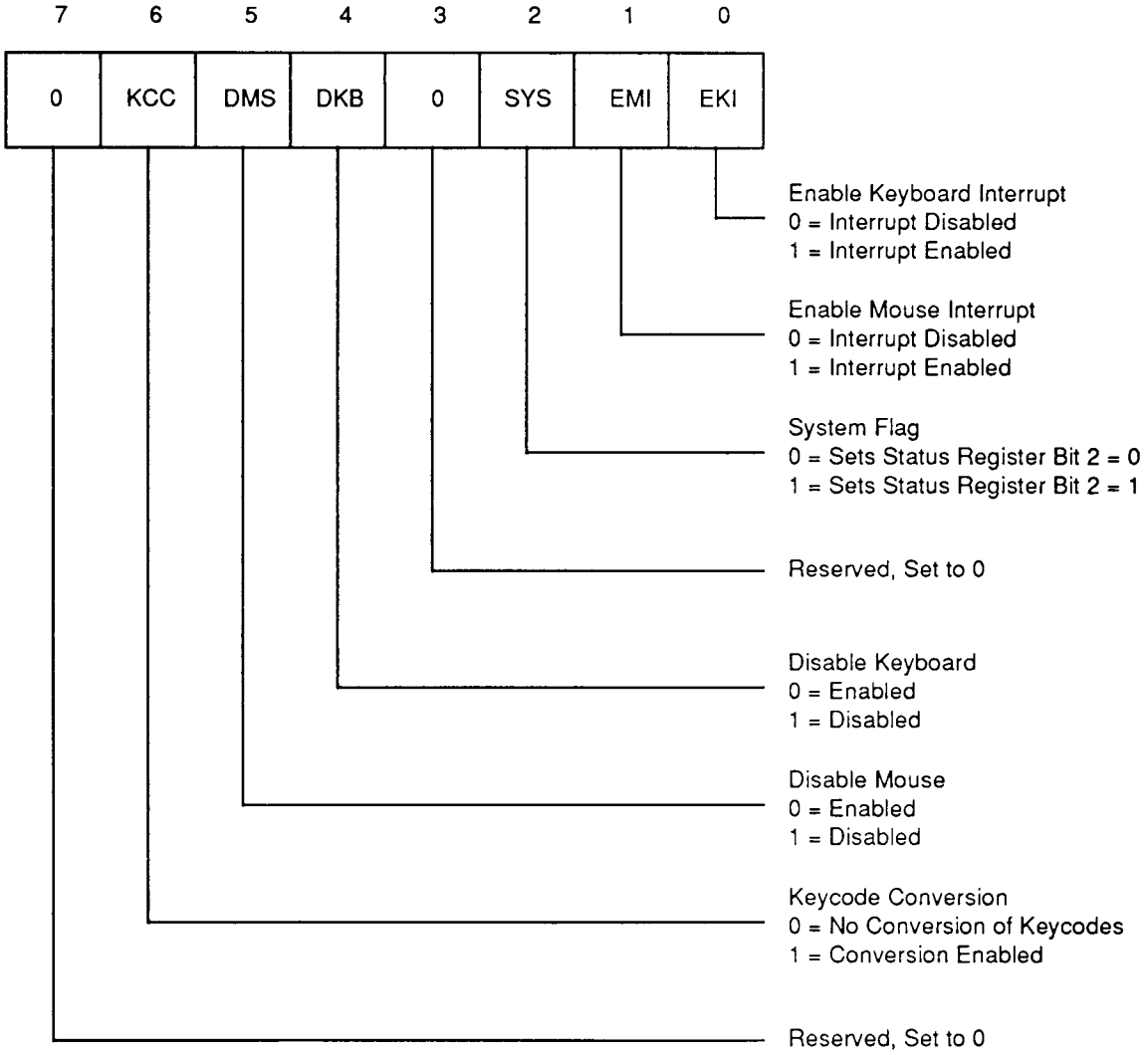
Bit 4 DKB - Disable Keyboard: When set (1), it disables the keyboard by holding the KCLK line high.

Bit 5 KBD - Keyboard Type: When set (1), it allows for compatibility with PC-style keyboards. In this mode, parity is not checked and scan codes are not converted.

Bit 6 KCC - Keycode Conversion: When set (1), it causes the controller to convert the scan codes to PC format. When cleared (0), the codes are passed along unconverted.

Bit 7 Reserved: This bit should be written as 0.

TABLE 13. PS/2 MODE REGISTER (R/W - Command 20h/60h to Port 60h)



PS/2 Mode Register

Bit 0 EKI - Enable Keyboard Interrupt: When set (1), it allows the controller to generate a keyboard interrupt whenever data (keyboard or command) is written into the output buffer.

Bit 1 EMI - Enable Mouse Interrupt: When set (1), it allows the controller to generate a mouse interrupt when mouse data is available in the output buffer.

Bit 2 SYS - System Flag: When set (1), it writes the system flag bit 2 of the Status Register to 1. This bit is used to indicate a switch from Virtual to Real Mode when set.

Bit 3 Reserved: This bit should be written as 0.

Bit 4 DKB - Disable Keyboard: When set (1), it disables the keyboard by holding the KCLK output high.

Bit 5 DMS - Disable Mouse: When set (1), it disables the mouse by holding the KSRE output high in PS/2 Mode (mouse clock).

Bit 6 KCC - Keycode Conversion: When set (1), it causes the controller to convert the scan codes to PC format. When cleared (0), the codes are passed along unconverted.

Bit 7 Reserved: This bit should be written as 0.

Command Descriptions (Cont.)

21-3F Read Keyboard Controller RAM (PC/AT and PS/2): Bits D4-D0 specify the address.

61-7F Write the Keyboard Controller RAM (PC/AT and PS/2): This command writes to the keyboard controller RAM with the address specified in bits D4-D0.

A4 Test Password Installed (PS/2 only): This command checks if there is currently a password installed in the controller. The test result is placed in the output buffer (the OBF bit is set) and KIRQ is asserted (if the EKI bit is set). Test result - FAh means that the password is installed, and F1h means that it is not.

A5 Load Password (PS/2 only): This command initiates the password load procedure. Following this command, the controller will take data from the input buffer port (60h) until a 00h is detected or a full 8-byte password including a delimiter (e.g., <cr>) is loaded into the password latches.

Note: This means that during password validation the password can be a maximum of 7 bytes with a delimiter such as <cr>.

A6 Enable Password (PS/2 only): This command enables the security feature. The command is valid only when a password pattern is written into the controller (see A5 command). No other commands will be "honored" until the security sequence is completed and command A6 is cleared.

A7 Disable Mouse (PS/2 only): This command sets bit 5 of the Mode Register which disables the mouse by driving the KSRE line (mouse clock) high.

A8 Enable Mouse (PS/2 only): This command resets bit 5 of the Mode Register, thus enabling the mouse again.

A9 Mouse Interface Test (PS/2 only): This command causes the controller to test the mouse clock and data lines. The results are placed in the output buffer (the OBF bit is set) and the KIRQ line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No Error
01	Mouse Clock Line Stuck Low
02	Mouse Clock Line Stuck High
03	Mouse Data Line Stuck Low
04	Mouse Data Line Stuck High

AA Self Test (PC/AT and PS/2): This commands the controller to perform internal diagnostic tests. A 55h is placed in the output buffer if no errors were detected. The OBF bit is set and KIRQ is asserted (if the EKI bit is set).

AB Keyboard Interface Test (PC/AT and PS/2): This command causes the controller to test the keyboard clock and data lines. The test result is placed in the output buffer (the OBF bit is set) and the KIRQ line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No Error
01	Keyboard Clock Line Stuck Low
02	Keyboard Clock Line Stuck High
03	Keyboard Data Line Stuck Low
04	Keyboard Data Line Stuck High

AC Diagnostic Dump (PC/AT only, reserved on PS/2): Sends 16 bytes of the controller's RAM, the current state of the input port, and the current state of the output port to the system.

AD Disable Keyboard (PC/AT and PS/2): This command sets bit 4 of the Mode Register to a 1. This disables the keyboard by driving the clock line (KCLK) high. Data will not be received. The keyboard will be enabled after the system sends data to be transmitted to the keyboard.

AE Enable Keyboard (PC/AT and PS/2): This command resets bit 4 of the mode byte to a 0. This enables the keyboard again by allowing the keyboard clock to free-run.

C0 Read P1 Input Port (PC/AT and PS/2): This command reads the keyboard input port and places it in the output buffer. This command overwrites the data in the buffer.

C1 Poll Input Port Low (PS/2 only): P1 bits 0-3 are written into Status Register bits 4-7. The bits are restored to their original status upon a write to port 64h.

C2 Poll Input Port High (PS/2 only): P1 bits 4-7 are written into Status Register bits 4-7. The bits are restored to their original status upon a write to port 64h.

D0 Read Output Port (PC/AT and PS/2): This command causes the controller to read the P2 output port and place the data in its output buffer. The definitions of the bits are as follows:

Bit	Pin	PC/AT Mode	PS/2 Mode
1	P20	-RC	-RC
1	P21	A20 Gate	A20 Gate
2	P22	Speed Sel (ENMOD)	Mouse Data
3	P23	Shadow Enable	Mouse Clk
4	P24	Output Buffer Full	KIRQ
5	P24		MIRQ
6	P26	-KCLKOUT	-KCLKOUT
7	P27	KDATOUT	-KDATOUT

D1 Write Output Port (PC/AT and PS/2): The next byte of data written to the keyboard data port (60h) will be written to the controller's output port. The definitions of the bits are as defined previously. In PC/AT Mode, P26 and P27 will not be altered. In PS/2 Mode, P22, P23, P26 and P27 cannot be altered.

D2 Write Keyboard Output Buffer (PS/2 only): The next byte written to the data buffer (60h) is written by the output buffer (60h) as if initiated by the keyboard (the OBF bit is set (1) and KIRQ will be set if the EKI bit is set (1)).

D3 Write Mouse Output Buffer (PS/2 only): The next byte written to the data buffer (60h) is written to the output buffer as if initiated by the mouse (the OBF bit is set (1) and MIRQ will be set if the EMI bit is set (1)).

D4 Write to Mouse (PS/2 only): The next byte written to the data buffer (60h) is transmitted to the mouse.

Note: If data is written to the data buffer (60h) and the command preceding it did not expect data from the port (60h), the data will be transmitted to the keyboard.

E0 Read Test Inputs (PC/AT and PS/2): This command causes the controller to read the T0 and T1 input bits. The data is placed in the output buffer with the following meanings:

Bit	PC/AT Mode	PS/2 Mode
0	Kybd Clk	Kybd Clk
1	Kybd Data	Mouse Clk
3-7	Read as 0s	Read as 0s

F0-FF Pulse Output Port (PC/AT and PS/2): Bits 0-3 of the controller's output port may be pulsed low for approximately 6 µs. Bits 0-3 of the command specify which bit will be pulsed. A 0 indicates that the bit should be pulsed, a 1 indicates that the bit should not be modified. FF is treated as a special case (Pulse Null Port).

Note: In PS/2 Mode, bits P22 and P23 will not be pulsed.

Sleep Mode Operation

The VL82C107 can be put into a low-power mode of operation in which the high frequency internal clock to the keyboard controller is stopped and resumed in a controlled manner, thereby lowering the power dissipation of the device considerably. Entry into this mode can be controlled by two methods, either by an externally controlled –SLP input pin or by a software configurative control bit. A bit in the KBDCTRL Register, HSLP, enables either mode of operation. When in the –SLP input pin controlled mode, levels on this pin determine whether the keyboard clock is enabled or disabled. In the software controlled mode, the keyboard clock is disabled by clearing the SLP bit in the KBDCTRL Register. The clock remains disabled until either an I/O read or write operation to the VL82C107 occurs or until a falling edge occurs on the keyboard clock input, KCLK, or the mouse clock input, KSRE, if PS/2 Mode has been enabled. The sleep status of the keyboard controller can be determined by reading bit 7 of the KBDCTRL Register.

REAL-TIME CLOCK DESCRIPTION

The real-time clock (RTC) portion of the VL82C107 performs the following functions:

- Time of day clock
- Alarm function
- 100 year calendar function
- Programmable periodic interrupt output
- Programmable square wave output
- 50 bytes of user RAM
- User RAM preset feature

The RTC memory consists of ten RAM bytes which contain the time, calendar and alarm data, four control and status bytes, and 50 general purpose RAM bytes. The address map of the real-time clock is shown as follows:

Addr	Function	Range
0	Seconds (time)	0-59
1	Seconds (alarm)	0-59
2	Minutes (time)	0-59
3	Minutes (alarm)	0-59
4	Hours (time)	0-11, 12 Hr Mode
4	Hours (time)	0-23, 24 Hr Mode
5	Hours (alarm)	0-23
6	Day of Week	1-7
7	Date of Month	1-31
8	Month	1-12
9	Year	0-99
10	RTC Register A	(R/W)
11	RTC Register B	(R/W)
12	RTC Register C	(R-O)
13	RTC Register D	(R-O)
14-127	User RAM (standby)	

All 127 bytes are directly readable and writeable by the processor program except for the following:

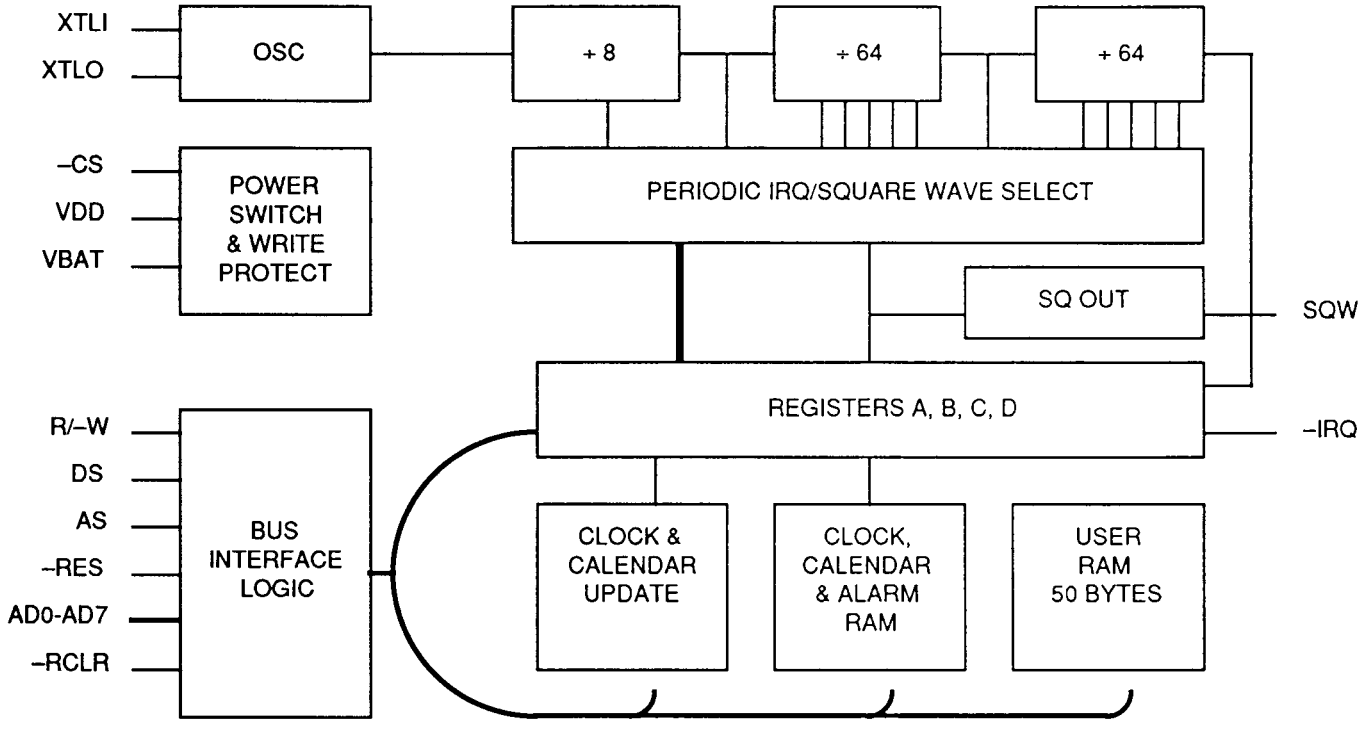
1) Registers C and D are read-only.
2) Bit 7 of Register A is read-only.
3) Bit 7 of the seconds byte is read-only.

The RTC address map also includes additional standby RAM. The bottom 64 bytes of the address space are devoted to the RTC function. Two banks of additional standby RAM is mapped into this space in the index address range of 64-127. Control of which bank is accessed is provided by the RAMEN bit of the KBDCTRL Register. The total address map is shown below:

Addr	Function
0-13	Time portion
14-63	Scratch-pad RAM portion
64-127	Dual-mapped additional scratch-pad RAM

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the ten time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

FIGURE 3. REAL-TIME CLOCK BLOCK DIAGRAM



TIME OF DAY REGISTER DESCRIPTIONS

The contents of the Time of Day Registers can be either in binary or binary-coded decimal (BCD) format. The address map of these registers is shown below:

Addr	Function	Range
0	Seconds (time)	0-59
1	Seconds (alarm)	0-59
2	Minutes (time)	0-59
3	Minutes (alarm)	0-59
4	Hours (time)	0-11, 12 Hr Mode
4	Hours (time)	0-23, 24 Hr Mode
5	Hours (alarm)	0-23
6	Day of Week	1-7
7	Date of Month	1-31
8	Month	1-12
9	Year	0-99

Address 0 - Seconds:
The range of this register is 0-59 in BCD Mode and 0-3Bh in Binary Mode.

Address 1 - Seconds Alarm:
The range of this register is 0-59 in BCD Mode and 0-3Bh in Binary Mode.

Address 2 - Minutes:
The range of this register is 0-59 in BCD Mode and 0-3Bh in Binary Mode.

Address 3 - Minutes Alarm:
The range of this register is 0-59 in BCD Mode and 0-3Bh in Binary Mode.

Address 4 - Hours:
The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01h-0Ch	Binary	AM
81h-8Ch	Binary	PM

Address 5 - Hours Alarm:
The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01h-0Ch	Binary	AM
81h-8Ch	Binary	PM

Address 6 - Day of Week:
The range of this register is 1-7 in BCD Mode and 1-7h in Binary Mode.

Address 7 - Date:
The range of this register is 1-31 in BCD Mode and 1-1Fh in Binary Mode.

Address 8 - Month:
The range of this register is 1-12 in BCD Mode and 1-0Ch in Binary Mode.

Address 9 - Year:
The range of this register is 0-99 in BCD Mode and 0-63h in Binary Mode.

RTC CONTROL REGISTER DESCRIPTIONS

The VL82C107 has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Addr	Function	Type
10	RTC Register A	(R/W)
11	RTC Register B	(R/W)
12	RTC Register C	(R-O)
13	RTC Register D	(R-O)
14-63	User RAM (Standby)	(R/W)

Register A Description

This register contains control bits for the selection of the periodic interrupt, input divisor, and update-in-progress (UIP) status bit. The bits in the register are defined as follows:

Bit	Description	Abbr
0	Rate Select bit 0	RS0
1	Rate Select bit 1	RS1
2	Rate Select bit 2	RS2
3	Rate Select bit 3	RS3
4	Divisor bit 0	DV0
5	Divisor bit 1	DV1
6	Divisor bit 2	DV2
7	Update-in-progress	UIP

Bits 0-3 RS0-RS3 - Rate Select: These four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate a periodic interrupt. These four bits are read/write bits which are not affected by reset. The periodic interrupt rate that results from the selection of various tap values is as follows:

RS Value	Periodic Interrupt Rate	
0	None	
1	3.90625	ms
2	7.8125	ms
3	122.070	µs
4	244.141	µs
5	488.281	µs
6	976.562	µs
7	1.953125	ms
8	3.90625	ms
9	7.8125	ms
0Ah	15.625	ms
0Bh	31.25	ms
0Ch	62.5	ms
0Dh	125	ms
0Eh	250	ms
0Fh	500	ms

Bits 4-6 DV0-DV2 - Divisor: The three divisor selection bits are fixed to provide for only a five-state divider chain, which would be used with a 32 kHz external crystal. Only bit 6 of this register can be changed allowing control of the reset for the divisor chain. When the divider reset is removed the first update cycle begins one-half second later. These bits are not affected by power-on reset (external pin).

DV Value	Condition
2	Operation Mode, divider running
6	Reset Mode, divider in reset state

Bit 7 UIP - Update-In-Progress: This bit is a status flag that may be monitored by the program. When a 1, the update cycle is in progress or will soon begin. When a 0, the update cycle is not in progress and will not be for at least 244 µs. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is 0. The UIP bit is a read-only bit, and is not affected by reset. Writing the SET bit in Register B to a 1 will inhibit any update cycle and then clear the UIP status bit.

Register B Description
Register B contains command bits to control various modes of operations and interrupt enables for the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Daylight Savings Enable	DSE
1	24/12-Hour Mode	24/12
2	Data Mode (Binary or BCD)	DM
3	Reserved	
4	Update-End Interrupt Enable	UIE
5	Alarm Interrupt Enable	AIE
6	Periodic Interrupt Enable	PIE
7	Set Command	SET

Bit 0 DSE - Daylight Savings Enable: A read/write bit which allows the program to enable two special updates (when DSE is 1). On the last Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October, when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a 0. DSE is not changed by any internal operations or reset.

Bit 1 24/12 - 24/12-Hour Mode: This control bit establishes the format of the hours bytes as either the 24-Hour Mode (1) or the 12-Hour Mode (0). This is a read/write bit, which is affected only by software.

Bit 2 DM - Data Mode: This bit indicates whether time and calendar updates are to use a binary or a BCD format. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or reset. A 1 in DM specifies binary data, while a 0 specifies BCD data.

Bit 3 Reserved: This bit is unused in this version of the RTC.

Bit 4 UIE - Update-End Interrupt Enable: A read/write bit which enables the update-end flag (UF) bit in Register C to assert an –RTCIRQ. The RSTDRV pin being asserted or the SET bit going high clears the UIE bit.

Bit 5 AIE - Alarm Interrupt Enable: A read/write bit which, when set to a 1, permits the alarm flag (AF) bit in Register C to assert an –RTCIRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of 11XXXXXXb). When the AIE bit is a 0, the AF bit does not initiate an –RTCIRQ signal. The RSTDRV pin clears AIE to 0. The internal functions do not affect the AIE bit.

Bit 6 PIE - Periodic Interrupt Enable: A read/write bit which allows the periodic interrupt flag (PF) bit in Register C to cause the –RTCIRQ pin to be driven low. A program writes a 1 to the PIE bit in order to receive periodic interrupts at the rate specified by RS3-RS0 in Register A. A 0 in PIE blocks –RTCIRQ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal functions but is cleared to 0 by a reset.

Bit 7 SET - Set Command: When the SET bit is a 0, the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a 1, any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not modified by reset or internal functions.

Register C Description
Register C contains status information about interrupts and internal operation of the real-time clock. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Reserved, Read as 0	
1	Reserved, Read as 0	
2	Reserved, Read as 0	
3	Reserved, Read as 0	
4	Update-Ended Flag	UF
5	Alarm Interrupt Flag	AF
6	Periodic Interrupt Flag	PF
7	–RTCIRQ Pending Flag	IRQF

Bits 0-3 Reserved: These bits are read as 0s and cannot be written.

Bit 4 UF - Update-Ended Interrupt Flag: This bit is set after each update cycle. When the UIE bit is a 1, the 1 in UF causes the IRQF bit to be a 1, asserting –RTCIRQ. UF is cleared by a Register C read or a reset.

Bit 5 AF - Alarm Interrupt Flag: A 1 indicates that the current time has matched the alarm time. A 1 also causes the –RTCIRQ pin to go low, and a 1 to appear in the IRQF bit when the AIE bit also is a 1. A reset or a read of Register C clears AF.

Bit 6 PF - Periodic Interrupt Flag: This is a read-only bit which is set to a 1 when a particular edge is detected on the selected tap of the divider chain. The RS3-RS0 bits establish the periodic rate. PF is set to a 1 independent of the state of the PIE bit. PF being a 1 initiates an –RTCIRQ signal and sets the IRQF bit when PIE is also a 1. The PF bit is cleared by a reset or a software read of Register C.

Bit 7 IRQF - Interrupt Request Flag: This bit is set to a 1 when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

The logic can be expressed in equation form as:

IRQF = PF • PIE + AF • AIE + UF • UIE

Any time the IRQF bit is a 1, the –RTCIRQ pin is asserted. All flag bits are cleared after Register C is read by the program or when the RSTDRV pin is asserted.

Register D Description
Register D contains a bit that indicates the status of the on-chip standby RAM. The contents of the registers are described as the following:

Bit	Description	Abbr
0	Not Used, Read as 0	
1	Not Used, Read as 0	
2	Not Used, Read as 0	
3	Not Used, Read as 0	
4	Not Used, Read as 0	
5	Not Used, Read as 0	
6	Not Used, Read as 0	
7	Valid RAM Data and Time	VRT

Bits 0-6 Reserved: These bits cannot be written and are always read as 0s.

Bit 7 VRT - Valid RAM Data and Time: It indicates the condition of the contents of the RAM, provided the power-sense (PS) pin is satisfactorily connected. A 0 appears in the VRT bit when the PS pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read-only bit which is not modified by the RSTDRV pin. The VRT bit can only be set by reading Register D.

RTC CMOS STANDBY RAM DESCRIPTION
In addition to the 50 dedicated general purpose RAM bytes, the VL82C107 provides an additional 128 bytes of battery-backed RAM for general purpose uses. They can be used by the system BIOS or user program, and are available during the RTC update cycle. They are mapped as two banks of 64 bytes each residing in the 64-127 index address range. Access to these banks is controlled by setting the RAMEN bit of the KBDCTRL Register.

GENERAL OPERATIONAL NOTES
Set Operation
Before initializing the internal registers, the SET bit in Register B should be set to a 1 to prevent time/calendar updates from occurring. The program initializes the ten locations in the selected format (binary or BCD), then indicates the format in the Data Mode (DM) bit of Register B. All ten time, calendar, and alarm bytes must use the same Data Mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized, the real-time clock makes all updates in the selected Data Mode. The Data Mode cannot be changed without re-initializing the ten data bytes.

24/12-Hour Mode
The 24/12 bit in Register B establishes whether the hour locations represent 0-11 or 0-23. The 24/12 bit cannot be changed without re-initializing the hour locations. When the 12-Hour Mode is selected, the high-order bit of the hours byte represents PM when it is a 1.

Update Operation
The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the ten bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the ten bytes are read at this time, the data outputs are undefined. The update lockout time is 1948 µs for the 32.768 kHz time base. The update cycle section shows how to accommodate the update cycle in the processor program.

Alarm Operation
The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any byte from 0C0h-0FFh. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Interrupts
The RTC includes three separate, fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from one-per-second to one-a-day. The periodic interrupt may be selected for rates from one-half second to 30.517 µs. The update-ended interrupt may be used to indicate to the program that an update cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a 1 to a interrupt enable bit permits that interrupt to be initiated when the event occurs. A 0 in the interrupt enable bit prohibits the –RTCIRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the –RTCIRQ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts. The flags are cleared by a read of Register C.

When an interrupt event occurs, a flag bit is set to a 1 in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independently of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

Divider Control
The divider control bits are fixed for only 32.768 kHz operation. The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one-half second later. The divider control bits are also used to facilitate testing the VL82C107.

Square Wave Output Selection
This version of the VL82C107 does not support the square wave output function.

Periodic Interrupt Selection
The periodic interrupt allows the –RTCIRQ pin to be triggered from once every 500 ms to once every 30.517 µs. The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Update Cycle
The VL82C107 executes an update cycle one-per-second, assuming one of the proper time bases is in place, the DV2-DV0 divider is not clear, and the SET bit in Register B is clear. The SET bit in the 1 state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 32.768 kHz time base, the update cycle takes 1984 µs, during which the time, calendar, and alarm bytes are not accessible by the processor program. The VL82C107 protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete, the output will be undefined. The update-in-progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating non-availability during an update cycle are useable by the program. In discussing the three methods, it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes high, the update cycle begins 244 µs later. Therefore, if a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. If a 1 is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C.

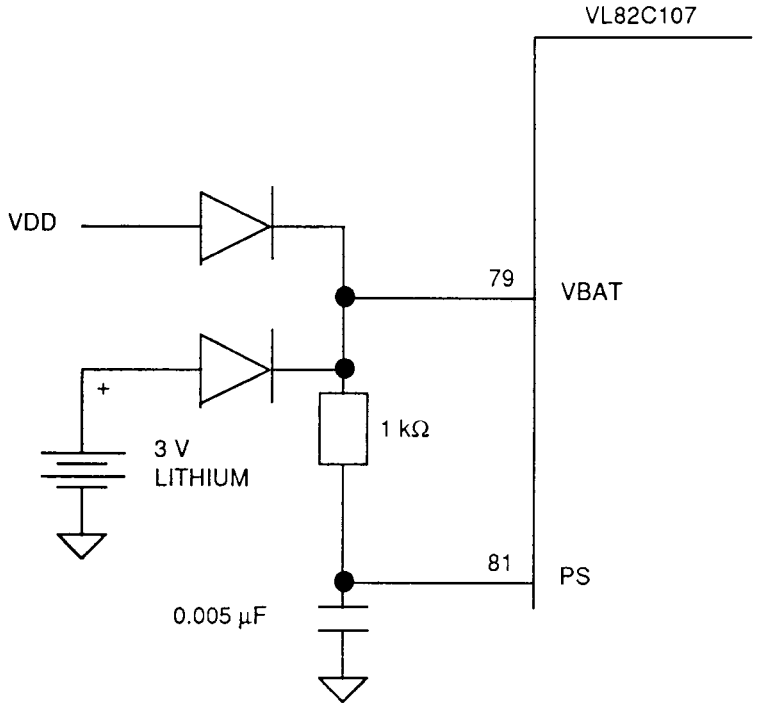
To properly setup the internal counters for daylight savings time operation, the user must set the time at least two seconds before the roll-over will occur. Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

Power-Down Mode
The passive components that are critical for low-power operation are shown in Figure 4.

The power-sense (PS) signal is used to reset the state of the valid RAM and time (VRT) bit. This input must be asserted after power is applied to the RTC to set the state of the VRT bit properly.

With a power consumption target specification of 5 µA, and a lithium battery with a capacity of 100 mA-hr, time will be properly kept for approximately 2.25 years.

FIGURE 4. POWER-DOWN MODE



IN-CIRCUIT TEST MODE

The VL82C107 is designed to make system board testing as easy as possible. When the –CE/–CS0/–TRI input is held low at POR (power-on reset, i.e., the falling edge of RSTDRV), it causes all pins on the VL82C107 to go to a high impedance state. This can be used to electrically isolate the VL82C107 so other components in the system can be tested.

The VL82C107 can also be set into a special test mode called In-Circuit Test (ICT) Mode. The purpose of ICT is not to test the VL82C107 functionally while it is inserted in a circuit board, but to test that the part is connected correctly and all the pins can be toggled high and low in a predictable pattern. This will catch solder joint or interconnect failures which could occur during the board manufacturing process. ICT Mode uses a multiplexing scheme between inputs and outputs to allow easy access and testing of each pin.

In order to activate the ICT Mode, the VL82C107 must first be placed in the high impedance state at POR, as described above. Then both –IOR and –IOW must be pulsed low while 06h is driven onto the SD bus. The address driven onto the A bus at this time does not matter. Standard read/write timings apply. At the trailing (rising) edge of –IOR and –IOW the VL82C107 will be placed into ICT Mode. Exit from ICT Mode is accomplished by a normal reset with RSTDRV.

Once in ICT Mode, the inversion of the ICT inputs listed in the following table directly drive the corresponding ICT output.

TABLE 14. IN-CIRCUIT TEST MODE

ICT Input		ICT Output		ICT Input		ICT Output	
Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
KI2	1	MCLK/KSRE	2	A21	67	LA21	66
KI3	3	KI0	4	A22	69	LA22	68
KI5	5	KI1	6	A23	71	LA23	70
KRSEL	7	MIRQ	9	HLDA	73	–DACK7	94
–IOR	11	–BHE	14	–MASTER	74	–DACK5	92
–EALE	13	–SBHE	15	–REFRESH	75	OSC	116
–IOW	10	A1	17	RSTDRV	76	–DACK6	93
SA0	12	SA1	18	XTALIN	77	XTALOUT	78
A2	19	SA2	20	PS	81	–RTCIRQ	80
A3	21	SA3	22	–DKEN	83	–DACK2	90
A4	23	SA4	24	DK0	84	–DACK0	87
A5	26	SA5	27	DK1	85	–DACK3	91
A6	28	SA6	29	DK2	86	–DACK1	89
A7	30	SA7	31	SD6	97	SD7	95
A8	33	SA8	34	SD4	99	SD5	98
A9	35	SA9	36	SD2	101	SD3	100
A10	37	SA10	38	SD0	103	SD1	102
A11	39	SA11	40	–IDENL	106	–IDECS1	105
A12	42	SA12	43	–BUSY	107	–MCS16	108
A13	44	SA13	45	–WP	109	–CE2	110
A14	46	SA14	47	–CD0	111	–CE1	113
A15	49	SA15	50	–IDENH	115	REG	114
A16	51	SA16	52	OSCI	117	OSCO	118
A17	54	LA/SA17	53/55	KKSW	119	KDAT	121
A18	58	LA/SA18	57/59	KCM	122	KA20	123
A19	61	LA/SA19	60/62	KCLK	124	KRES	125
A20	64	LA20	63	MDAT/KHSE	126	KIRQ	127

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
I/O Read/Write					
t5	Command Pulse Width	125		ns	
tSU6	Write Data Setup	60		ns	
tH7	Write Data Hold	20		ns	
tD8	Read Data Delay	0	130	ns	CL = 200 pF
tH9	Read Data Hold	5	60	ns	CL = 50 pF
WC	Write Cycle	280		ns	
RC	Read Cycle	280		ns	
tSU1	Address Valid to –EALE Rising	23		ns	
tSA	SA Valid from –EALE Rising		35	ns	
tLA	Address Valid to LA Valid		35	ns	
Chip Select Timing					
tD11	Chip Select Delay from SA Valid		35	ns	CL = 50 pF
–IOCS16 Timing					
tD13	–IOCS16 Active from SA Valid		60	ns	CL = 200 pF
tD17	–IOCS16 Inactive from Command		55	ns	CL = 200 pF
IDE Interface Timing					
tD19	IDENH/IDENL Delay from Address		60	ns	CL = 50 pF
tD20	IDED7 Delay from SD7 Input		40	ns	CL = 200 pF
tD21	SD7 Delay from IDED7 Input		40	ns	CL = 200 pF
tD23	SD7 Delay from –IOR During IDE Access	0	85	ns	CL = 200 pF

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
IDE Interface Timing (Cont.)					
tD24	SD7 Hold from –IOR Inactive	5	60	ns	CL = 50 pF
tD25	IDED7 Delay from –IOR Inactive	0	85	ns	CL = 200 pF
tD26	IDED7 Hold from –IOR Active	5	60	ns	CL = 50 pF
Real-Time Clock Timing					
tPSPW	Power-Sense Pulse Width	2		µs	
tPSP	Power-Sense Delay	2		µs	
tVRTD	VRT Bit Delay		2	µs	
–MCS16 Timing					
tDMC	–MCS16 Active from LA Valid		10	ns	
Master Mode Bus Timing					
tAM	A Bus Valid from SA/LA Input (Master Mode)		15	ns	

FIGURE 5. WRITE CYCLE

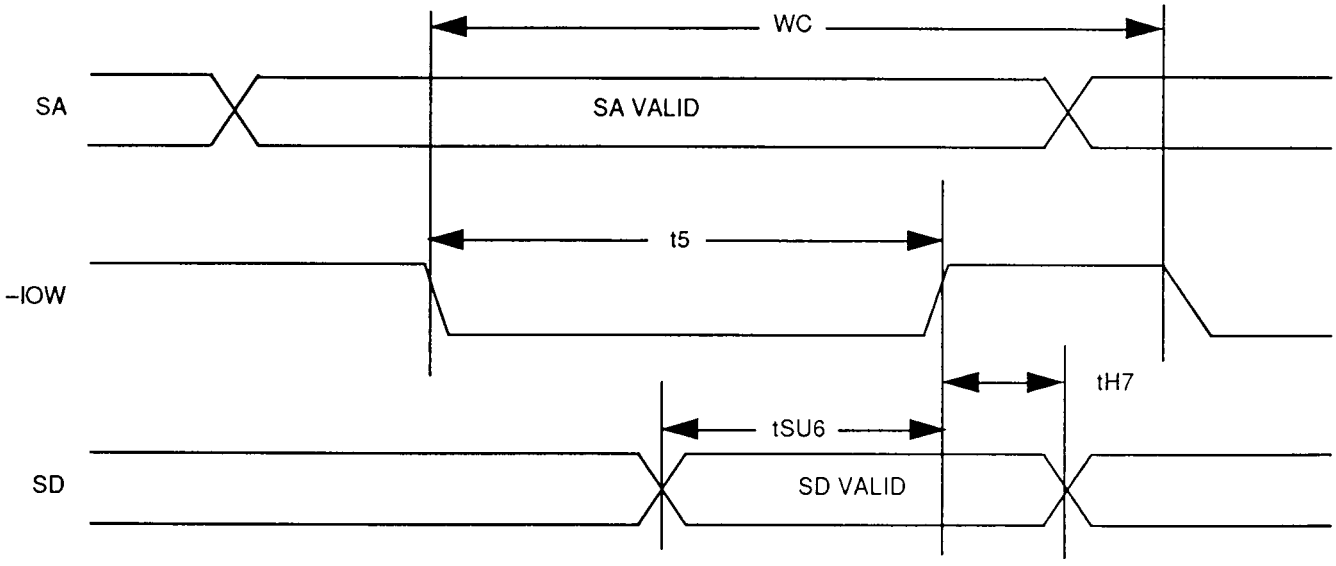


FIGURE 6. WRITE CYCLE

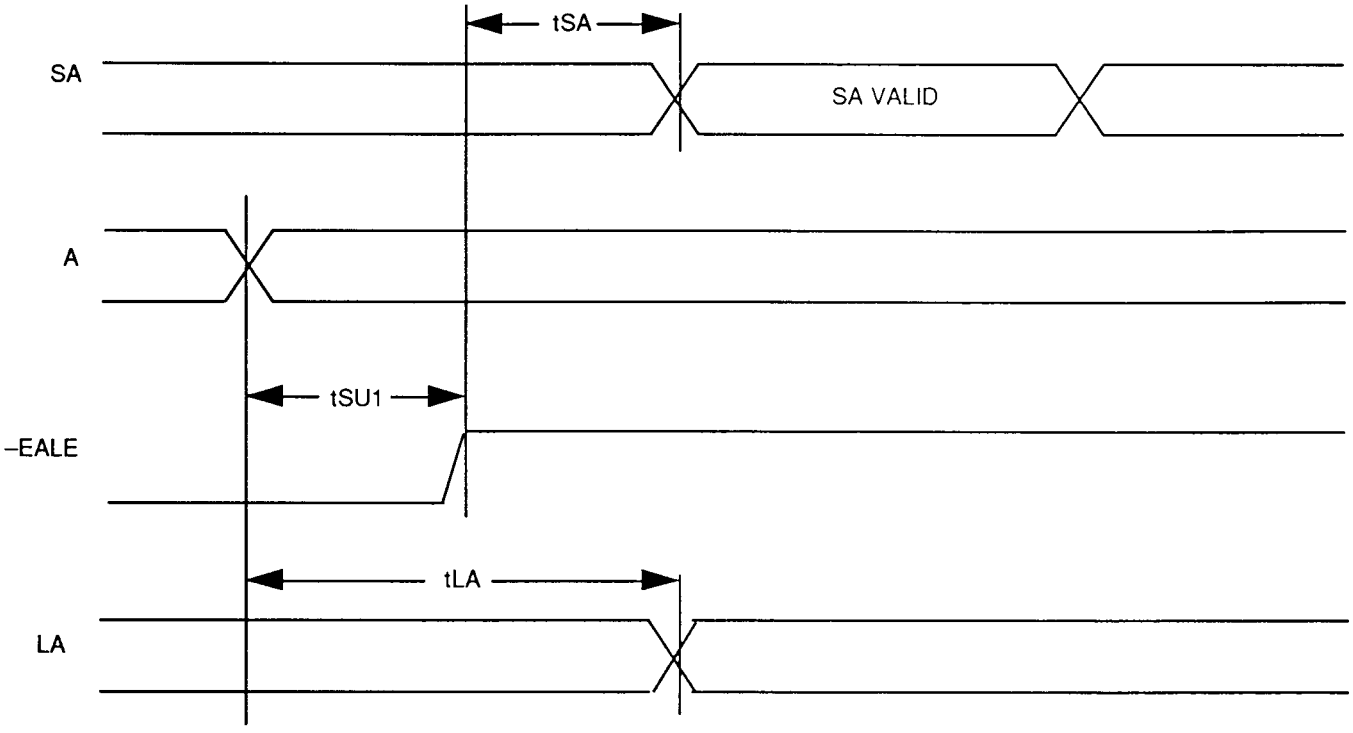


FIGURE 7. READ CYCLE

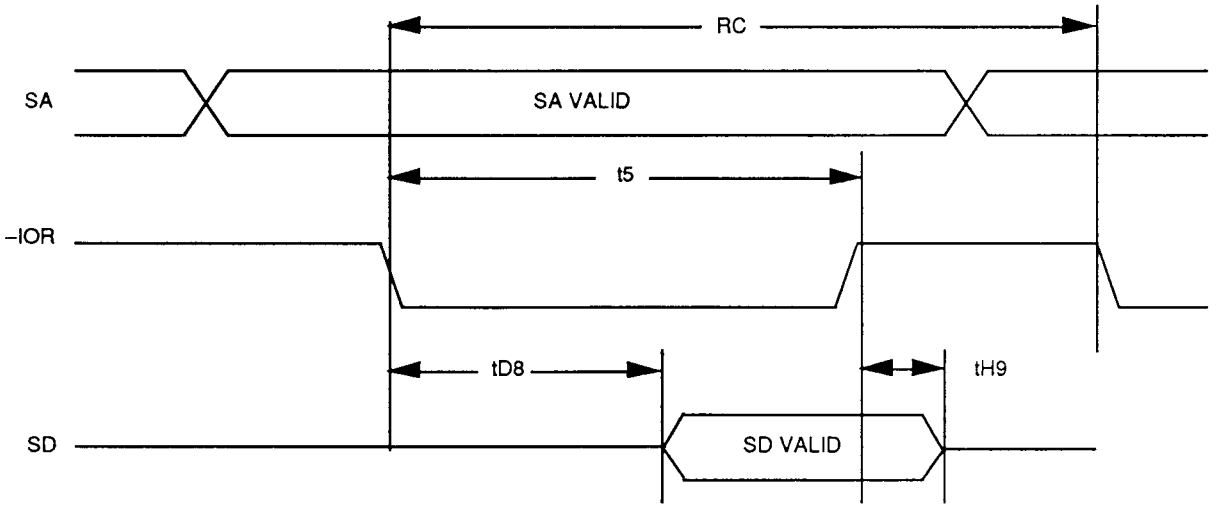


FIGURE 8. CHIP SELECT TIMING

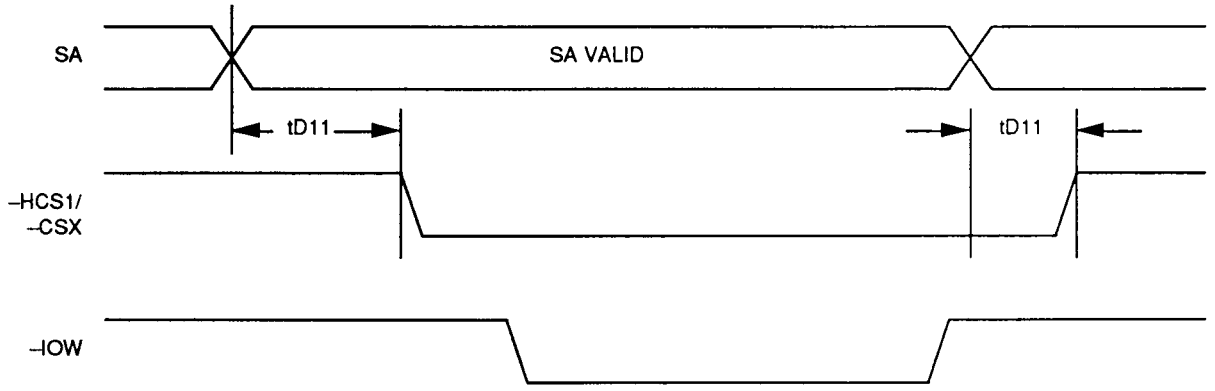


FIGURE 9. MASTER MODE BUS TIMING

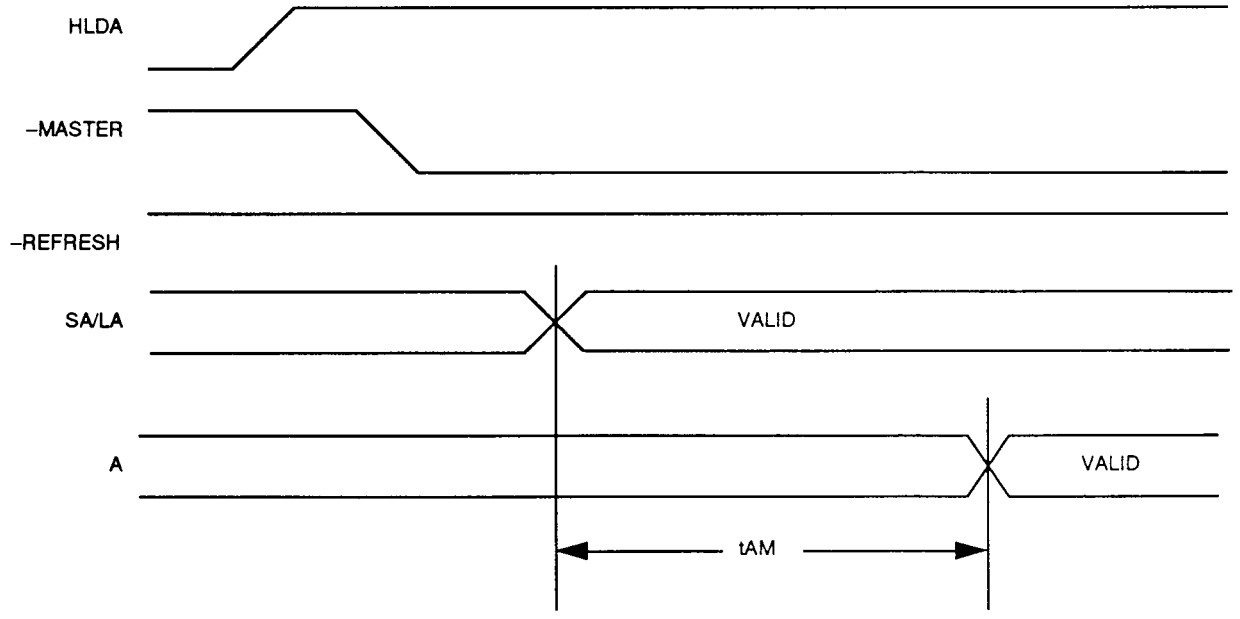


FIGURE 10. –MCS16/–IOCS16 TIMING

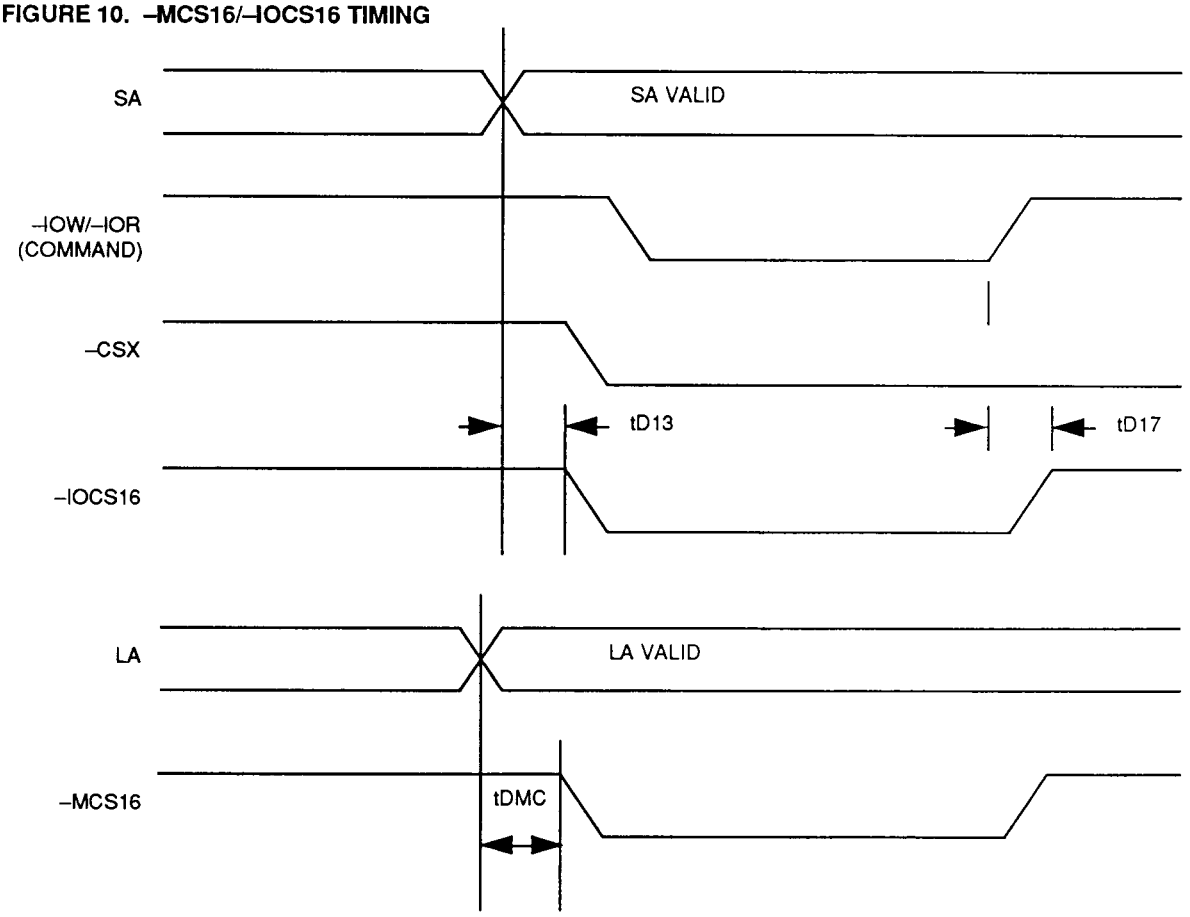


FIGURE 11. IDE INTERFACE TIMING

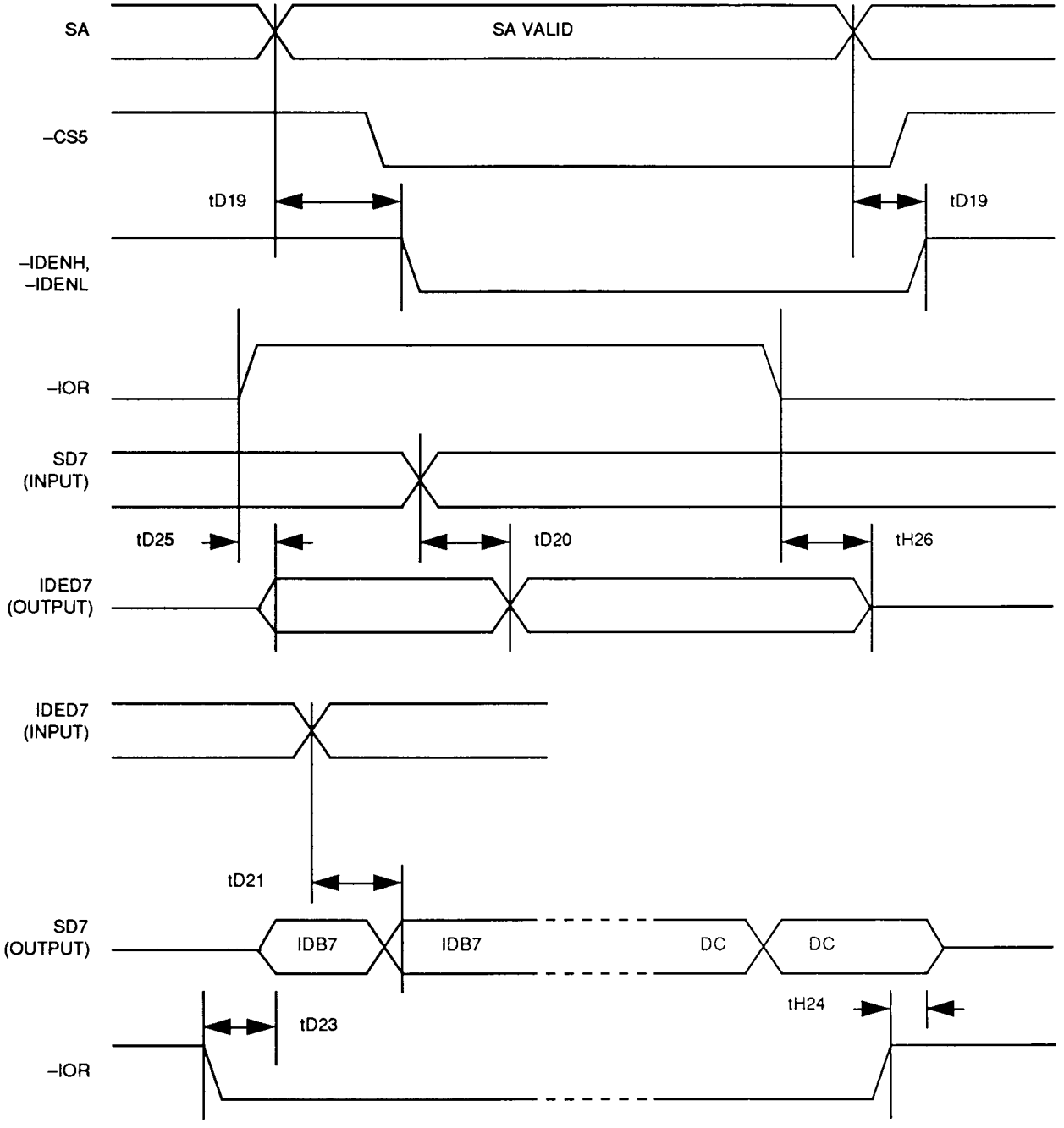
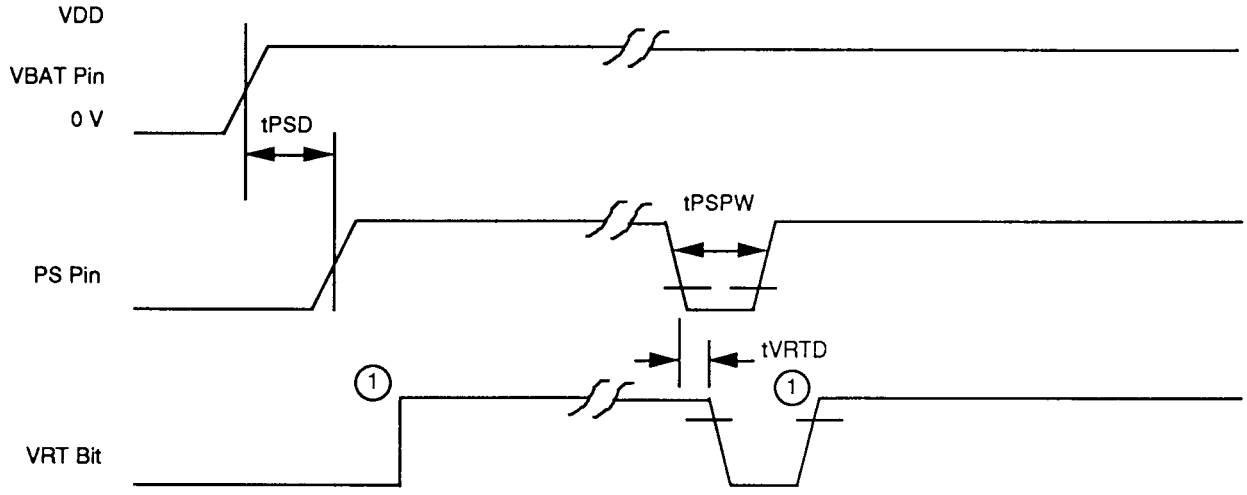
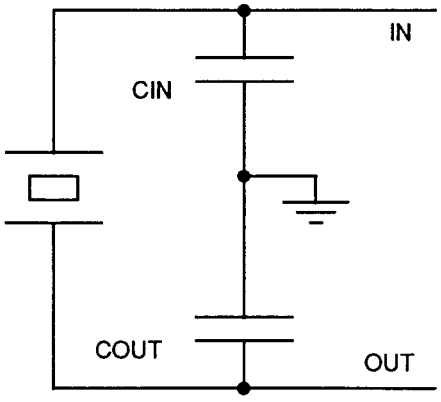


FIGURE 12. REAL-TIME CLOCK TIMING



(1). The VRT bit is set to a "1" by reading Register D. The VRT bit can only be cleared by pulling the PS pin low (see REGISTER D ($0D)).

CRYSTAL OSCILLATOR CONFIGURATIONS



32.768 kHz

CIN = COUT = 10-22 pF
CIN may be a trimmer for precision timekeeping applications

14.3181 MHz

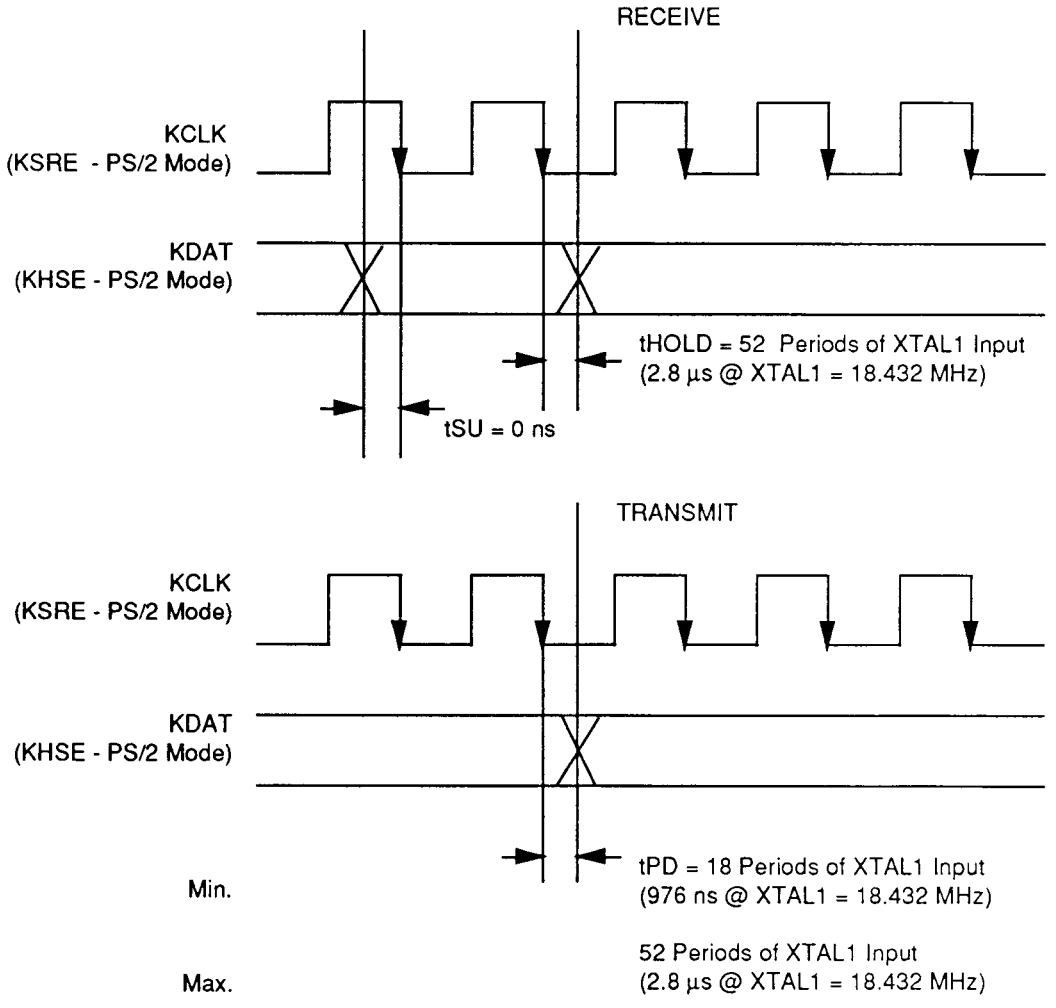
CIN = 10 pF
COUT = 30 pF

RECOMMENDED CRYSTAL PARAMETERS

Rs (max) ≤ 40k Ω
Co (max) ≤ 1.7 pF
CI (max) ≤ 12.5 pF
Parallel Resonance

Rs ≤ 50 Ω
Co ≤ 7 pF
CI ≤ 20 pF
Parallel Resonance

FIGURE 13. KEYBOARD CONTROLLER TIMING



ABSOLUTE MAXIMUM RATINGS

Ambient Temperature −10°C to +70°C

Storage Temperature −65°C to +150°C

Supply Voltage to Ground Potential −0.5 V to VDD + 0.3 V

Applied Output Voltage −0.5 V to VDD + 0.3 V

Applied Input Voltage VDD + 0.5 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
VIL	Input Low Voltage	−0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0 2.4	VDD + 0.5 VDD + 0.5	V V	TTL Level Inputs, Note 1 TTL Level Inputs, Note 2
VOL	Output Low Voltage		0.4 0.4 0.4 0.4	V V V V	IOL = 4.0 mA, Note 3 IOL = 8.0 mA, Note 4 IOL = 12.0 mA, Note 5 IOL = 24.0 mA, Note 6
VOH	Output High Voltage	2.4 2.4 2.4		V V V	IOH = 0.8 mA, Note 3 IOH = 1.4 mA, Note 4 IOH = 2.4 mA, Note 6
IIH	Input High Current		10	µA	VIN = VDD, Note 7
IIL	Input Low Current	−10 −500	 −50	µA µA	VIN = VSS + 0.2 V, Note 8 VIN = 0.8 V, Note 9
ILOL	Three-state Leakage Current	−50	 50	µA µA	VOUT = VSS + 0.2 V, Note 10 VOUT = VDD, Note 11
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
IDD	Operating Supply Current		40	mA	
IBAT	Supply Current, Standby Mode		5 50	µA µA	VBAT = 2.4 V VBAT = 5.0 V

(Notes on next page.)

DC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

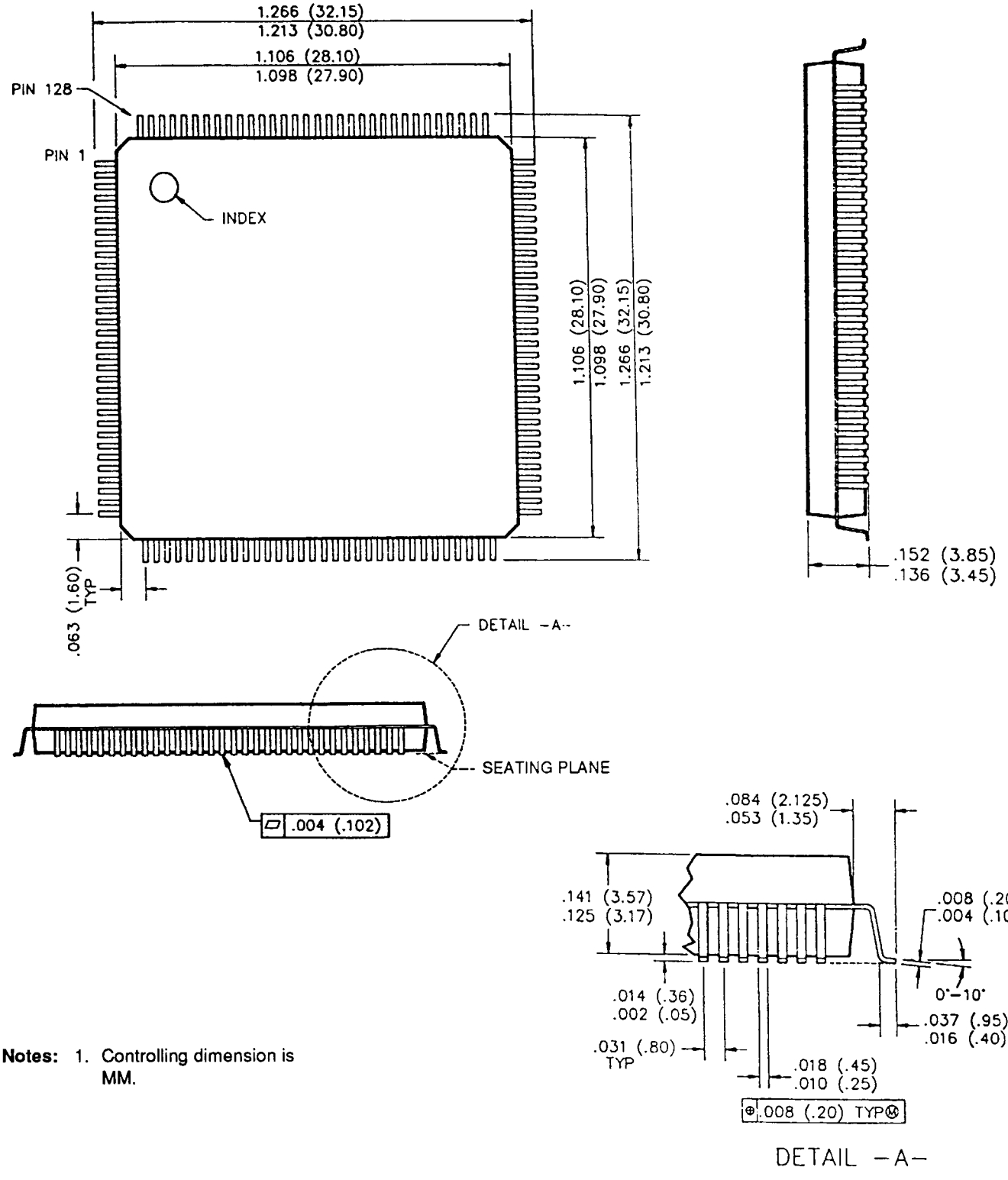
Notes:

1. Pins: KI2, KI3, KI0, KI5, KI1, KRSEL, –IOW, –IOR, SA0, –EALE, –BHE, –SBHE, A23-A1, SA19-SA1, LA23-LA17, HLDA, –MASTER, –REFRESH, –DKEN, DK2-DK0, SD7-SD0, –CD1/–IDECS1, BVD1/–IDENL, –BUSY/–IDECS0, WP/–FDCCS, –CD0/IDED7, –CE1/–CS0/–TRI, BVD2/–IDENH, KKSW, KCM, KA20/–SLP, KRES, KIRQ.
2. Pins: KSRE, RSTDRV, PS, KDAT, KCLK, KHSE.
3. Pins: MIRQ, KA20/–SLP, KRES, KIRQ.
4. Pins: KI0, KI1, –BHE, A23-A1, –DACK3 - –DACK0, –DACK7 - –DACK5, –CD1/–IDECS1, BVD1/–IDENL, –BUSY/–IDECS0, WP/–FDCCS, –CE2/–CS1, –CE1/–CS0/–TRI, REG/–CS2, BVD2/–IDENH.
5. Pins: KSRE, KDAT, KCLK, KHSE, –RTCIRQ (–SBHE, SA19-SA1, LA23-LA17 in low drive mode only*).
6. Pins: –SBHE, SA19-SA1, LA23-LA17, SD7-SD0, –MCS16/–IOCS16, –CD0/IDED7, OSC.
7. Pins: KI2, KI3, KI5, KRSEL, –IOW, –IOR, SA0, –EALE, HLDA, –MASTER, –REFRESH, RSTDRV, PS, –DKEN, DK2-DK0, KKSW, KCM.
8. Pins: –IOW, –IOR, SA0, –EALE, HLDA, –MASTER, –REFRESH, RSTDRV, PS, –DKEN, DK2-DK0.
9. Pins: KI2, KI3, KI0, KI5, KI1, KRSEL, –RTCIRQ, –CD1/–IDECS1, –BUSY/–IDECS0, WP/–FDCCS, –CD0/IDED7, –CE1/–CS0/–TRI, KKSW, KCM, KA20/–SLP, KRES, KIRQ, –CE2/–CS1*.
10. Pins: KSRE, MIRQ, –BHE, –SBHE, A23-A1, SA19-SA1, LA23-LA17, –RTCIRQ, –DACK7 - DACK5, –DACK3 - –DACK0, SD7-SD0, BVD1/–IDENL, –MCS16/–IOCS16, –CE2/–CS1, BVD2/–IDENH, KDAT, KCLK, KHSE.
11. Pins: KSRE, KI0, KI1, MIRQ, –BHE, –SBHE, A23-A1, SA19-SA1, LA23-LA17, –RTCIRQ, –DACK3 - –DACK0, –DACK7 - –DACK5, SD7-SD0, –CD1/–IDECS1, BVD1/–IDENL, –BUSY/–IDECS0, –MCS16/–IOCS16, WP/–FDCCS, –CE2/–CS1, –CD0/IDED7, –CE1/–CS0/–TRI, BVD2/–IDENH, KDAT, KA20/–SLP, KCLK, KRES, KHSE, KIRQ.

*Only applies to parts that were manufactured after January 1992.

PACKAGE OUTLINE

128-PIN METRIC (PLASTIC) QUAD FLAT PACK



Notes: 1. Controlling dimension is MM.

VLSI CORPORATE OFFICES

CORPORATE HEADQUARTERS • COMMUNICATIONS PRODUCTS DIVISION AND SPECIAL PRODUCTS DIVISION
VLSI Technology, Inc. • 1109 McKay Drive • San Jose, CA 95131 • 408-434-3100

PERSONAL COMPUTER PRODUCTS DIVISION, GOVERNMENT PRODUCTS DIVISION AND AUTOMOTIVE OPERATIONS
VLSI Technology, Inc. • 8375 South River Parkway • Tempe, AZ 85284 • 602-752-8574

VLSI SUBSIDIARY

COMPASS DESIGN AUTOMATION
1865 Lundy Avenue • San Jose, CA 95131 • 408-433-4880

VLSI SALES OFFICES AND TECH CENTERS

ARIZONA
8375 South River Parkway
Tempe, AZ 85284
602-752-6450
FAX 602-752-6001

CALIFORNIA
2235 Qume Dr
San Jose, CA 95131
408-922-5200
FAX 408-943-9792
Mail:
1109 McKay Drive
San Jose, CA 95131

6345 Balboa Blvd.,
Building 1, Suite 100
Encino, CA 91316
818-609-9981
FAX 818-609-0535

30 Corporate Park,
Stes. 100-102
Irvine, CA 92714
714-250-4900
FAX 714-250-9041

FLORIDA
2200 Park Central N., Ste. 600
Pompano Beach, FL 33064
305-971-0404
FAX 305-971-2086

GEORGIA
2400 Pleasant Hill Rd., Ste 200
Duluth, GA 30136
404-476-8574
FAX 404-476-3790

ILLINOIS
3100 Higgins Rd., Ste. 155
Hoffman Estates, IL 60195
708-884-0500
FAX 708-884-9394

MARYLAND
8424 Veterans Highway
Millersville, MD 21108
301-987-8777
FAX 301-987-4489

MASSACHUSETTS
261 Ballardvale St.
Wilmington, MA 01887
508-658-9501
FAX 508-657-6420

NEW JERSEY
311C Enterprise Dr.
Plainsboro, NJ 08536
609-799-5700
FAX 609-799-5720

NORTH CAROLINA
1000 Park Forty Plaza, Ste. 300
Durham, NC 27713
919-544-1891/92
FAX 919-544-6667

TEXAS
850 E. Arapaho Rd., Ste. 270
Richardson, TX 75081
214-231-6716
FAX 214-669-1413

WASHINGTON
405 114th Ave. SE, Ste. 300
Bellevue, WA 98004
206-453-5414
FAX 206-453-5229

FRANCE
2, Allee des Garays
F-91124 Palaiseau Cedex
France
1-69 93 26 00
FAX 1-64 47 04 80

GERMANY
Rosenkavalierplatz 10
D-8000 Muenchen 81
Germany
89-92795-0
FAX 89-92795-145

HONG KONG
Shui On Centre 1504-07
6-8 Harbour Road
Wanchai, Hong Kong
852-802-7755
FAX 852-802-7959

ITALY
Italia S.R.L.
Centro Direzionale Colleoni
Palazzo Cassiopeia, 3
I-20041 Argrate Brianza (MI)
39-6056791
FAX 39-6056808

JAPAN
Shuwa-Kioicho TBR Bldg., #101
Kojimachi 5-7, Chiyoda-Ku
Tokyo, Japan 102
03-3239-5211
FAX 03-3239-5215

Shinsaibashi MID Bldg., 7F
Minami Senba 3-2-29
Chuo-ku, Osaka, 542, Japan
06-243-6041
FAX 06-243-6960

TAIWAN
Unit 7, 7th Floor, Lotus Bldg.
136 Jen-Ai Rd., Section 3
Taipei, Taiwan, R.O.C.
886-2-325-4422
FAX 886-2-325-4411

UNITED KINGDOM
486-488 Midsummer Blvd.
Saxon Gate West, Central Milton
Keynes, MK9 2EQ
United Kingdom
09 08/66 75 95
FAX 09 08/67 00 27

VLSI SALES OFFICES

ALABAMA
2614 Artie St., Ste. 36
Huntsville, AL 35805
205-539-5513
FAX 205-536-8622

CONNECTICUT
850 North Main St., Bldg. 1, 2C
Wallingford, CT 06492
203-265-6698
FAX 203-265-3653

FLORIDA
5955 T. G. Lee Blvd., Ste. 170
Orlando, FL 32822
407-240-9604
FAX 407-855-2595

MINNESOTA
5831 Cedar Lake Rd.
St. Louis Park, MN 55416
612-545-1490
FAX 612-545-3489

NEW YORK
820 Cross Keys Office Park
Fairport, NY 14450
716-223-0590
FAX 716-425-1112

OHIO
4 Commerce Park Square
23200 Chagrin Blvd., Ste.600
Cleveland, OH 44122
216-292-8235
FAX 216-464-7609

OREGON
10300 S.W. Greenburg Rd.,
Ste. 478
Portland, OR 97223
503-244-9882
FAX 503-245-0375

TEXAS
9600 Great Hills Trail,
Ste. 150W
Austin, TX 78759
512-343-8191
FAX 512-343-2759

JAPAN
Shuwa-Kioicho Park Bldg., #503
Kioicho 3-6, Chiyoda-Ku
Tokyo, Japan 102
03-3262-0850
FAX 03-3262-0881

SINGAPORE
20 Jalan Afifi #04-01
Cisco Centre
Singapore 1440
65-742-2314
FAX 65-742-1768

VLSI AUTHORIZED DESIGN CENTERS

COLORADO
SIS MICROELECTRONICS, INC.
Longmont, 303-776-1667

ILLINOIS
ASIC DESIGNS
Naperville, 708-717-5841

MAINE
QUADIC SYSTEMS, INC.
South Portland, 207-871-8244

PENNSYLVANIA
INTEGRATED CIRCUIT
SYSTEMS, INC.
King of Prussia, 215-265-8690

CANADA
PACIFIC MICROELECTRONICS
CENTRE
British Columbia, 604-293-5755

EIRE AND U.K.
PA TECHNOLOGY
Herts, 76-261222

SYMBIONICS
Cambridge, 223-421025

FRANCE
CETIA
Toulon Cedex, 9-42-12005

SOREP
Chateaubourg, 99-623955

JAPAN
ADC CORPORATION
Tokyo, 03-3492-1251

LSI SYSTEMS, INC.
Kanagawa, 0462-29-3220

NIPPON STEEL CORPORATION
Tokyo, 03-5566-2141

KOREA
ANAM VLSI DESIGN CENTER
Seoul, 82-2-553-2106

NORWAY
NORKRETS AS
Oslo, 47-2360677/8

VLSI SALES REPRESENTATIVES

ARIZONA
LUSCOMBE ENGINEERING
Scottsdale, 602-949-9333

CALIFORNIA
CENTAUR CORP.
Irvine, 714-261-2123
Calabasas, 818-591-1655

EMERGING TECHNOLOGY
San Jose, 408-263-9366
Cameron Park, 916-676-4387

COLORADO
LUSCOMBE ENGINEERING
Longmont, 303-772-3342

IDAHO
EMERGING TECHNOLOGY
Boise, 208-378-4680

IOWA
SELTEC SALES
Cedar Rapids, 319-364-7660

KANSAS
ELECTRI-REP
Overland Park, 913-649-2168

MICHIGAN
APPLIED DATA MANAGEMENT
Westland, 313-427-8181

MISSOURI
ELECTRI-REP
St. Louis, 314-993-4421

NEW YORK
bbd ELECTRONICS
Rochester, 716-425-4101

OHIO
APPLIED DATA MANAGEMENT
Cincinnati, 513-579-8108

OREGON
ELECTRA TECHNICAL SALES
Beaverton, 503-643-5074

UTAH
LUSCOMBE ENGINEERING
Salt Lake City, 801-565-9885

WASHINGTON
ELECTRA TECHNICAL SALES
Kirkland, 206-821-7442

AUSTRALIA
GEORGE BROWN GROUP
Adelaide, 61-8-352-2222
Brisbane, 61-7-252-3876
Melbourne, 61-3-878-8111
Newcastle, 61-49-69-6399
Perth, 61-9-362-1044
Sydney, 61-2-638-1888

CANADA
DAVETEK MARKETING, INC.
Alberta, 403-291-4984
British Columbia, 604-430-3680

HHR ELECTRO REP
Ontario, 519-651-1050
Quebec, 514-739-7054

HONG KONG
LESTINA INTERNATIONAL, LTD
Tsimshatsui, 852-7351736

ISRAEL
RDT ELECTRONICS ENG. LTD
Tel-Aviv, 23-4832119

SINGAPORE
DYNAMIC SYSTEMS PTE, LTD
Singapore, 65-742-1986

TAIWAN
PRINCETON TECH CORP
Taipei, 886-2-917-8856

WEIKENG INDUSTRIAL CO
Taipei, 886-2-776-3998

THAILAND
TRON ELECTRONICS CO LTD
Bangkok, 66-2589863

VLSI DISTRIBUTORS

United States represented by
ARROW/SCHWEBER
except where noted

ALABAMA
Huntsville, 205-837-6955

ARIZONA
Phoenix, 602-431-0030

CALIFORNIA
Arrow Pacific, 408-432-7171
Los Angeles, 818-880-9686
Orange County, 714-838-5422
San Diego, 619-565-4800
San Francisco, 408-441-9700

COLORADO
Denver, 303-799-0258

CONNECTICUT
Wallingford, 203-265-7741

FLORIDA
North Florida, 407-333-9300
South Florida, 305-429-8200

GEORGIA
Atlanta, 404-497-1300

ILLINOIS
Chicago, 708-250-0500

INDIANA
Indianapolis, 317-299-2071

IOWA
Cedar Rapids, 319-395-7230

KANSAS
Kansas City, 913-541-9542

MARYLAND
Baltimore, 301-596-7800

MASSACHUSETTS
Boston, 508-658-0900

MICHIGAN
Detroit, 313-462-2290

MINNESOTA
Minnesota, 612-941-5280

MISSOURI
St. Louis, 314-567-6888

NEW JERSEY
Philadelphia, 609-596-8000
North Jersey, 201-227-7880

NEW YORK
Rochester, 716-427-0300
Metro, 516-231-1000

NORTH CAROLINA
Raleigh, 919-876-3132

OHIO
Dayton, 513-435-5563
Cleveland, 216-248-3990

OKLAHOMA
Tulsa, 918-252-7537

OREGON
ARROW/ALMAC
Portland, 503-629-8090

PENNSYLVANIA
Pittsburgh, 412-963-6807

TEXAS
Austin, 512-835-4180
Dallas, 214-380-6464
Houston, 713-530-4700

UTAH
Salt Lake City, 801-973-6913

WASHINGTON
ARROW/ALMAC
Seattle, 206-643-9992
Spokane, 509-924-9500

WISCONSIN
Milwaukee, 414-792-0150

AUSTRIA
THOMAS NEUROTH
Wien, 222-825645

BELGIUM/LUXEMBURG
MICROTRON
Mechelen, 215-212223

CANADA
ARROW/SCHWEBER
Montreal, 514-421-7411
Ottawa, 613-226-6903
Toronto, 416-670-7769
Vancouver, 604-421-2333

SEMAD
Calgary, 403-252-5664
Markham, 416-475-8500
Montreal, 514-694-0860
Ottawa, 613-727-8325
British Columbia, 604-420-9889

DENMARK
DELCO
Allerod, 42-277733

ENGLAND
HAWKE COMPONENTS
Bramley, NR Basingstoke
256-880800

KUDOS-THAME LTD
Berks, 734-351010

QUARNDON ELECTRONICS
Derby, 332-32651

FINLAND
COMDAX
Helsinki, 80-670277

FRANCE
ASAP s.a.
Montigny-le-Bretonneux,
1-30438233

GERMANY
DATA MODUL GmbH
Muenchen, 89-560170

BIT-ELECTRONIC AG
Muenchen, 89-4180070

ITALY
INTER-REP S.P.A.
Torino, 11-2165901

JAPAN
ASAHI GLASS CO. LTD
Tokyo, 03-3218-5854

TOKYO ELECTRON, LTD
Tokyo, 03-3340-8111

TOMEN ELECTRONICS
Tokyo, 03-3506-3650

NETHERLANDS
TME
Aa Heeswijk-Dinther,
4139-8895

PUERTO RICO
ISLA CARIBE ELECTRO SALES
Guaynabo, 809-720-4430

SWEDEN
TRACO AB
Farsta, 8-930000

SPAIN AND PORTUGAL
SEMICONDUCTORES s.a.
Barcelona, 3-21723 40

SWITZERLAND
DECTRO SWISS AG
Zuerich, 1-3868600

3091

8350-195107-001 5M 12/91