Advance Data Sheet, Rev. 5
March 2000

microelectronics group

Lucent Technologies
Bell Labs Innovations

UNIVERSAL SERIAL BUS

USS-312
Two-Port PCI-to-USB OpenHCI Host Controller

Features

- 32-bit, 33 MHz PCI interface compliant with *PCI Local Bus Specification Revision 2.1s*
- Two downstream USB ports
- Full compliance with *Universal Serial Bus Specification Revision 1.1*
- *OpenHCI Open Host Controller Interface Specification for USB Release 1.0a* compatible
- Provides advanced power management capabilities compliant with *PCI Bus Power Management Interface Specification Revision 1.1*
- Fully compatible with *Microsoft Windows** Standard OpenHCD Drivers
- Supports legacy keyboard and mouse devices
- Integrated dual-speed USB transceivers
- 3 V or 5 V switchable PCI signaling
- Part of Lucent USB *Silicon Suite*® technology family
- 100-pin MQFP and 100-pin TQFP
- Evaluation kit available

Applications

- Seamless integration with 3 V or 5 V PCI-based computer products
- Supports all USB compliant devices and hubs

Description

Lucent Technologies Microelectronics Group's USS-312 provides a single-chip PCI-to-Universal Serial Bus (USB) solution. The USS-312 interfaces directly to any 32-bit 33 MHz PCI bus and is ideal for either onboard applications or add-in card applications. It can easily be configured to communicate in either a 3 V PCI environment or 5 V PCI environment simply by selecting the appropriate communications voltage level on the VIO input pin.

The USS-312 provides two downstream USB ports for connectivity with any USB compliant device or hub. Full-speed or low-speed peripherals are supported along with all of the USB transfer types: control, interrupt, bulk, or isochronous. The USS-312's OpenHCI compliance offers significant USB performance benefits and reduced CPU overhead compared to other host controllers.

The USS-312 is fully compatible with the *Microsoft Windows* Standard OpenHCD Drivers.

The USS-312 is a 3.3 V device fabricated in 0.35 µm technology. Integrated dual-speed USB transceivers enable a single-chip PCI-to-USB solution.

The USS-312 supports the legacy peripherals feature, as defined in the *OpenHCI Specification Release 1.0a*.

An advanced power management capabilities interface compliant with *PCI Bus Power Management Interface Specification Revision 1.1* is present to offer a variety of power-savings modes to the host system.

* *Microsoft* and *Windows* are registered trademarks of Microsoft Corporation.

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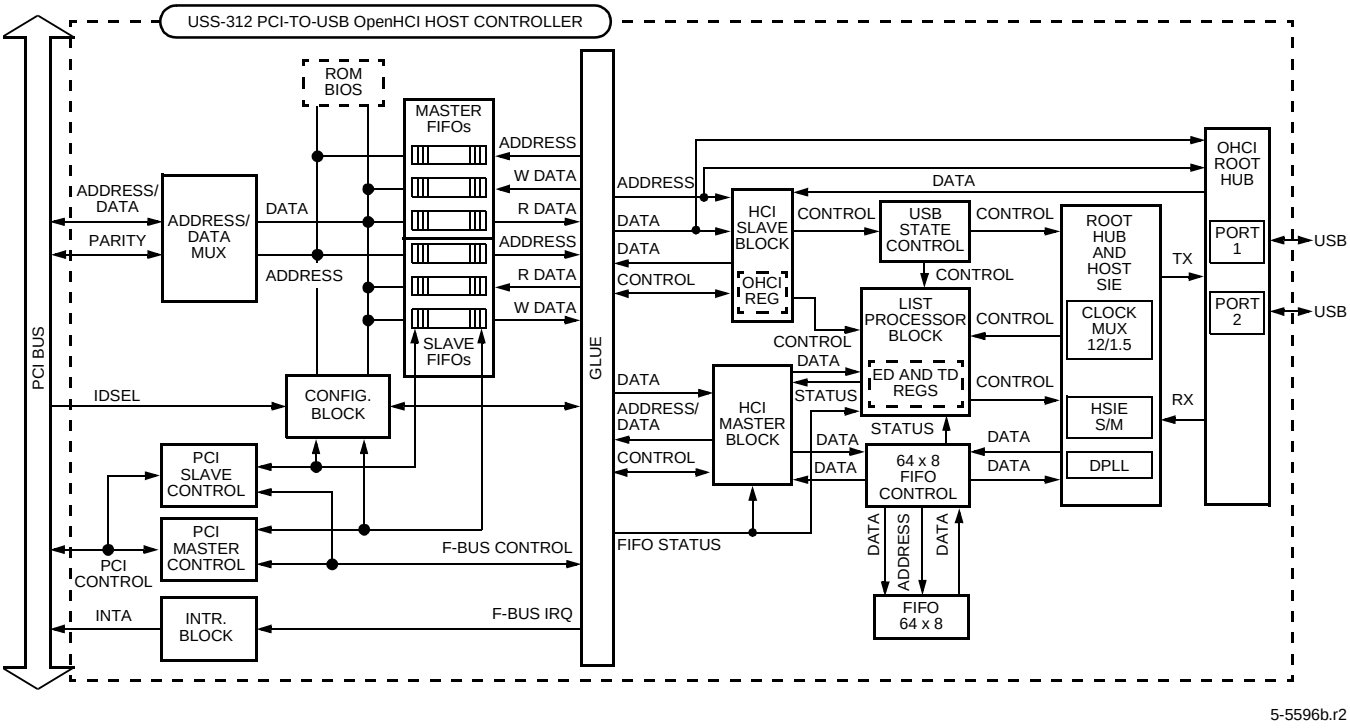

Figure 1. USS-312 Interconnection Diagram

Applicable Documents and Specifications

- *PCI Local Bus Specification Revision 2.1s.*, June 1, 1995. PCI Special Interest Group.
- *Universal Serial Bus Specification Revision 1.1.*, September 23, 1998. Compaq/Digital Equipment Corporation/ IBM PC Company/Intel/Microsoft/NEC/Northern Telecom.
- *OpenHCI Open Host Controller Interface Specification for USB Release 1.0a.*, July 31, 1997. Compaq/Microsoft/ National Semiconductor.
- *PCI Bus Power Management Interface Specification Revision 1.1.*, December 18, 1998. PCI Special Interest Group.

Pin Information

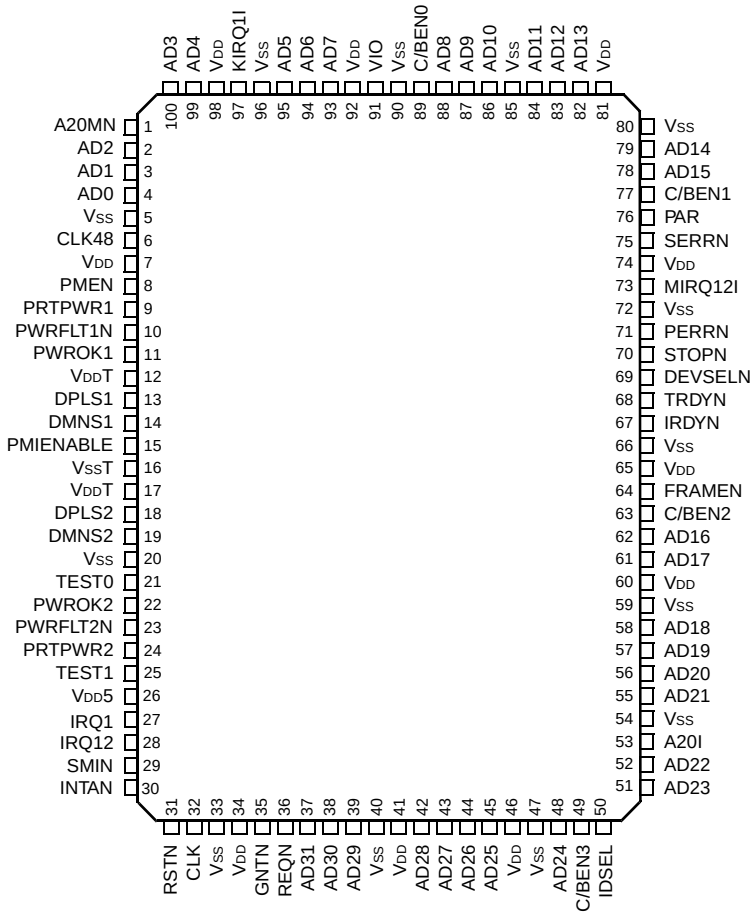

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Figure 2. Pin Diagram (100-Pin MQFP)

Pin Information (continued)

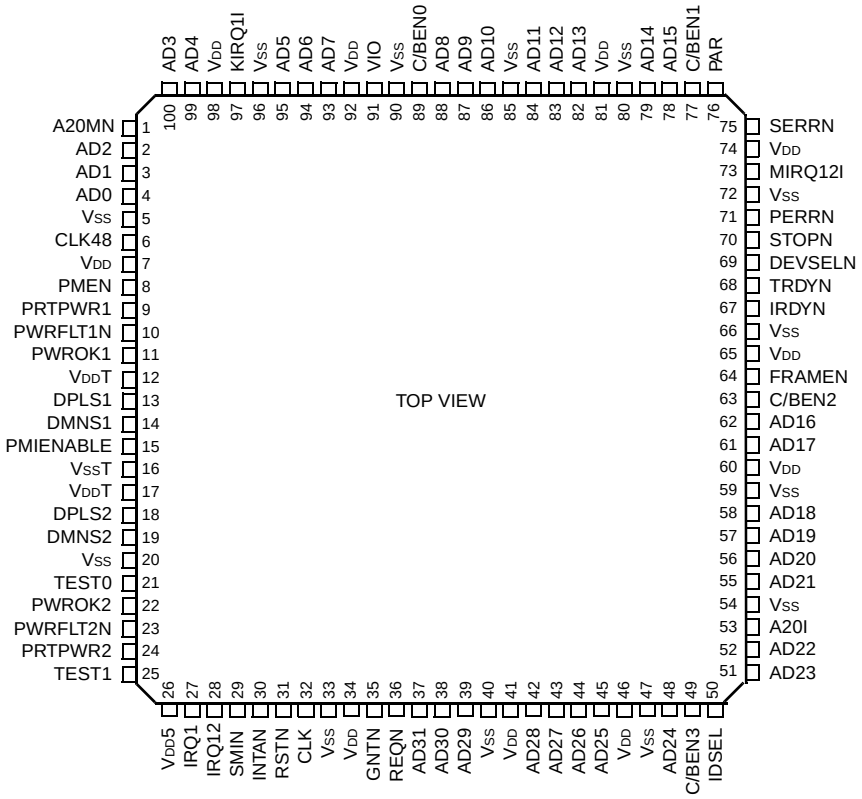

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Figure 3. Pin Diagram (100-Pin TQFP)

Pin Information (continued)

Table 1. Numeric Pin Cross Reference

Pin	Symbol*	Pin	Symbol*	Pin	Symbol*	Pin	Symbol*
1	A20MN	26	VDD5	51	AD23	76	PAR
2	AD2	27	IRQ1	52	AD22	77	C/BEN1
3	AD1	28	IRQ12	53	A20I	78	AD15
4	AD0	29	SMIN	54	VSS	79	AD14
5	VSS	30	INTAN	55	AD21	80	VSS
6	CLK48	31	RSTN	56	AD20	81	VDD
7	VDD	32	CLK	57	AD19	82	AD13
8	PMEN	33	VSS	58	AD18	83	AD12
9	PRTPWR1	34	VDD	59	VSS	84	AD11
10	PWRFLT1N	35	GNTN	60	VDD	85	VSS
11	PWROK1	36	REQN	61	AD17	86	AD10
12	VDDT	37	AD31	62	AD16	87	AD9
13	DPLS1	38	AD30	63	C/BEN2	88	AD8
14	DMNS1	39	AD29	64	FRAMEN	89	C/BEN0
15	PMIENABLE	40	VSS	65	VDD	90	VSS
16	VSST	41	VDD	66	VSS	91	VIO
17	VDDT	42	AD28	67	IRDYN	92	VDD
18	DPLS2	43	AD27	68	TRDYN	93	AD7
19	DMNS2	44	AD26	69	DEVSELN	94	AD6
20	VSS	45	AD25	70	STOPN	95	AD5
21	TEST0	46	VDD	71	PERRN	96	VSS
22	PWROK2	47	VSS	72	VSS	97	KIRQ1I
23	PWRFLT2N	48	AD24	73	MIRQ12I	98	VDD
24	PRTPWR2	49	C/BEN3	74	VDD	99	AD4
25	TEST1	50	IDSEL	75	SERRN	100	AD3

* Active-low signals within this document are indicated by an N following the symbol names.

Pin Information (continued)

Table 2. Pin Descriptions

Pin	Symbol*	Type	Description
1	A20MN	Output/Open Drain	**Legacy Gate A20 Output (Active-Low).**
2	AD2	Bidir	**PCI Address/Data Bit.**
3	AD1	Bidir	**PCI Address/Data Bit.**
4	AD0	Bidir	**PCI Address/Data Bit.**
5	V_{SS}	Power	**Device Ground.**
6	CLK48	Input	**USB Clock (48 MHz).**
7	V_{DD}	Power	**Device Power (3.3 V).**
8	PMEN	Output/Open Drain	**Power Management Event (Active-Low).**
9	PRTPWR1	Bidir	**Port 1 Power.** Logic output expected to turn on port 1 power. Bootstrap low for high active. Bootstrap high for low active.
10	PWRFLT1N	Input	**Port 1 Power Fault (Active-Low).** Logic input indicates an overcurrent fault on port 1.
11	PWROK1	Input	**Port 1 Power OK.** Analog or digital input to inform the USS-312 that USB port 1 power is stable (when >4 V).
12	V_{DD}T	Power	**Transceiver Power (3.3 V).**
13	DPLS1	Bidir	**DIfferential USB Port 1 Signals.**
14	DMNS1	Bidir	
15	PMIENABLE	Input	**Power Management Interface Enable Input (Active-High).**
16	V_{SS}T	Power	**Transceiver Ground.**
17	V_{DD}T	Power	**Transceiver Power (3.3 V).**
18	DPLS2	Bidir	**Differential USB Port 2 Signals.**
19	DMNS2	Bidir	
20	V_{SS}	Power	**Device Ground.**
21	TEST0	Input	**Test 0.** For device testing. Connect this to ground during normal use. Connect to logic high for NAND tree mode. See NAND Tree Mode on page 2-32.
22	PWROK2	Input	**Port 2 Power OK.** Analog or digital input to inform the USS-312 that USB port 2 power is stable (when >4 V).
23	PWRFLT2N	Input	**Port 2 Power Fault (Active-Low).** Logic input indicates an overcurrent fault on port 2.
24	PRTPWR2	Bidir	**Port 2 Power.** Logic output expected to turn on port 2 power. Bootstrap low for high active. Bootstrap high for low active.
25	TEST1	Input	**Test 1.** For device testing. Tie this to ground during normal use. Connect to logic high for NAND tree mode. See the NAND Tree Mode section on page 2-32.
26	V_{DD}5	Power	**5 V Power for 5 V PCI Operation.** 5 V must be present on this pin while selecting either 3 V PCI or 5 V PCI operation with the VIO pin. See PCI Connection Instructions section on page 2-26.
27	IRQ1	Output/Open Drain	**System Keyboard Interrupt (Active-High).**
28	IRQ12	Output/Open Drain	**System Mouse Interrupt (Active-High).**
29	SMIN	Output/Open Drain	**System Management Interrupt (Active-Low).**
30	INTAN	Output/Open Drain	**PCI Interrupt (Active-Low).**
31	RSTN	Input	**PCI Reset (Active-Low).** Also the chip reset.

* Active-low signals within this document are indicated by an N following the symbol names.

Pin Information (continued)

Table 2. Pin Descriptions (continued)

Pin	Symbol*	Type	Description
32	CLK	Input	**PCI Clock.** 33 MHz input clock.
33	VSS	Power	**Device Ground.**
34	VDD	Power	**Device Power (3.3 V).**
35	GNTN	Input	**PCI Grant Signal (Active-Low).**
36	REQN	Output/3-State	**PCI Request Signal (Active-Low).**
37	AD31	Bidir	**PCI Address/Data Bit.**
38	AD30	Bidir	**PCI Address/Data Bit.**
39	AD29	Bidir	**PCI Address/Data Bit.**
40	VSS	Power	**Device Ground.**
41	VDD	Power	**Device Power (3.3 V).**
42	AD28	Bidir	**PCI Address/Data Bit.**
43	AD27	Bidir	**PCI Address/Data Bit.**
44	AD26	Bidir	**PCI Address/Data Bit.**
45	AD25	Bidir	**PCI Address/Data Bit.**
46	VDD	Power	**Device Power (3.3 V).**
47	VSS	Power	**Device Ground.**
48	AD24	Bidir	**PCI Address/Data Bit.**
49	C/BEN3	Bidir	**PCI Command/Byte Enable.**
50	IDSEL	Bidir	**PCI ID Select.**
51	AD23	Bidir	**PCI Address/Data Bit.**
52	AD22	Bidir	**PCI Address/Data Bit.**
53	A20I	Input	**Legacy Gate A20 Input.**
54	VSS	Power	**Device Ground.**
55	AD21	Bidir	**PCI Address/Data Bit.**
56	AD20	Bidir	**PCI Address/Data Bit.**
57	AD19	Bidir	**PCI Address/Data Bit.**
58	AD18	Bidir	**PCI Address/Data Bit.**
59	VSS	Power	**Device Ground.**
60	VDD	Power	**Device Power (3.3 V).**
61	AD17	Bidir	**PCI Address/Data Bit.**
62	AD16	Bidir	**PCI Address/Data Bit.**
63	C/BEN2	Bidir	**PCI Command/Byte Enable.**
64	FRAMEN	Bidir	**PCI Frame (Active-Low).**
65	VDD	Power	**Device Power (3.3 V).**
66	VSS	Power	**Device Ground.**
67	IRDYN	Bidir	**PCI Initiator Ready (Active-Low).**
68	TRDYN	Bidir	**PCI Target Ready (Active-Low).**
69	DEVSELN	Bidir	**PCI Device Select (Active-Low).**
70	STOPN	Bidir	**PCI Stop (Active-Low).**
71	PERRN	Bidir	**PCI Parity Error (Active-Low).**
72	VSS	Power	**Device Ground.**
73	MIRQ12I	Input	**Legacy Mouse Controller Interrupt Input.**

* Active-low signals within this document are indicated by an N following the symbol names.

Pin Information (continued)

Table 2. Pin Descriptions (continued)

Pin	Symbol*	Type	Description
74	VDD	Power	**Device Power (3.3 V).**
75	SERRN	Output/Open Drain	**PCI System Error (Active-Low).**
76	PAR	Bidir	**PCI Parity.**
77	C/BEN1	Bidir	**PCI Command/Byte Enable.**
78	AD15	Bidir	**PCI Address/Data Bit.**
79	AD14	Bidir	**PCI Address/Data Bit.**
80	VSS	Power	**Device Ground.**
81	VDD	Power	**Device Power (3.3 V).**
82	AD13	Bidir	**PCI Address/Data Bit.**
83	AD12	Bidir	**PCI Address/Data Bit.**
84	AD11	Bidir	**PCI Address/Data Bit.**
85	VSS	Power	**Device Ground.**
86	AD10	Bidir	**PCI Address/Data Bit.**
87	AD9	Bidir	**PCI Address/Data Bit.**
88	AD8	Bidir	**PCI Address/Data Bit.**
89	C/BEN0	Bidir	**PCI Command/Byte Enable.**
90	VSS	Power	**Device Ground.**
91	VIO	Power	**Voltage I/O.** This signal is used to indicate to the USS-312 the PCI signaling interface to use (3 V or 5 V PCI signaling). A 3 V on VIO will indicate 3 V PCI signaling while 5 V on VIO will indicate 5 V PCI signaling. This pin may be connected directly to the PCI VIO signal.
92	VDD	Power	**Device Power (3.3 V).**
93	AD7	Bidir	**PCI Address/Data Bit.**
94	AD6	Bidir	**PCI Address/Data Bit.**
95	AD5	Bidir	**PCI Address/Data Bit.**
96	VSS	Power	**Device Ground.**
97	KIRQ1I	Input	**Legacy Keyboard Controller Interrupt Input.**
98	VDD	Power	**Device Power (3.3 V).**
99	AD4	Bidir	**PCI Address/Data Bit.**
100	AD3	Bidir	**PCI Address/Data Bit.**

* Active-low signals within this document are indicated by an N following the symbol names.

Register Overview

Table 3. PCI Bus Configuration Memory Summary

Refer to Tables 4—24 for more details on each of these registers.

Configuration Space Offset	Register Name	Read/Write	Default Value (Reset)
00h—01h	Vendor ID	R	11C1h
02h—03h	Device ID	R	5802h
04h—05h	Command	R/W	0000h
06h—07h	Status	R/W	0200h if PMIENABLE = 0b 0210h if PMIENABLE = 1b
08h	Revision ID*	R	11h = Revision B 10h = Revision C
09h—0Bh	Class Code	R	0C0310h
0Ch	Cache Line Size	R	00h
0Dh	Latency Timer	R/W	00h
0Eh	Header Type	R	00h
0Fh	BIST	R	00h
10h—13h	BAR 0	R/W	00000000h
14h—17h	BAR 1	R	00000000h
18h—1Bh	BAR 2	R	00000000h
1Ch—1Fh	BAR 3	R	00000000h
20h—23h	BAR 4	R	00000000h
24h—27h	BAR 5	R	00000000h
28h—2Bh	CardBus CIS Pointer	R	00000000h
2Ch—2Dh	Subsystem Vendor ID	R/W†	11C1h
2Eh—2Fh	Subsystem ID	R/W†	5802h
30h—33h	Expansion ROM Base Address	R	00000000h
34h	Capabilities Pointer	R	00h if PMIENABLE = 0b 50h if PMIENABLE = 1b
3Ch	Interrupt Line	R/W	00h
3Dh	Interrupt Pin	R	01h
3Eh	Min_Gnt	R	03h
3Fh	Max_Lat	R	56h
4Ch	Special—Subsystem Write Capability	R/W	00000000h

* The revision of the USS-312 can be identified either electronically or by physical markings. The revision can be identified electronically using the standard PCI revision ID register described in this table. The revision can also be identified by physical markings using the last letter of the USS-312 identifier code printed on the device. The USS-312 identifier code will be printed using the format USS312XY, where X will identify the package type (M or T) and Y will identify the revision.

† This register is normally read only. Write capability of this register is available to system BIOS only.

PCI Registers

Table 4. Vendor ID Register (00h—01h)

This register is fixed as the Lucent Technologies Microelectronics Group vendor ID assigned by the PCI SIG.

Bits	Field	Read/Write	Reset/Description
15:0	Vendor ID	R	Assigned 11C1h

Table 5. Device ID Register (02h—03h)

This register is fixed as the Lucent Technologies Microelectronics Group product USS-312.

Bits	Field	Read/Write	Reset/Description
15:0	Device ID	R	Assigned 5802h

Table 6. Command Register (04h—05h)

All read-only bits represent nonconfigurable features of the USS-312.

Bits	Field	Read/Write	Reset/Description
0	IO Space	R/W	0
1	Memory Space	R/W	0
2	Bus Master	R/W	0
3	Special Cycles	R	0
4	Memory Write and Invalidate Enable	R/W	0
5	VGA Palette Snoop	R	0
6	Parity Error Response	R/W	0
7	Wait Cycle Control	R	0
8	SERRN Enable	R/W	0
9	Fast Back-to-back Enable	R/W	0
15:10	Reserved	R	000000b

PCI Registers (continued)

Table 7. Status Register (06h—07h)

All read-only bits represent nonconfigurable features of the USS-312.

Bits	Field	Read/Write	Reset/Description
3:0	Reserved	R	0000b
4	Capabilities	R	0 if PMIENABLE = 0b 1 if PMIENABLE = 1b
5	66 MHz Capable	R	0
6	UDF Support	R	0
7	Fast Back-to-back Capable	R	0
8	Data Parity Error Detected	R/W	0
10:9	DEVSEL Timing	R	01
11	Signaled Target Abort	R/W	0
12	Received Target Abort	R/W	0
13	Received Master Abort	R/W	0
14	Signaled System Error	R/W	0
15	Detected Parity Error	R/W	0

PCI Registers (continued)

Table 8. Revision ID Register (08h)

Represents the current revision of the USS-312.

Bits	Field	Read/Write	Reset/Description
7:0	Revision ID*	R	11h = Revision B 10h = Revision C

* The revision of the USS-312 can be identified either electronically or by physical markings. The revision can be identified electronically using the standard PCI revision ID register described in this table. The revision can also be identified by physical markings using the last letter of the USS-312 identifier code printed on the device. The USS-312 identifier code will be printed using the format USS312XY, where X will identify the package type (M or T) and Y will identify the revision.

Table 9. Class Code Register (09h—0Bh)

The PCI class code for all OpenHCI host controllers is defined in the OpenHCI specification.

Bits	Field	Read/Write	Reset/Description
7:0	Programming Interface	R	10h = OpenHCI Host Controller
15:8	Sub Class	R	03h = Universal Serial Bus
23:16	Base Class	R	0Ch = Serial Bus Controller

Table 10. Cache Line Size Register (0Ch)

No cache line is supported by the USS-312.

Bits	Field	Read/Write	Reset/Description
7:0	Cache Line Size	R	00h

Table 11. Latency Timer Register (0Dh)

Controls the number of clock cycles the USS-312 may remain on the PCI bus after becoming bus master.

Bits	Field	Read/Write	Reset/Description
7:0	Latency Timer	R/W	Upper 5 bits are read/write. Lower 3 bits are read only.

Table 12. Header Type Register (0Eh)

The USS-312 supports PCI header type 0 only.

Bits	Field	Read/Write	Reset/Description
7:0	Header Type	R	00h

PCI Registers (continued)

Table 13. BIST Register (0Fh)

BIST is not supported by the USS-312.

Bits	Field	Read/Write	Reset/Description
7:0	BIST	R	00h

Table 14. Base Address Register 0 (10h—13h)

The base address register is used to specify to the PCI operating system the memory size of the USS-312 device. As recommended by the OpenHCI specification, the lower 12 bits are read only (fixed to logic 0) to indicate 4K (2^{12}) memory size.

Bits	Field	Read/Write	Reset/Description
31:0	BAR 0	R/W	Lower 12 bits are read only. Upper 20 bits are read/write.

Table 15. Base Address Register 1, 2, 3, 4, 5 (14h—17h), (18h—1Bh), (1Ch—1Fh), (20h—23h), (24h—27h)

These base address registers are unused by the USS-312 device.

Bits	Field	Read/Write	Reset/Description
31:0	BAR 1—5	R	00000000h

Table 16. Cardbus CIS Pointer Register (28h—2Bh)

Cardbus CIS pointer not required for the USS-312.

Bits	Field	Read/Write	Reset/Description
31:0	CardBus CIS Pointer	R	00000000h

Table 17. Subsystem Vendor ID Register (2Ch—2Dh)

The subsystem vendor ID is R/W for compliance with *Microsoft* PC98 specifications. On reset, this register is read only. System BIOS may write a 1 to Special—Subsystem Write Capability register (4Ch) bit 0 to enable write capability of this register. After configuring this register, the system BIOS must write a 0 to Special—Subsystem Write Capability register (4Ch) bit 0 to disable write capability of this register.

Bits	Field	Read/Write	Reset/Description
15:0	Subsystem Vendor ID	R/W	11C1h

Table 18. Subsystem ID Register (2Eh—2Fh)

The subsystem vendor ID is R/W for compliance with *Microsoft* PC98 specifications. On reset, this register is read only. System BIOS may write a 1 to Special—Subsystem Write Capability register (4Ch) bit 0 to enable write capability of this register. After configuring this register, the system BIOS must write a 0 to Special—Subsystem Write Capability register (4Ch) bit 0 to disable write capability of this register.

Bits	Field	Read/Write	Reset/Description
15:0	Subsystem ID	R/W	5802h

PCI Registers (continued)

Table 19. Expansion ROM Base Address Register (30h—33h)

Expansion ROM not supported by the USS-312.

Bits	Field	Read/Write	Reset/Description
31:0	Expansion ROM Base Address	R	00000000h

Table 20. Capabilities Pointer Register (34h)

Bits	Field	Read/Write	Reset/Description
7:0	Cap_Ptr	R	00h if PMIENABLE = 0b 50h if PMIENABLE = 1b

Table 21. Interrupt Line Register (3Ch)

Bits	Field	Read/Write	Reset/Description
7:0	Interrupt Line	R/W	00h

Table 22. Interrupt Pin Register (3Dh)

Interrupt A used as the USS-312 interrupt.

Bits	Field	Read/Write	Reset/Description
7:0	Interrupt Pin	R	01h

Table 23. Min_Gnt Register (3Eh)

The USS-312 can support a four DWORD master burst read or write which requires less than 500 ns.

Bits	Field	Read/Write	Reset/Description
7:0	Min_Gnt	R	03h

Table 24. Max_Lat Register (3Fh)

The USS-312 requires service at a minimum interval of 21.3 µs.

Bits	Field	Read/Write	Reset/Description
7:0	Max_Lat	R	56h

Table 25. Special—Subsystem Write Capability (4Ch)

This is a special register implemented for compliance with *Microsoft* PC98 Specification, Chapter 9, Item 11. Bit 0 is read/write to allow the system BIOS to enable write capability of the Subsystem Vendor ID and Subsystem ID registers (refer to Tables 17 and 18).

Bits	Field	Read/Write	Reset/Description
31:1	Reserved	R	00000000h
0	Subsystem Write	R/W	0b 0 = Subsystem write disabled 1 = Subsystem write enabled

USB Registers

Table 26. USB Operational Registers Summary

Refer to Tables 27—48 for more details on each of these registers.

Offset	Register Name
00h	HcRevision
04h	HcControl
08h	HcCommandStatus
0Ch	HcInterruptStatus
10h	HcInterruptEnable
14h	HcInterruptDisable
18h	HcHCCA
1Ch	HcPeriodCurrentED
20h	HcControlHeadED
24h	HcControlCurrentED
28h	HcBulkHeadED
2Ch	HcBulkCurrentED
30h	HcDoneHead
34h	HcFmInterval
38h	HcFmRemaining
3Ch	HcFmNumber
40h	HcPeriodicStart
44h	HcLSThreshold
48h	HcRhDescriptorA
4Ch	HcRhDescriptorB
50h	HcRhStatus
54h	HcRhPortStatus[1]
58h	HcRhPortStatus[2]
100h	HceControl
104h	HceInput
108h	HceOutput
10Ch	HceStatus

Table 27. HcRevision Register (00h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
7:0	Revision (REV)	10h	R	R
8	Legacy (L)	1b	R	R

USB Registers (continued)

Table 28. HcControl Register (04h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
1:0	Control Bulk Service Ratio (CBSR)	00b	R/W	R
2	Periodic List Enable (PLE)	0b	R/W	R
3	Isochronous Enable (IE)	0b	R/W	R
4	Control List Enable (CLE)	0b	R/W	R
5	Bulk List Enable (BLE)	0b	R/W	R
7:6	Host Controller Functional State (HCFS) 00b: UsbReset 01b: UsbResume 10b: UsbOperational 11b: UsbSuspend	00b	R/W	R/W
8	Interrupt Routing (IR)	0b	R/W	R
9	Remote Wakeup Connected (WC)	0b	R/W	R/W
10	Remote Wakeup Enable (RWE)	0b	R/W	R

Table 29. HcCommandStatus Register (08h)

Bits	Field	Reset	HCD	HC
0	Host Controller Reset (HCR)	0b	R/W	R/W
1	Control List Filled (CLF)	0b	R/W	R/W
2	Bulk List Filled (BLF)	0b	R/W	R/W
3	Ownership Change Request (OCR)	0b	R/W	R/W
17:16	Scheduling Overrun Count (SOC)	0b	R	R/W

Table 30. HcInterruptStatus Register (0Ch)

Bits	Field	Reset	HCD	HC
0	Scheduling Overrun (SO)	0b	R/W	R/W
1	Writeback Done Head (WDH)	0b	R/W	R/W
2	Start of Frame (SF)	0b	R/W	R/W
3	Resume Detected (RD)	0b	R/W	R/W
4	Unrecoverable Error (UE)	0b	R/W	R/W
5	Frame Number Overflow (FNO)	0b	R/W	R/W
6	Root Hub Status Change (RHSC)	0b	R/W	R/W
31	Ownership Change (OC)	0b	R/W	R/W

USB Registers (continued)

Table 31. HcInterruptEnable Register (10h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
0	Scheduling Overrun (SO) 0—Ignore 1—Enable interrupt	0b	R/W	R
1	Writeback Done Head (WDH) 0—Ignore 1—Enable interrupt	0b	R/W	R
2	Start of Frame (SF) 0—Ignore 1—Enable interrupt	0b	R/W	R
3	Resume Detected (RD) 0—Ignore 1—Enable interrupt	0b	R/W	R
4	Unrecoverable Error (UE) 0—Ignore 1—Enable interrupt	0b	R/W	R
5	Frame Number Overflow (FNO) 0—Ignore 1—Enable interrupt	0b	R/W	R
6	Root Hub Status Change (RHSC) 0—Ignore 1—Enable interrupt	0b	R/W	R
30	Ownership Change (OC) 0—Ignore 1—Enable interrupt	0b	R/W	R
31	Master Interrupt Enable (MIE) 0—Ignored by HC 1—Enables interrupt generation due to events specified in the other bits of this register.	0b	R/W	R

USB Registers (continued)

Table 32. HcInterruptDisable Register (14h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
0	Scheduling Overrun (SO) 0—Ignore 1—Disable interrupt generation	0b	R/W	R
1	Writeback Done Head (WDH) 0—Ignore 1—Disable interrupt	0b	R/W	R
2	Start of Frame (SF) 0—Ignore 1—Disable interrupt	0b	R/W	R
3	Resume Detected (RD) 0—Ignore 1—Disable interrupt	0b	R/W	R
4	Unrecoverable Error (UE) 0—Ignore 1—Disable interrupt	0b	R/W	R
5	Frame Number Overflow (FNO) 0—Ignore 1—Disable interrupt	0b	R/W	R
6	Root Hub Status Change (RHSC) 0—Ignore 1—Disable interrupt	0b	R/W	R
30	Ownership Change (OC) 0—Ignore 1—Disable interrupt	0b	R/W	R
31	Master Interrupt Enable (MIE) 0—Ignored by HC 1—Disables interrupt generation due to events specified in the other bits of this register.	0b	R/W	R

USB Registers (continued)

Table 33. HcHCCA Register (18h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:8	Host Controller Communications Area (HCCA) Base Address Bits 7:0 will always return a 0.	0h	R/W	R

Table 34. HcPeriodCurrentED Register (1Ch)

Bits	Field	Reset	HCD	HC
31:4	Period Current ED (PCED) Base Address Bits 3:0 will always return a 0.	0h	R/W	R

Table 35. HcControlHeadED Register (20h)

Bits	Field	Reset	HCD	HC
31:4	Control Head ED (CHED) Base Address Bits 3:0 will always return a 0.	0h	R/W	R

Table 36. HcControlCurrentED Register (24h)

Bits	Field	Reset	HCD	HC
31:4	Control Current ED (CCED) Base Address Bits 3:0 will always return a 0.	0h	R/W	R/W

Table 37. HcBulkHeadED Register (28h)

Bits	Field	Reset	HCD	HC
31:4	Bulk Head ED (BHED) Base Address Bits 3:0 will always return a 0.	0h	R/W	R

Table 38. HcBulkCurrentED Register (2Ch)

Bits	Field	Reset	HCD	HC
31:4	Bulk Current ED (BCED) Base Address Bits 3:0 will always return a 0.	0h	R/W	R/W

Table 39. HcDoneHead Register (30h)

Bits	Field	Reset	HCD	HC
31:4	Done Head ED (DH) Base Address Bits 3:0 will always return a 0.	0h	R	R/W

USB Registers (continued)

Table 40. HcFmInterval Register (34h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
13:0	Frame Interval (FI)	2EDFh	R/W	R
30:16	FS Largest Data Packet (FSMPS)	0h	R/W	R
31	Frame Interval Toggle (FIT)	0b	R/W	R

Table 41. HcFmRemaining Register (38h)

Bits	Field	Reset	HCD	HC
13:0	Frame Remaining (FR)	0h	R	R/W
31	Frame Remaining Toggle (FRT)	0b	R	R/W

Table 42. HcFmNumber Register (3Ch)

Bits	Field	Reset	HCD	HC
15:0	Frame Number (FN)	0h	R	R/W

Table 43. HcPeriodicStart Register (40h)

Bits	Field	Reset	HCD	HC
13:0	Periodic Start (PS)	0h	R/W	R

Table 44. HcLSThreshold (44h)

Bits	Field	Reset	HCD	HC
11:0	LS Threshold	628h	R/W	R

Table 45. HcRhDescriptorA Register (48h)

Bits	Field	Reset	HCD	HC
7:0	Number Downstream Ports (NDP)	02h	R	R
8	Power Switching Mode (PSM)	1b	R/W	R
9	No Power Switching (NPS)	0b	R/W	R
10	Device Type (DT)	0b	R	R
11	Overcurrent Protection Mode (OCPM)	1b	R/W	R
12	No Overcurrent Protection (NOCP)	0b	R/W	R
24:31	Power On to Power Good Time (POTPGT)	10h	R/W	R

USB Registers (continued)

Table 46. HcRhDescriptorB Register (4Ch)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
15:0	Device Removable (DR)	0000h	R/W	R
17:16	Port Power Control Mask (PPCM)	0006h	R/W	R

Table 47. HcRhStatus Register (50h)

Bits	Field	Reset	HCD	HC
0	Local Power Status (LPS)	0b	R/W	R
1	Overcurrent Indicator (OCI)	0b	R	R/W
15	Device Remote Wakeup Enable (DRWE)	0b	R/W	R
16	Local Power Status Change (LPSC)	0b	R/W	R
17	Overcurrent Indicator Change (OCIC)	0b	R/W	R/W
31	Clear Remote Wakeup Enable (CRWE)	0b	W	R

Table 48. HcRhPortStatus 1, 2 Register (54h), (58h)

Bits	Field	Reset	HCD	HC
0	Current Connect Status (CCS)	0b	R/W	R/W
1	Port Enable Status (PES)	0b	R/W	R/W
2	Port Suspend Status (PSS)	0b	R/W	R/W
3	Port Overcurrent Indicator (POCI)	0b	R/W	R/W
4	Port Reset Status (PRS)	0b	R/W	R/W
8	Port Power Status (PPS)	0b	R/W	R/W
9	Low-speed Device Attached (LSDA)	0b	R/W	R/W
16	Connect Status Change (CSC)	0b	R/W	R/W
17	Port Enable Status Change (PESC)	0b	R/W	R/W
18	Port Suspend Status Change (PSSC)	0b	R/W	R/W
19	Port Overcurrent Indicator Change (OCIC)	0b	R/W	R/W
20	Port Reset Status Change (PRSC)	0b	R/W	R/W

Legacy Support Registers

Four operational registers are used to provide the legacy support. Each of these registers is located on a 32-bit boundary. The offset of these registers is relative to the base address of the host controller operational registers with HceControl located at offset 100h.

Table 49. Legacy Support Registers

Offset	Register	Description
100h	HceControl	Used to enable and control the emulation hardware and report various status information.
104h	HceInput	Emulation side of the Legacy Input Buffer register.
108h	HceOutput	Emulation side of the Legacy Output Buffer register where keyboard and mouse data is to be written by software.
10Ch	HceStatus	Emulation side of the Legacy Status register.

Three of the operational registers (HceStatus, HceInput, HceOutput) are accessible at I/O address 60h and 64h when emulation is enabled. Reads and writes to the registers using I/O addresses have side effects as outlined in the Table 50.

Table 50. Emulated Registers

I/O Address	Cycle Type	Register Contents Accessed/Modified	Side Effects
60h	IN	HceOutput	IN from port 60h will set OutputFull in HceStatus to 0.
60h	OUT	HceInput	OUT to port 60h will set InputFull to 1 and CmdData to 0 in HceStatus.
64h	IN	HceStatus	IN from port 64h returns current value of HceStatus with no other side effect.
64h	OUT	HceInput	OUT to port 64h will set InputFull to 0 and CmdData in HceStatus to 1.

HceInput Register

Table 51. HceInput Register (104h)

Bit	Field	R/W	Description
7:0	InputData	R/W	This register holds data that is written to I/O ports 60h and 64h.
31:8	Reserved	—	—

I/O data that is written to ports 60h and 64h is captured in this register when emulation is enabled. This register may be read or written directly by accessing it with its memory address in the host controller's operational register space. When accessed directly with a memory cycle, reads and writes of this register have no side effects.

Legacy Support Registers (continued)

HceOutput Register

Table 52. HceOutput Register (108h)

Bit	Field	R/W	Description
7:0	OutputData	R/W	This register hosts data that is returned when an I/O read of port 60h is performed by application software.
31:8	Reserved	—	—

The data placed in this register by the emulation software is returned when I/O port 60h is read and emulation is enabled. On a read of this location, the OutputFull bit in HceStatus is set to 0.

HceStatus Register

Table 53. HceStatus Register (10Ch)

Bit	Field	R/W	Description
0	OutputFull	R/W	The HC sets this bit to 0 on a read of I/O port 60h. If IRQEn is set and AuxOutputFull is set to 0, then an IRQ1 is generated as long as this bit is set to 1. If IRQEn is set and AuxOutputFull is set to 1, then an IRQ12 is generated as long as this bit is set to 1. While this bit is 0 and CharacterPending in HceControl is set to 1, an emulation interrupt condition exists.
1	InputFull	R/W	Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
2	Flag	R/W	Nominally used as a system flag by software to indicate a warm or cold boot.
3	CmdData	R/W	The HC sets this bit to 0 on an I/O write to port 60h and to 1 on an I/O write to port 64h.
4	Inhibit Switch	R/W	This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is **not** inhibited.
5	AuxOutputFull	R/W	IRQ12 is asserted whenever this bit is set to 1 and OutputFull is set to 1 and the IRQEn bit is set.
6	Time-out	R/W	Used to indicate a time-out.
7	Parity	R/W	Indicates parity error on keyboard/mouse data.
31:8	Reserved	—	—

The contents of the HceStatus register are returned on an I/O read of port 64h when emulation is enabled. Reads and writes of port 60h and writes to port 64h can cause changes in this register. Emulation software can directly access this register through its memory address in the host controller's operational register space. Accessing this register through its memory address produces no side effects.

Legacy Support Registers (continued)

HceControl Register

Table 54. HceControl Register (100h)

Bit	Field	Reset	R/W	Description
0	EmulationEnable	0b	R/W	When set to 1, the HC is enabled for legacy emulation. The HC decodes accesses to I/O registers 60h and 64h and generates IRQ1 and/or IRQ12 when appropriate. Additionally, the HC generates an emulation interrupt at appropriate times to invoke the emulation software.
1	EmulationInterrupt	—	R	This bit is a static decode of the emulation interrupt condition.
2	CharacterPending	0b	R/W	When set, an emulation interrupt is generated when the OutputFull bit of the HceStatus register is set to 0.
3	IRQEn	0b	R/W	When set, the HC generates IRQ1 or IRQ12 as long as the OutputFull bit in HceStatus is set to 1. If the AuxOutputFull bit of HceStatus is 0, then IRQ1 is generated; if it is 1, then an IRQ12 is generated.
4	ExternalIRQEn	0b	R/W	When set to 1, IRQ1 and IRQ12 from the keyboard controller causes an emulation interrupt. The function controlled by this bit is independent of the setting of the EmulationEnable bit in this register.
5	GateA20Sequence	0b	R/W	Set by HC when a data value of D1h is written to I/O port 64h. Cleared by HC on write to I/O port 64h of any value other than D1h.
6	IRQ1Active	0b	R/W	Indicates that a positive transition on IRQ1 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0). SW write of a 0 to this bit has no effect.
7	IRQ12Active	0b	R/W	Indicates that a positive transition on IRQ12 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0). SW write of a 0 to this bit has no effect.
8	A20State	0b	R/W	Indicates current state of gate A20 on keyboard controller. Used to compare against value written to 60h when GateA20Sequence is active.
31:9	Reserved	—	—	Must read as 0s.

PCI Connection Instructions

The USS-312 interfaces directly with any 32-bit, 33 MHz PCI bus simply by connecting all PCI related signals directly to the signals on the host motherboard or card edge of an expansion card. The PCI signaling level for all PCI signals of the USS-312 is selected by connecting the VIO signal to the signaling voltage on the motherboard or VIO pin on the card edge of the expansion card. The VIO pin will select the PCI signaling level as indicated in Table 55. Regardless of signaling level chosen on VIO, the VDD5 input pin must remain 5 V.

Table 55. PCI Signaling Levels

VIO Pin Input Voltage	USS-312 PCI Signaling Level (All PCI Signals)
4.75 V—5.25 V	5 V signaling
3.0 V—3.6 V	3.3 V signaling

USB Connection Instructions

The USS-312 is a port-powered OHCI host controller (refer to OHCI specification) requiring an external switchable power regulator to supply downstream USB port power controlled by the USS-312. The power regulator interface has been designed to interface directly with commonly used USB power regulators with very little additional circuitry. The PRTPWR[1, 2] output signal is used as the switch for the power regulator. The PRTPWR[1, 2] signal must be bootstrapped with a pull-up or pull-down resistor to select the appropriate power switch polarity. Bootstrapping with a pull-up resistor will select an active-low power switch while bootstrapping with a pull-down will select an active-high power switch.

The PWROK[1, 2] is connected directly to the USB power from the regulator output to indicate the presence of USB port power.

The PWRFLT[1, 2]N can be connected directly to an active-low power fault regulator output to inform the USS-312 of a USB port overcurrent condition.

DPLS[1, 2] and DMNS[1, 2] are related to the integrated USB transceiver and are connected directly to the USB port connector through a 33 Ω—36 Ω series resistor for each signal. Figure 4 shows the USS-312 connection to the USB.

CLK48 must be connected to a 48 MHz oscillator to provide a suitable USB clock to the USS-312.

Power Connection Recommendations

The USS-312 is a 3.3 V device. Therefore, all VDD inputs must be connected to an appropriate 3.3 V source. VDD5 must always be connected to a 5 V source. VDDT provides all transceiver power and must be connected to a 3.3 V source. It is recommended that the system designer undertake special board routing and filtering of VDDT and VSST to isolate these power inputs from noise induced by other components.

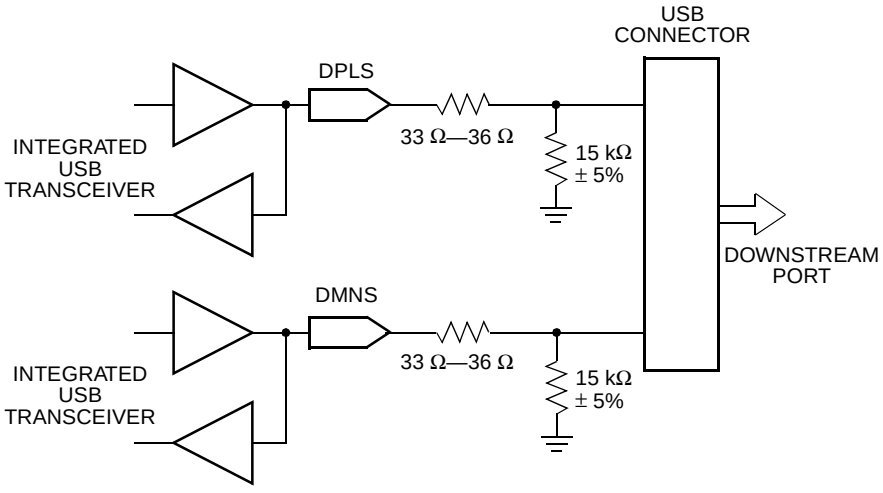

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Figure 4. USB Transceiver Connection

Power Management Interface

An advanced power management capabilities interface compliant with *PCI Bus Power Management Interface Specification Revision 1.1* has been incorporated into the USS-312. This interface allows the USS-312 to be placed in various power management states offering a variety of power savings for a host system. All required and optional power management states have been incorporated into the USS-312.

Table 56 highlights the USS-312 support for power management states and features supported for each of the power management states. The USS-312 has the ability to internally gate-off the CLK48 input, disable the USB transceivers, and assert USB resume signaling asynchronously (without active CLK48) in response to upstream USB resume being detected. The USS-312 will assert PMEN and retain chip context in accordance with the rules defined in the *PCI Bus Power Management Interface Specification Revision 1.1.*

Table 56. USS-312 Support for Power Management States

Power Management State	State Required/ Optional	Clk48 Active Internally	USB Trans-ciever Active	Async Resume Logic Active	PMEN Assert Enabled	Chip Context Main-tained	Comments
D0	Required	X	X	—	—	X	Fully awake backwards compat-ible state. All logic in full power mode.
D1	Optional	X	X	—	X	X	Fully awake state with PCI bus master capabilities turned off by host. All logic in full power mode because of low latency returning to D0 state.
D2	Optional	—	—	X*	X	X	USB sleep state with PCI bus master capabilities turned off by host. PCI clocks may be turned off by the system.
D3hot	Optional	—	—	X*	X	—	Deep USB sleep state with PCI bus master capabilities turned off by host. PCI clocks may be turned off by the system.
D3cold	Required	—	—	—	—	—	Fully asleep backwards com-patible state. All power turned off. Reset required to recover to D0 state. All downstream devices disconnected because of power loss.

* Asynchronous resume logic active only when PME_Enable register bit is active.

A wakeup event (power management event) detected by a USB host controller is considered either an upstream resume detected or a connect status change (device disconnecting/connecting) detected. Any of these events detected by the USS-312 while the power management event is enabled will cause PMEN to be issued.

This power management feature is considered an extension of the PCI Specification and is only present when enabled by the PmiEnable input pin. While the PmiEnable input pin is logic 1, the power management function is enabled, the Power Management registers and Capabilities Pointer register are accessible, and the PCI Configura-tion Space Status register, bit 4, will read as logic 1 (capabilities list present). While the PmiEnable input pin is logic 0 (or ground), the power management function is disabled, the Power Management registers and Capabilities Pointer register are inaccessible and read as 0h, and the PCI Configuration Space Status register, bit 4, will read as logic 0 (no capabilities list).

Power Management Interface (continued)

PMEN is an open collector output allowing wire-OR of several PMEN signals.

The following power management register definitions present the specific implementation of the *PCI Bus Power Management Interface Specification* for the USS-312. All the following registers are located in the USS-312 PCI Configuration Memory Space. All further information concerning the register functions and the system implementation of this interface should be referenced from the *PCI Bus Power Management Interface Specification Revision 1.1* available from the PCI Special Interest Group.

Configuration Space Offset 50h

Table 57. Capabilities Identifier (Cap_ID) Register

Bits	Default Value	Read/Write	Description
7:0	01h	R	This capability is for the PCI power management data structure.

Configuration Space Offset 51h

Table 58. Next Item Pointer Register

Bits	Default Value	Read/Write	Description1
7:0	00h	R	No other PCI capabilities are implemented.

Power Management Interface (continued)

Configuration Space Offset 52h

Table 59. Power Management Capabilities Register

Bits	Default Value	Read/ Write	Name/Description
15:11	01110b	R	**PME_Support.** Specifies the states in which the PME signal can be asserted. XXXX0b—PME cannot be asserted in D0 state. XXX1Xb—PME can be asserted in D1 state. XX1XXb—PME can be asserted in D2 state. X1XXXb—PME can be asserted in D3hot state. 0XXXXb—PME cannot be asserted in D3cold state.
10	1b	R	**D2_Support.** This device supports the D2 power management state.
9	1b	R	**D1_Support.** This device supports the D1 power management state.
8:6	000b	R	**Aux_Current.** PMEN generation is not supported by this function. Therefore, this register is not applicable and returns 000b.
5	0b	R	**DSI.** No device-specific initialization sequence is required before using this device.
4	0b	R	**Reserved.**
3	0b	R	**PME Clock.** No clocks are required for this device to issue PMEN.
2:0	010b	R	**Version.** PCI Power Management Interface Specification Revision 1.1 compliant.

Power Management Interface (continued)

Configuration Space Offset 54h

Table 60. Power Management Control/Status Register

Bits	Default Value	Read/ Write	Name/Description
15	0b	Read/ Write-Clear	**PME_Status.** This bit is set when the function would normally assert the PMEN signal independent of the state of the PME_En bit. Writing a 1b to this bit will clear the PME_Status bit and force the function to stop asserting PMEN.
14:13	See Table 63	R	**Data Scale.** Variable based upon data select. See Table 63.
12:9	0000b	R/W	**Data_Select.** The system uses this register to select the appropriate data for reporting in the Data Scale register and Data register.
8	0b	R/W	**PME_En**. When active (1b), the function is enabled to assert PMEN.
7:2	000000b	R	**Reserved.**
1:0	00b	R/W	**Power_State.** Represents the current power state of the function.

Configuration Space Offset 56h

Table 61. Power Management Control/Status Bridge Support Extension Register

Bits	Default Value	Read/ Write	Name/Description
7	0b	R	**BPCC_En (Bus Power/Clock Control Enable).** This is not a PCI bridge function.
6	0b	R	**B2_B3# (B2/B3 Support for D3hot).** This is not a PCI bridge function.
5:0	000000b	R	**Reserved.**

Power Management Interface (continued)

Configuration Space Offset 57h

Table 62. Data Register

Bits	Default Value	Read/ Write	Description
7:0	See Table 63	R	Represents the amount of power dissipated or consumed in various power management states. Variable based upon data select. See Table 63.

Power Consumption/Dissipation Reporting

The value that the software writes in the Data_Select register (see Table 60) selects the values that are returned in both the data (see Table 62) and data scale (see Table 60) registers.

Table 63. Power Consumption/Dissipation Reporting

Value In Data Select	Data Reported	Data	Data Scale	Units (Interpreting Data Scale)
0000b	D0 Power Consumed	26h	01b	mW * 100
0001b	D1 Power Consumed	26h	01b	mW * 100
0010b	D2 Power Consumed	66h	11b	mW
0011b	D3 Power Consumed	07h	11b	mW
0100b	D0 Power Dissipated	37h	10b	mW * 10
0101b	D1 Power Dissipated	37h	10b	mW * 10
0110b	D2 Power Dissipated	64h	11b	mW
0111b	D3 Power Dissipated	03h	11b	mW
1111b—1000b	Reserved (single-function PCI device configuration)	00000000b	00b	NA

NAND Tree Mode

The USS-312 can be placed in a NAND tree mode of operation for board-level production testing. The NAND tree is designed to allow board level contact testing of inputs and bidirectional pins of the USS-312.

To activate the NAND tree in the USS-312, force pin 21 (TEST0) and pin 25 (TEST1) to a logic high. Prior to testing the NAND tree, the clock input must be pulsed twice while the reset input is active. When pin 21 and pin 25 are logic high, the NAND tree will be active and follow the order of the map presented in Table 64. Figure 5 shows the NAND tree logic structure.

Table 64. NAND Tree

Order Assignment	Pin Number	Pin Name	Order Assignment	Pin Number	Pin Name
1 (Start)	31	RSTN	33	78	AD15
2	32	CLK	34	79	AD14
3	35	GNTN	35	82	AD13
4	37	AD31	36	83	AD12
5	38	AD30	37	84	AD11
6	39	AD29	38	86	AD10
7	42	AD28	39	87	AD9
8	43	AD27	40	88	AD8
9	44	AD26	41	89	C/BEN0
10	45	AD25	42	93	AD7
11	48	AD24	43	94	AD6
12	49	C/BEN3	44	95	AD5
13	50	IDSEL	45	97	KIRQ1I
14	51	AD23	46	99	AD4
15	52	AD22	47	100	AD3
16	53	A20I	48	2	AD2
17	55	AD21	49	3	AD1
18	56	AD20	50	4	AD0
19	57	AD19	51	6	CLK48
20	58	AD18	52	9	PRTPWR1
21	61	AD17	53	10	PWRFLT1N
22	62	AD16	54	11	PWROK1
23	63	C/BEN2	55	22	PWROK2
24	64	FRAMEN	56	23	PWRFLT2N
25	67	IRDYN	57	24	PRTPWR2
26	68	TRDYN	58	13	DPLS1
27	69	DEVSELN	59	14	DMNS1
28	70	STOPN	60	18	DPLS2
29	71	PERRN	61	19	DMNS2
30	73	MIRQ12I	62	30	INTAN
31	76	PAR	63	75	SERRN
32	77	C/BEN1	Output Pin	36	REQN

NAND Tree Mode (continued)

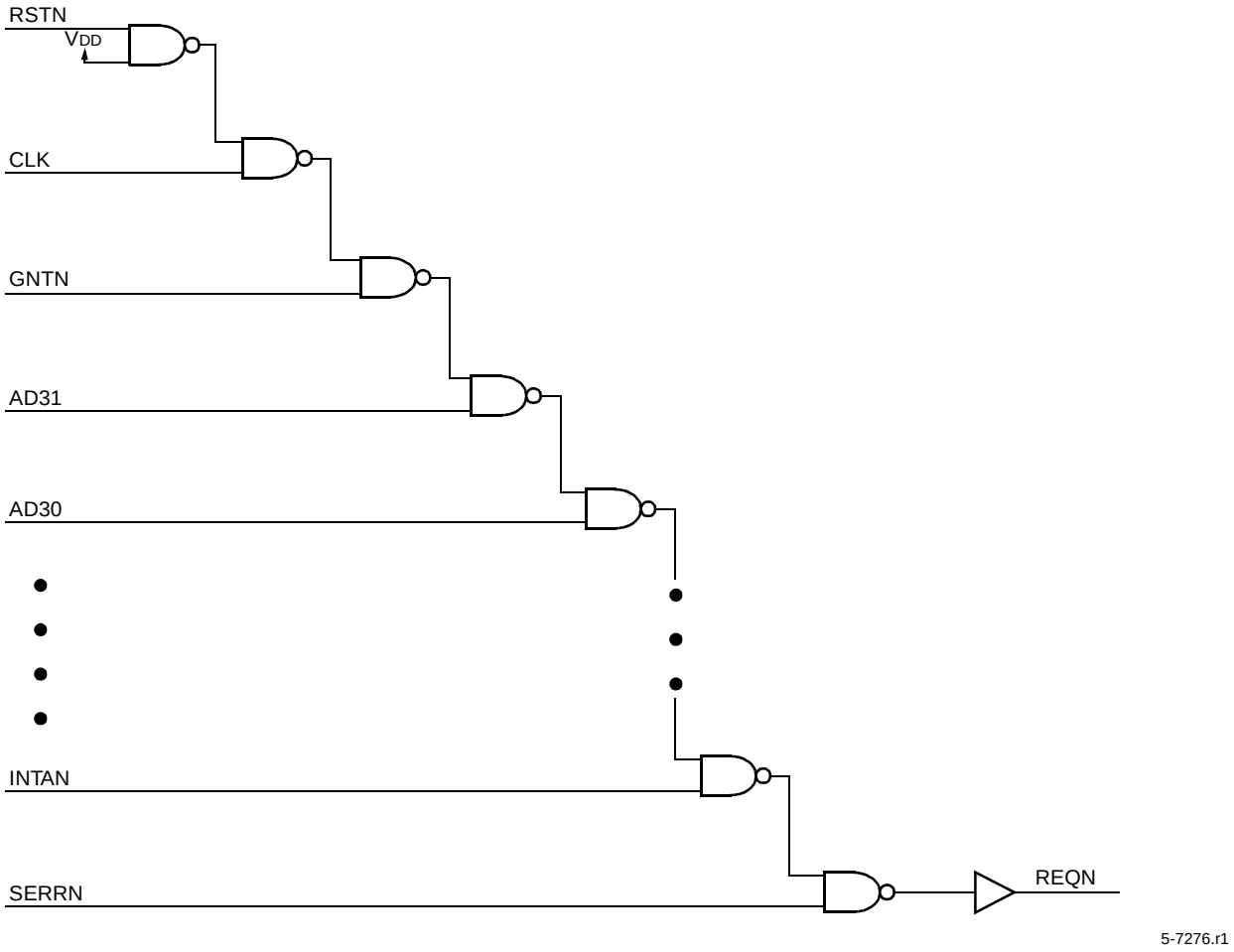


Figure 5. NAND Tree Logic Structure

Absolute Maximum Ratings

Table 65. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature Range	T_A	0	70	°C
Storage Temperature	T_{stg}	–40	125	°C
Voltage on Any Pin with Respect to Ground (Excluding Test0 and Test1)	—	V_{SS} – 0.3	5.5	V
Voltage on Any Pin with Respect to Ground (Test0 and Test1)	—	V_{SS} – 0.3	V_{DD} + 0.3	V
V_{DD}	—	3.0	3.6	V
$V_{DD}T$	—	3.135	3.465	V
$V_{DD}5$	—	4.75	5.25	V
VIO (3.3 V operation)	—	3.0	3.6	V
VIO (5 V operation)	—	4.75	5.25	V

Electrical Characteristics

Table 66. Power Dissipation

Parameter	Symbol	Min	Typ	Max	Unit
Power Dissipation	P_D	140	170	202	mW

PCI Electrical Characteristics

PCI Timing Specifications

The clock waveform must be delivered to each PCI component in the system. In the case of expansion boards, compliance with the clock specification is measured at the expansion board component, not at the connector slot. Figure 6 shows the clock waveform and required measurement points for both 5 V and 3.3 V signaling environments. Table 67 summarizes the clock specifications.

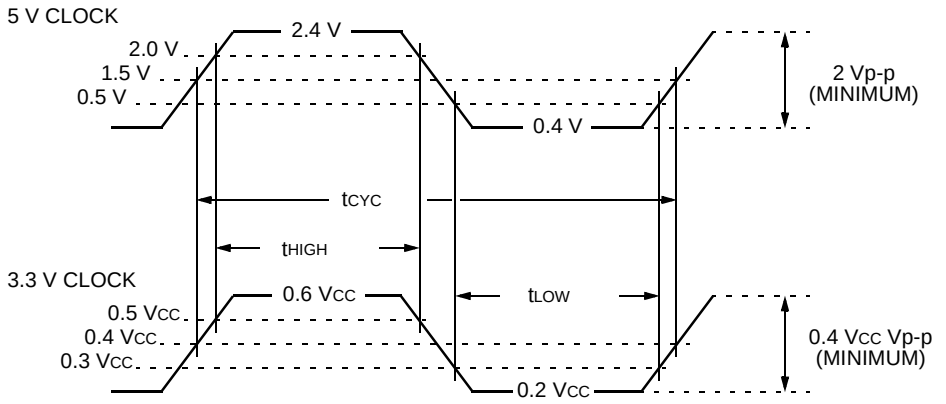


Figure 6. Clock Waveforms

Electrical Characteristics (continued)

PCI Timing Parameters

Table 67. Clock and Reset Specifications

Symbol	Parameter	Min	Max	Unit
t_{CYC}	CLK Cycle Time[1]	30	∞	ns
t_{HIGH}	CLK High Time	11	—	ns
t_{LOW}	CLK Low Time	11	—	ns
—	CLK Slew Rate[2]	1	4	V/ns
—	RSTN Slew Rate[3]	50	—	mV/ns

1. In general, all PCI components must work with any clock frequency between nominal dc and 33 MHz. Device operational parameters at frequencies under 16 MHz may be guaranteed by design rather than by testing. The clock frequency may be changed at any time during the operation of the system, so long as the clock edges remain “clean” (monotonic), and the minimum cycle and high and low times are not violated. The clock may only be stopped in a low state. A variance on this specification is allowed for components designed for use on the system motherboard only. These components may operate at any single fixed frequency up to 33 MHz and may enforce a policy of no frequency changes.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform, as shown in Figure 6.
3. The minimum RSTN slew rate applies only to the rising (deassertion) edge of the reset signal and ensures that system noise cannot render an otherwise monotonic signal to appear to bounce in the switching range.

Electrical Characteristics (continued)

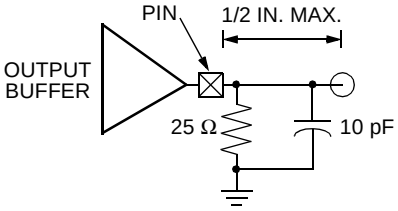
Table 68. 5 V and 3.3 V PCI Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{VAL}	CLK to Signal Valid Delay—Bused Signals[1, 2, 3]	2	11	ns
$t_{VAL(ptp)}$	CLK to Signal Valid Delay—Point to Point[1, 2, 3]	2	12	ns
t_{ON}	Float to Active Delay[1, 7]	2	—	ns
t_{OFF}	Active to Float Delay[1, 7]	—	28	ns
t_{SU}	Input Setup Time to CLK—Bused Signals[3, 4]	7	—	ns
$t_{SU(ptp)}$	Input Setup Time to CLK—Point to Point[3, 4]	10, 12	—	ns
t_{H}	Input Hold Time from CLK[4]	0	—	ns
t_{RST}	Reset Active Time After Power Stable[5]	1	—	ns
$t_{RST-CLK}$	Reset Active Time After CLK Stable[5]	100	—	ns
$t_{RST-OFF}$	Reset Active to Output Float Delay[5, 6, 7]	—	40	ns
t_{RRSU}	REQN to RSTN Setup Time	$10 \times t_{CYC}$	—	ns
t_{RRH}	RSTN to REQN Hold Time	0	50	ns

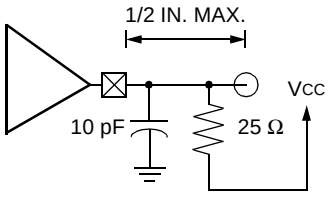
1. See the timing measurement conditions in Figure 4-8 of PCI Specification Revision 2.1.
2. For parts compliant to the 5 V signaling environment:
   Minimum times are evaluated with 0 pF equivalent load; maximum times are evaluated with 50 pF equivalent load. Actual test capacitance may vary, but results should be correlated to these specifications. Note that faster buffers may exhibit some ring back when attached to a 50 pF lump load, which should be of no consequence as long as the output buffers are in full compliance with slew rate and V/I curve specifications.

   For parts compliant to the 3.3 V signaling environment:
   Minimum times are evaluated with same load used for slew rate measurement (see PCI Specification, Rev. 2.1s); maximum times are evaluated with the following load circuits, for high-going and low-going edges, respectively.

t_{VAL}(MAX) RISING EDGE



t_{VAL}(MAX) FALLING EDGE



3. REQN and GNTN are point-to-point signals and have different output valid delay and input setup times than bused signals. GNTN has a setup time of 10 ns; REQN has a setup time of 12 ns. All other signals are bused.
4. See the timing measurement conditions in Figure 4-8 of PCI Specification Revision 2.1.
5. RSTN is asserted and deasserted asynchronously with respect to CLK.
6. All output drivers must be asynchronously floated when RSTN is active.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Electrical Characteristics (continued)

USB Electrical Characteristics

Table 69. Full-Speed Source USB Electrical Characteristics

Parameter	Symbol	Conditions[1, 2, 3]	Min	Max	Unit
Driver Characteristics					
Transition Time[4, 5]:					
Rise Time	t_R	CL = 50 pF	4	20	ns
Fall Time	t_F	CL = 50 pF	4	20	ns
Rise/Fall Time Matching	t_{RFM}	(TR/TF)	90	110	%
Output Signal Crossover Voltage	V_{CRS}	—	1.3	2.0	V
Driver Output Resistance	Z_{DRV}	Steady-State Drive	28	43	Ω
Data Source Timings					
Full-speed Data Rate	t_{DRATE}	Average Bit Rate (12 Mbits/s ± 0.25%)	11.97	12.03	Mbits/s
Frame Interval	t_{FRAME}	1.0 ms ± 0.05%	0.9995	1.0005	ms

1. All voltages measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load (CL) to ground of 50 pF, unless otherwise specified.
3. Full-speed timings have a 1.5 kΩ pull-up to 2.8 V on the D+ data line.
4. Measured from 10% to 90% of the data signal.
5. The rising and falling edges should be smoothly transitioning (monotonic).

Table 70. Low-Speed Source USB Electrical Characteristics

Parameter	Symbol	Conditions	Min	Max	Unit
Driver Characteristics					
Transition Time[1, 2]:					
Rise Time	t_R	CL = 50 pF	75	—	ns
		CL = 350 pF	—	300	ns
Fall Time	t_F	CL = 50 pF	75	—	ns
		CL = 350 pF	—	300	ns
Rise/Fall Time Matching	t_{RFM}	(TR/TF)	80	120	%
Output Signal Crossover Voltage	V_{CRS}	—	1.3	2.0	V
Data Source Timings					
Low-speed Data Rate	t_{DRATE}	Average Bit Rate (1.5 Mbits/s ± 1.5%)	1.4775	1.5225	Mbits/s

1. Measured from 10% to 90% of the data signal.
2. The rising and falling edges should be smoothly transitioning (monotonic).

Table 71. CLK48 Clock Specification

Parameter	Symbol	Min	Max	Unit
CLK Cycle Time	t_{CYC}	20.8 – 0.01%	20.8 + 0.01%	ns
CLK High Time	t_{HIGH}	8.32	12.48	ns
CLK Low Time	t_{LOW}	8.32	12.48	ns

Physical Markings

Each USS-312 will be physically marked as follows:

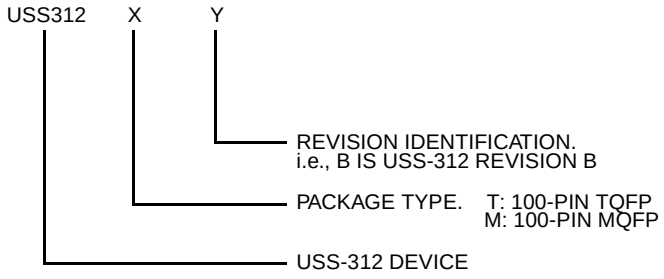


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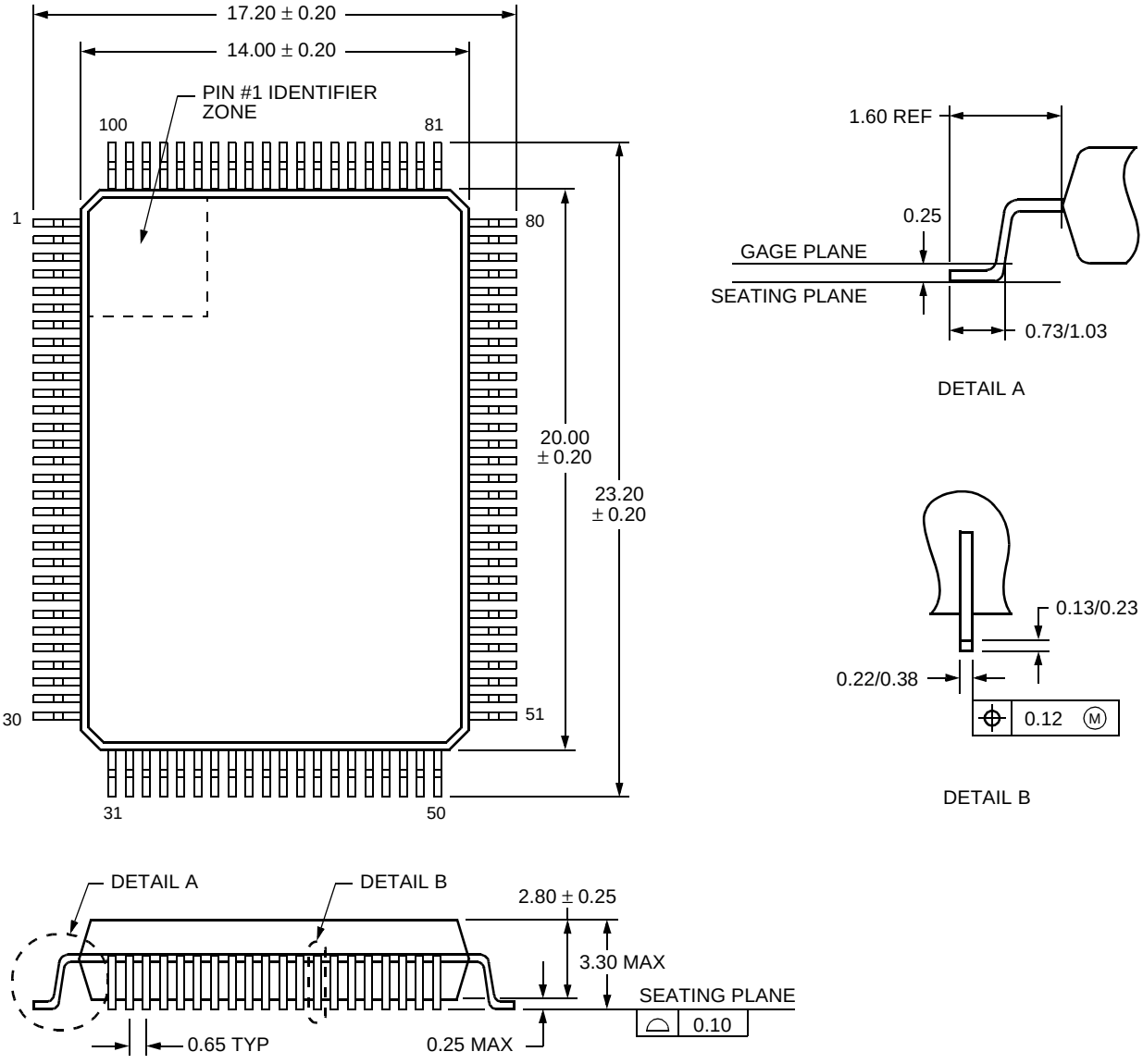
Figure 7. USS-312 Physical Markings

Outline Diagrams

100-Pin MQFP

Dimensions are in millimeters.



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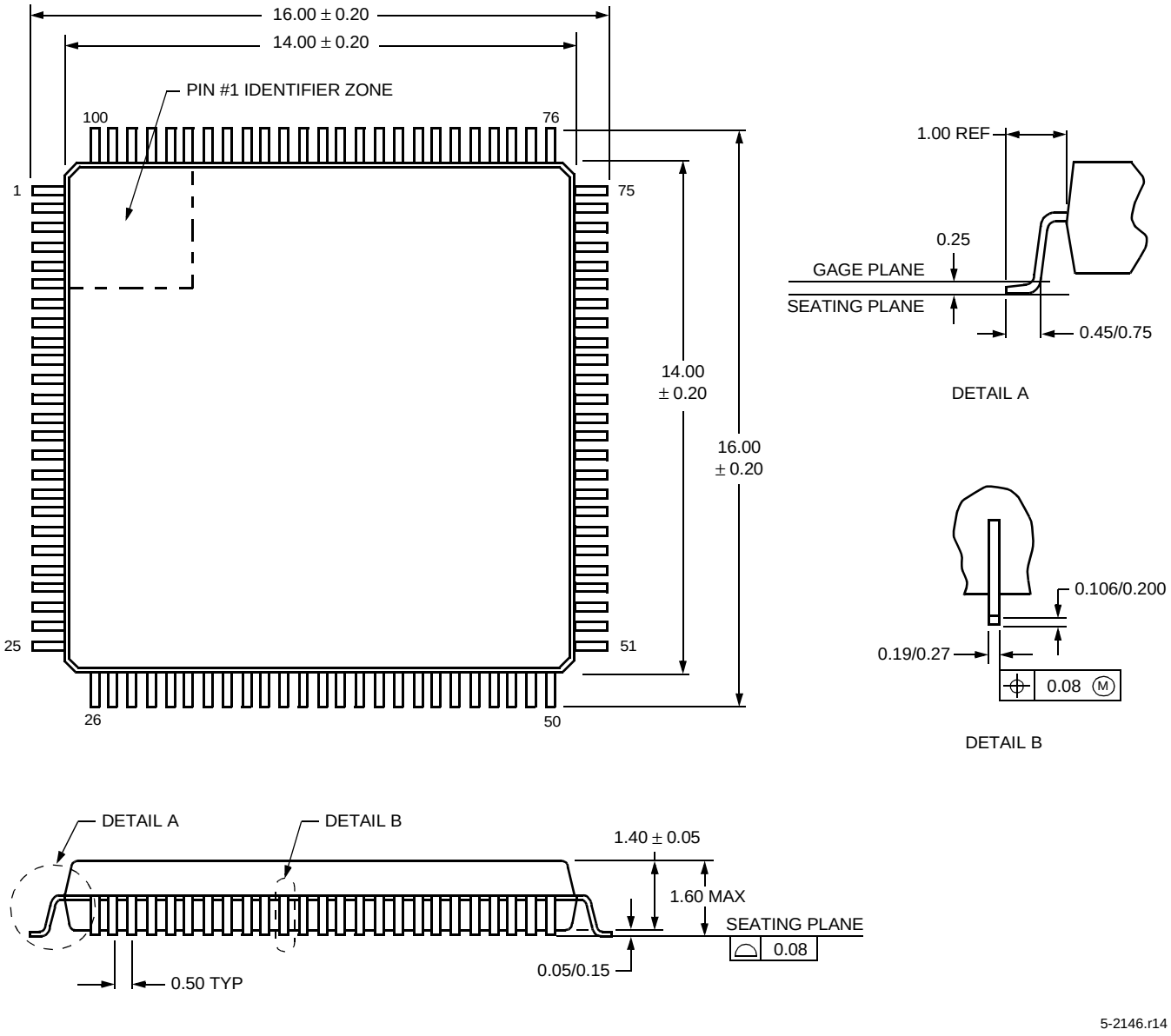
Outline Diagrams (continued)

100-Pin TQFP

Dimensions are in millimeters.



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Ordering Information

Device Code	Package	Comcode
USS312MC	100-Pin MQFP	108555194
USS312TC	100-Pin TQFP	108555186

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