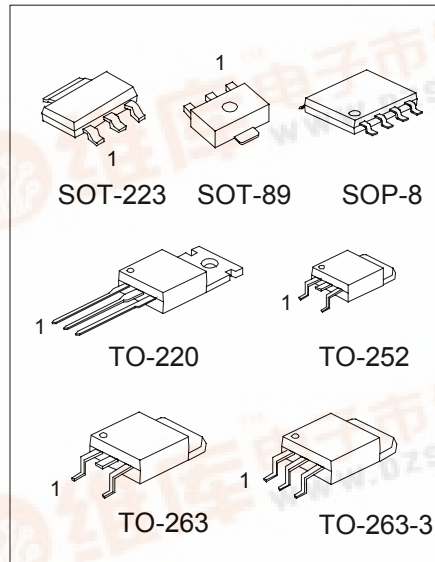


UTC UR233 LINEAR INTEGRATED CIRCUIT

LOW DROP FIXED AND ADJUSTABLE POSITIVE VOLTAGE REGULATORS

DESCRIPTION

The UTC UR233 is a LOW DROP Voltage Regulator able to provide up to 0.8A of Output Current, available even in adjustable version ($V_{ref}=1.25V$). Concerning fixed versions, are offered the following Output Voltages: 1.8V, 2.5V, 2.85V, 3.0V, 3.3V and 5.0V. The device is supplied in: SOT-223, SOT-89, TO-252, TO-263, TO-263-3, SOP-8 and TO-220. The SOT-223, SOT-89, SOP-8, TO-263, TO-263-3 and TO-252 surface mount packages optimize the thermal characteristics even offering a relevant space saving effect. High efficiency is assured by NPN pass transistor. In fact in the case, unlike than PNP one, the Quiescent Current flows mostly into the load. Only a very common $10\mu F$ minimum capacitor is needed for stability. On chip trimming allows the regulator to reach a very tight output voltage tolerance, within $\pm 1\%$ at $25^{\circ}C$. The ADJUSTABLE UR233 is pin to pin compatible with the other standard Adjustable voltage regulators maintaining the better performances in terms of Drop and Tolerance.



SOP-8 1: GND; 2,3,6,7: Vout;
4: Vin; 5,8: NC

FEATURES

- *Low dropout voltage (1V Typ.)
- *Output current up to 0.8A
- *Fixed output voltage of: 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 5.0V
- *Adjustable version availability ($V_{ref}=1.25V$)
- *Internal current and thermal limit
- *Available in $\pm 1\%$ (at $25^{\circ}C$) and 2% in all temperature range
- *Supply voltage rejection: 75dB (TYP)
- *Temperature range: $0^{\circ}C$ to $125^{\circ}C$

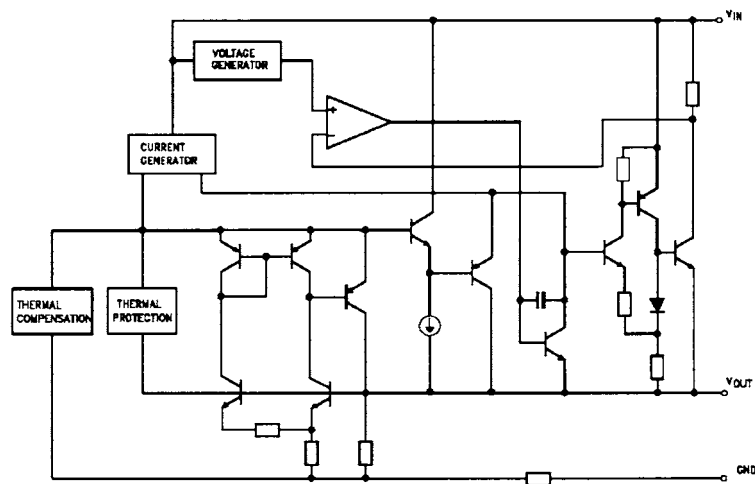


UTC UR233 LINEAR INTEGRATED CIRCUIT

MARKING INFORMATION

PACKAGE	VOLTAGE CODE	PIN CODE	PIN 1	PIN 2	PIN 3	MARKING
SOT-223	18:1.8V	A	GND	OUT	IN	
	25:2.5V	B	OUT	GND	IN	
	28:2.85V	C	GND	IN	OUT	
	30:3.0V	D	IN	GND	OUT	
	33:3.3V					
50:5.0V	AD:ADJ	A	GND	OUT	IN	
SOT-89		B	OUT	GND	IN	
		C	GND	IN	OUT	
		D	IN	GND	OUT	
TO-220 TO-252 TO-263 TO-263-3		A	GND	OUT	IN	
		B	OUT	GND	IN	
		C	GND	IN	OUT	
		D	IN	GND	OUT	

BLOCK DIAGRAM



UTC UR233 LINEAR INTEGRATED CIRCUIT

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
DC Input Voltage	V _{IN}	12	V
Power Dissipation	P _{tot}	12	W
Storage temperature	T _{stg}	-65 ~ +150	°C
Operating Junction Temperature	T _{op}	0 ~ +125	°C

Note: Absolute Maximum Ratings are those value beyond which damage to the device may occur. Functional operation under there condition is not implied. Over the above suggested Max Power Dissipation a Short Circuit could definitively damage the device.

THERMAL DATA

PARAMETER	SYMBOL	VALUE	UNIT
Thermal Resistance Junction-case	R _{th-case}		
SOT-223		15	°C/W
SOP-8		20	°C/W
TO-252		8	°C/W
TO-220		3	°C/W
TO-263		3	°C/W
Thermal Resistance Junction-ambient	R _{thj-amb}		
TO-220		50	°C/W

UTC UR233-1.8 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, T_j=0 to 125°C, C_o=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	V _o	V _{in} =3.8V, I _o =10mA, T _j =25°C	1.782	1.800	1.818	V
Output Voltage	V _o	I _o =0 to 800mA, V _{in} =3.2 to 10V	1.764		1.836	V
Line Regulation	ΔV _o	V _{in} =3.2 to 10V, I _o =0mA		1	6	mV
Load Regulation	ΔV _o	V _{in} =3.2V, I _o =0 to 800mA		1	10	mV
Temperature stability	ΔV _o			0.5		%
Long Term Stability	ΔV _o	1000 hrs, T _j =125°C		0.3		%
Operating Input Voltage	V _{in}	I _o =100mA			12	V
Quiescent Current	I _d	V _{in} ≤10V		5	10	mA
Output Current	I _o	V _{in} =6.8V, T _j =25°C	800	950	1200	mA
Output Noise Voltage	e _N	B=10Hz to 10KHz, T _j =25°C		100		μV
Supply Voltage Rejection	SVR	I _o =40mA, f=120Hz, T _j =25°C, V _{in} =4.8V, V _{ripple} =1V _{pp}	60	75		dB
Dropout Voltage	V _d				1.50	V
Thermal Regulation		T _a =25°C, 30ms Pulse		0.01	0.10	%/W

UTC UR233 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, T_j=0 to 125°C, C_o=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	V _o	V _{in} =4.5V, I _o =10mA, T _j =25°C	±1% 2.475	2.500	2.525	V
			±2% 2.450	2.500	2.550	V
Output Voltage	V _o	I _o =0 to 800mA, T _j =25°C	±2% 2.450		2.550	V
		V _{in} =3.9 to 10V	±4% 2.400		2.600	V
Line Regulation	ΔV _o	V _{in} =3.9 to 10V, I _o =0mA		1	6	mV

UTC UR233 LINEAR INTEGRATED CIRCUIT

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Load Regulation	ΔV_o	$V_{in}=3.9V, I_o=0$ to 800mA		1	10	mV
Temperature stability	ΔV_o			0.5		%
Long Term Stability	ΔV_o	1000 hrs, $T_j=125^\circ C$		0.3		%
Operating Input Voltage	V_{in}	$I_o=100mA$			12	V
Quiescent Current	I_d	$V_{in}\leq 10V$		5	10	mA
Output Current	I_o	$V_{in}=7.5V, T_j=25^\circ C$	800	950	1200	mA
Output Noise Voltage	eN	$B=10Hz$ to 10KHz, $T_j=25^\circ C$		100		μV
Supply Voltage Rejection	SVR	$I_o=40mA, f=120Hz, T_j=25^\circ C, V_{in}=5.5V, V_{ripple}=1V_{pp}$	60	75		dB
Dropout Voltage	V_d				1.50	V
Thermal Regulation		$T_a=25^\circ C, 30ms$ Pulse		0.01	0.10	%/W

UTC UR233-2.85 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, $T_j=0$ to $125^\circ C, C_o=10\mu F$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_o	$V_{in}=4.85V, I_o=10mA, T_j=25^\circ C$	2.82	2.85	2.88	V
Output Voltage	V_o	$I_o=0$ to 800mA, $V_{in}=4.25$ to 10V	2.79		2.91	V
Line Regulation	ΔV_o	$V_{in}=4.25$ to 10V, $I_o=0mA$		1	6	mV
Load Regulation	ΔV_o	$V_{in}=4.25V, I_o=0$ to 800mA		1	10	mV
Temperature stability	ΔV_o			0.5		%
Long Term Stability	ΔV_o	1000 hrs, $T_j=125^\circ C$		0.3		%
Operating Input Voltage	V_{in}	$I_o=100mA$			12	V
Quiescent Current	I_d	$V_{in}\leq 10V$		5	10	mA
Output Current	I_o	$V_{in}=7.85V, T_j=25^\circ C$	800	950	1200	mA
Output Noise Voltage	eN	$B=10Hz$ to 10KHz, $T_j=25^\circ C$		100		μV
Supply Voltage Rejection	SVR	$I_o=40mA, f=120Hz, T_j=25^\circ C, V_{in}=5.85V, V_{ripple}=1V_{pp}$	60	75		DB
Dropout Voltage	V_d				1.50	V
Thermal Regulation		$T_a=25^\circ C, 30ms$ Pulse		0.01	0.10	%/W

UTC UR233-3.0 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, $T_j=0$ to $125^\circ C, C_o=10\mu F$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Output Voltage	V_o	$V_{in}=5V, I_o=10mA, T_j=25^\circ C$	$\pm 1\%$	2.97	3.00	3.03	V
			$\pm 2\%$	2.94	3.00	3.06	V
Output Voltage	V_o	$I_o=0$ to 800 mA $V_{in}=4.5$ to 10V	$\pm 2\%$	2.94		3.06	V
			$\pm 4\%$	2.88		3.12	V
Line Regulation	ΔV_o	$V_{in}=4.5$ to 12V, $I_o=0mA$		1	6	mV	
Load Regulation	ΔV_o	$V_{in}=4.5V, I_o=0$ to 800mA		1	10	mV	
Temperature stability	ΔV_o			0.5		%	
Long Term Stability	ΔV_o	1000 hrs, $T_j=125^\circ C$		0.3		%	
Operating Input Voltage	V_{in}	$I_o=100mA$			12	V	
Quiescent Current	I_d	$V_{in}\leq 12V$		5	10	mA	
Output Current	I_o	$V_{in}=8V, T_j=25^\circ C$	800	950	1200	mA	
Output Noise Voltage	eN	$B=10Hz$ to 10KHz, $T_j=25^\circ C$		100		μV	
Supply Voltage Rejection	SVR	$I_o=40mA, f=120Hz, T_j=25^\circ C, V_{in}=6V, V_{ripple}=1V_{pp}$	60	75		dB	
Dropout Voltage	V_d				1.50	V	

UTC UR233 LINEAR INTEGRATED CIRCUIT

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC UR233-3.3 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Output Voltage	Vo	Vin=5.3V, Io=10mA, Tj=25°C	±1%	3.267	3.300	3.333	V
			±2%	3.235	3.300	3.365	V
Output Voltage	Vo	Io=0 to 800 mA, Vin=4.75 to 10V	±2%	3.235		3.365	V
			±4%	3.160		3.440	V
Line Regulation	ΔVo	Vin=4.75 to 12V, Io=0mA		1	6	mV	
Load Regulation	ΔVo	Vin=4.75V, Io=0 to 800mA		1	10	mV	
Temperature stability	ΔVo			0.5		%	
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%	
Operating Input Voltage	Vin	Io=100mA			12	V	
Quiescent Current	Id	Vin≤12V		5	10	mA	
Output Current	Io	Vin=8.3V, Tj=25°C	800	950	1200	mA	
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		μV	
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=6.3V, Vripple=1Vpp	60	75		DB	
Dropout Voltage	Vd				1.50	V	
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W	

UTC UR233-5.0 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Output Voltage	Vo	Vin=7V, Io=10mA, Tj=25°C	±1%	4.95	5.00	5.05	V
			±2%	4.90	5.00	5.10	V
Output Voltage	Vo	Io=0 to 800mA, Vin=6.5 to 12V	±2%	4.90		5.10	V
			±4%	4.80		5.20	V
Line Regulation	ΔVo	Vin=6.5 to 12V, Io=0mA		1	10	mV	
Load Regulation	ΔVo	Vin=6.5V, Io=0 to 800mA		1	15	mV	
Temperature stability	ΔVo			0.5		%	
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%	
Operating Input Voltage	Vin	Io=100mA			12	V	
Quiescent Current	Id	Vin≤12V		5	10	mA	
Output Current	Io	Vin=10V, Tj=25°C	800	950	1200	mA	
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		μV	
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=8V, Vripple=1Vpp	60	75		dB	
Dropout Voltage	Vd				1.50	V	
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W	

UTC UR233 LINEAR INTEGRATED CIRCUIT

UTC UR233-ADJUSTABLE ELECTRICAL CHARACTERISTICS

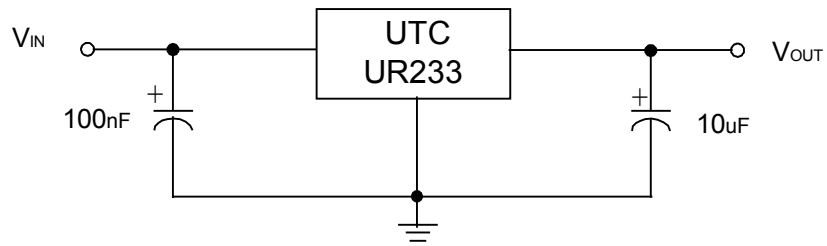
(refer to the test circuits, $T_j=0$ to 125°C , $C_o=10\mu\text{F}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference Voltage	Vref	Vin-VO=2V, Io=10mA, Tj=25°C	1.238	1.25	1.262	V
Reference Voltage	Vref	Io=10 to 800mA, Vin-Vo=1.5 to 10V	1.225		1.275	V
Line Regulation	ΔV_o	Vin-Vo=1.5 to 13.75V, Io=10mA		0.035	0.200	%
Load Regulation	ΔV_o	Vin-Vo=3V, Io=10 to 800mA		0.10	0.400	%
Temperature stability	ΔV_o			0.50		%
Long Term Stability	ΔV_o	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin				12	V
Adjustment Pin Current	Iadj	Vin≤12V		60	120	μA
Adjustment Pin Current Change	ΔI_{adj}	Vin-Vo=1.5 to 10V, Io=10 to 800mA		1	5	μA
Minimum Load Current	Io(min)	Vin=12V		2	5	mA
Output Current	Io	Vin-Vo=5V, Tj=25°C	800	950	1200	mA
Output Noise (%Vo)	eN	B=10Hz to 10KHz, Tj=25°C		0.003		%
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin-Vo=3V, Vripple=1Vpp	60	75		dB
Dropout Voltage	Vd				1.50	V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

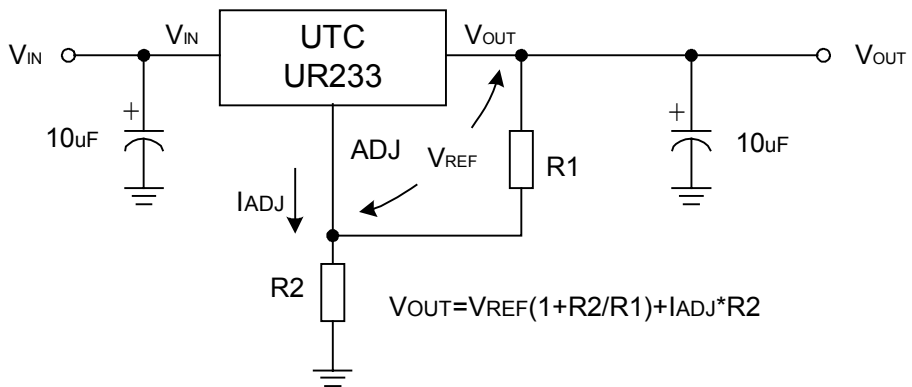
UTC UR233 LINEAR INTEGRATED CIRCUIT

APPLICATION CIRCUIT

FIXED VOLTAGE



ADJUSTABLE



UTCUR233 LINEAR INTEGRATED CIRCUIT

TYPICAL CHARACTERISTICS

Fig.1 Reference Voltage vs. Temperature

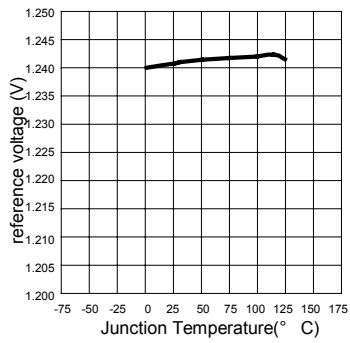


Fig.2 Output Voltage vs. Temperature

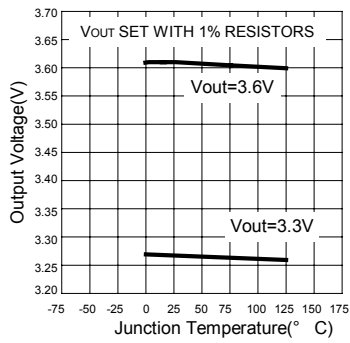


Fig.3 Maximum Power Dissipation

