MINGSTAR ELECTRONIC CORPORATION

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TFT-LCD CONTROLLER LSI (UPS017)

PRELIMINARY SPECIFICATION

MODEL NAME: UPS017

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Approved by	Checked by	Prepared by
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Contents :

A.General description:

This timing controller is a synchronizing signal controlling CMOS gate-array LSI for Mingstar LCD module. It provides all the necessary control timing signals to the LCD source and gate drivers. With external VCO as the master clock, the controller has built-in phase locked loop system which can synchronize the master clock with the horizontal and vertical Sync. signals from a classical TV system.
This IC support Mingstar's 16:9 aspect ratio series TFT-LCD modules and it also provides different zoom in/out display mode.

B. Feature:

* Programmable resolution mode.
* Low Power Consumption.
* Single Supply : +5.0 Volts.
* 48 pins LQFP.
* Shift Clocks Signal for the Source Driver. (3 - ϕ Clock)
* Line Inversion Driving Scheme.
* NTSC TV Standard System .
* Master Clock Frequency : 30 MHz max.
* Provides Timing Scan Signals for Left / Right and Up / Down Shift Control.
* Built-in zoom in/zoom out display mode selection.
* Display Timing Range = 49.4 μ s

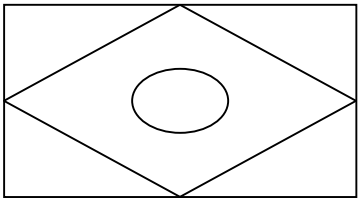
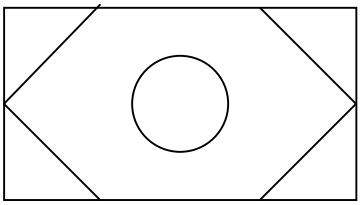
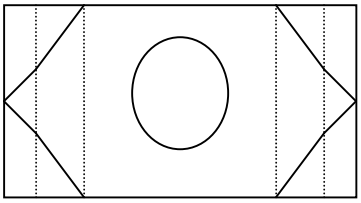
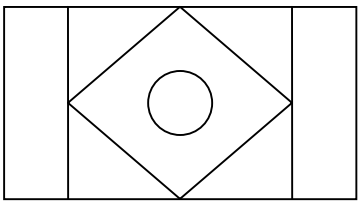
C.Pin description:

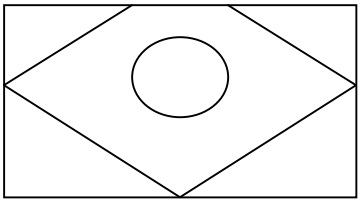
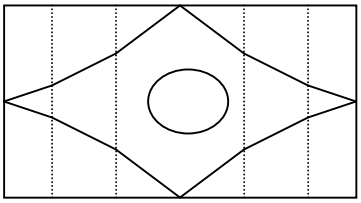
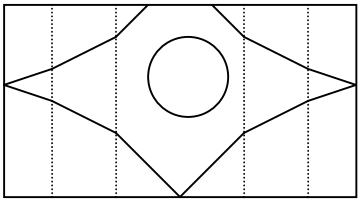
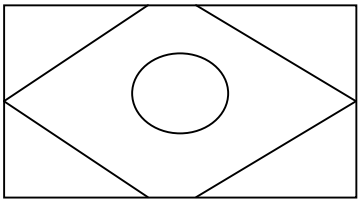
Pin no	Symbol	I/O	Description	Remark
1	NPFRP	O	Inverted output of PFRP_OUT	
2	HZ_OUT	O	Zoom in control signal	
3	HOE_OUT	O	Output enable control signal for source driver	
4	VOE_OUT	O	Output enable control signal for gate driver	
5	D_MOD	I	Digital mode setting pin.	
6	FDV_OUT	O	Test pin.	
7	GND		Ground	
8	MOD_OUT	O	Simultaneous/sequential sampling control setting of LCD.	
9	RES_C	I	Horizontal resolution mode setting pin . H: 1440, L:1200	
10	VO2	O	Gate driver start pulse. When (1).UDC=H, VO2 is output pin of start pulse. (2).UDC=L, VO2 is in high impedance state.	
11	VO1	O	Gate driver start pulse. when (1).UDC=H, VO1 is in high impedance state. (2).UDC=L, VO1 is output pin of start pulse.	
12	VCC			
13	STHL	O	Source driver start pulse. when (1).L_R=H, STHL is in high impedance state. (2).L_R=L, STHL is output pin of start pulse.	
14	STHR	O	Source driver start pulse. when (1).L_R=H, STHR is output pin of start pulse. (2).L_R=L, STHR is in high impedance state.	
15	PD_OUT	O	Negative polarity phase detector output.	
16	V_CK	O	Gate driver shift clock.	
17	CK1A	O	Source driver shift clock $\phi 1$.	
18	CK2A	O	Source driver shift clock $\phi 2$.	
19	CK3A	O	Source driver shift clock $\phi 3$.	
20	ZX1	I	Zoom in/out modes setting	Note 2
21	ZX2	I	Zoom in/out modes setting	Note 2
22	ZX3	I	Zoom in/out modes setting	Note 2
23	GND		Ground	
24	VCC			
25	F_OUT	O	Inverted F_IN signal output	
26	F_IN	I	Master system clock input. This input pin is connected to the external VCO output for system clock timing & synchronization to the TV sync. Signals through the phase locked loop block.	

Pin no	Symbol	I/O	Description	Remark
27	VSY_OUT	O	Negative polarity vertical sync. output	
28	HSYW	O	Test pin	Note 1
29	GR_IN	I	Global reset. It should be connected to V_{CC} in normal operation. If connected to GND, the controller is in reset state.	
30	V_IN	I	Vertical synchronization signal input from the sync. Separator of a TV system. It should be a negative polarity.	
31	UD_OUT	O	Inverted UDC signal output.	
32	ZTC	I	Test pin	Note 1
33	AUXS	I	Setting pin of zoom in/out control. Please set to “L”.	
34	HSY_OUT	O	Negative polarity horizontal sync. output.	
35	Csync	I	Positive polarity composite sync. input.	
36	GND		Ground	
37	UDC	I	Up / Down scan control pin. (1) Normal Scan : set to Low (2) Reverse Scan : set to High	
38	PD_SW	I	Horizontal noise counter setting pin.	
39	L_R	I	Left / Right scan control pin. (1) Normal Scan : set to Low (2) Reverse scan : set to High	
40	LR_A	O	Inverted L_R signal output.	
41	CSYN_OUT	O	Test pin.	Note 1
42	TC	I	Test pin	Note 1
43	NPC	I	It should be pulled to Vcc in normal operation.	
44	PFRP_OUT	O	Polarity alternating signal for V_{com}	
45	NP_SW	I	Test pin	
46	CP_OUT	O	Compare pulse output.	
47	CP_IN	I	Compare pulse input.	
48	VCC			

Note 1 : All these pins should be electrically opened.

Note 2 : Zoom in/out display mode setting :

Display mode	ZX1	ZX2	ZX3	Display Characteristics (4:3 aspect-ratio input signal)	Note
Full	H	H	H		Input signals are displayed on full screen. (To display 4 : 3 signal on 16 : 9 screen)
Zoom1	L	H	H		Central 176 lines of input signals are displayed on full screen. (Vertically extension, zoom factor = 4/3)
Zoom-Wide1	H	L	H		Central 176 lines of input signals are displayed on full screen. (Vertically extension and different horizontal timing scaling.)
Normal	L	L	H		Input signal (4:3) are displayed on center 75% screen. (4 :3 aspect-ratio)

Display Mode	ZX1	ZX2	Zx3	Display Characteristics (4:3 aspect-ratio input signal)	Note
Zoom2	H	H	L		Lower 205 lines of input signals are displayed on full screen. (Zoom factor = 8/7, vertically offset extension)
Wide	L	H	L		Input signals are displayed on full screen. (Different horizontal timing scaling.)
Zoom-Wide2	H	L	L		Lower 205 lines of input signal are displayed on full screen. (Vertically extension and different horizontal timing scaling.)
Zoom3	L	L	L		Center 205 lines of input signal are displayed on full screen. (Vertically extension, Zoom factor = 8/7)

D.DC characteristics

1.Absolute maximum ratings:

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power supply	-0.3 to 6.0	V
V_{IN}	Input voltage	-0.3 to VCC + 0.3	V
V_{OUT}	Output voltage	-0.3 to VCC + 0.3	V
T_{STG}	Storage temperature	-40 to 125	℃

2.Recommended operating conditions:

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power supply	4.5	5.0	5.5	V
V_{IN}	Input voltage	0	-	V_{CC}	V
T_{OPR}	Operating temperature	-20	-	85	℃

3.General DC characteristics:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	Remark
I_{IL}	Input low current	no pull-up or pull-down	-1	-	1	μA	
I_{IH}	Input high current	no pull-up or pull-down	-1	-	1	μA	
I_{OZ}	Tri-state leakage current		-10	-	10	μA	
C_{IN}	Input capacitance		-	3	-	PF	
C_{OUT}	Output capacitance		3	-	6	PF	
V_{IL}	Logic input low voltage	CMOS	-	-	0.3Vcc	V	
V_{SIL}	Schmitt input low voltage	CMOS	-	1.76	-	V	Note 1
V_{IH}	Logic input high voltage	CMOS	0.7Vcc	-	-	V	
V_{SIH}	Schmitt input high voltage	CMOS	-	3.2	-	V	Note 1
V_{OL}	Output low voltage	I_{OL}=4mA	-	-	0.4	V	
V_{OH}	Output high voltage	I_{OH}=4mA	3.5	-	-	V	Note 2
R_I	Input pull up/down resistance	V_{IL}=0V or V_{IH}=V_{CC}	-	50	-	KΩ	

Note 1: The applicable pins are F_IN, V_IN, Csync, CP_IN.
Note 2: When I_{OH} = 3mA , V_{OH} Min.= 4V.

4.Current consumption for 5 volts operating:

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Loading
I_{IN}	Current consumption	Vcc=5V	(12)	(18)	(25)	mA	MTL070D01W-XX Series
			(10)	(15)	(21)	mA	MTL056D01W-XX Series

E. AC characteristics

1.Timing condition

(Ⅰ) 1440 resolution mode.

a.Input signal characteristics(In non-zoom display mode)

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
F_IN period	t_{OSC}	33	34	35	ns	
Csync period	T_H	61.5	63.5	65.5	μs	
Csync pulse width	t_{CSYN}	4	4.7	5.4	μs	
Csync rising time	T_{Cr}	-	-	700	ns	
Csync falling time	T_{Cf}	-	-	300	ns	
V_IN pulse width	t_{VSY}	1	3	5	t_H	
V_IN rising time	T_{Vr}	-	-	700	ns	
V_IN falling	T_{Vf}	-	-	1.5	μs	
Horizontal lines per field		256	262.5	268	line	Note 1

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b.Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level Pulse width	t_{CPH}	-	3	-	t_{OSC}	CK1A~CK3A
Clock pulse duty	t_{CWH}	40	50	60	%	CK1A~CK3A
3ϕ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /2	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HSY_OUT pulse width	t_{HSY}	-	4.62	-	μs	
HOE_OUT pulse width	t_{OEH}	-	1.22	-	μs	
Sample & hold disable time	t_{DIS1}	-	8.17	-	μs	
VOE_OUT pulse width	t_{OEV}	-	4.62	-	μs	
V_CK pulse width	t_{CKV}	-	3.81	-	μs	
CP_OUT period	t_{CP}	-	1	-	t_H	
CP_OUT pulse duty	t_{WCP}	-	1/2	-	t_H	
HSY_OUT-HOE_OUT timing difference	t_1	-	3.38	-	μs	
HSY_OUT-V_CK timing difference	t_2	-	2.86	-	μs	
HSY_OUT-VOE_OUT timing difference	t_3	-	0.816	-	μs	
HSY_OUT-CP_OUT timing difference	t_4	-	3.26	-	μs	
VO1/2 setup time	t_{SUV}	-	2	-	μs	
VO1/2 pulse width	t_{STV}	-	1	-	t_H	

VSY_OUT-VO1/2 timing difference(UDC="H")	t_{VS1}	-	19	-	t_H	
VSY_OUT-VO1/2 timing difference(UDC="L")	t_{VS2}	-	19	-	t_H	
HOE_OUT-VO1/2 timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

(Ⅱ) 1200 resolution mode.

a.Input signal characteristics (In non-zoom display mode)

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
F_IN period	t_{OSC}	40.3	41.6	43	ns	
Csync period	T_H	61.5	63.5	65.5	μs	
Csync pulse width	t_{CSYN}	4	4.7	5.4	μs	
Csync rising time	T_{Cr}	-	-	700	ns	
Csync falling time	T_{Cf}	-	-	300	ns	
V_IN pulse width	t_{VSY}	1	3	5	t_H	
V_IN rising time	T_{Vr}	-	-	700	ns	
V_IN falling	T_{Vf}	-	-	1.5	μs	
Horizontal lines per field		256	262.5	268	line	Note 1

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b.Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level Pulse width	t_{CPH}	-	3	-	t_{OSC}	CK1A~CK3A
Clock pulse duty	t_{CWH}	40	50	60	%	CK1A~CK3A
3ϕ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /2	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HSY_OUT pulse width	t_{HSY}	-	4.64	-	μs	
HOE_OUT pulse width	t_{OEH}	-	1.49	-	μs	
Sample & hold disable time	t_{DIS1}	-	7.97	-	μs	
VOE_OUT pulse width	t_{OEV}	-	5.13	-	μs	
V_CK pulse width	t_{CKV}	-	4.14	-	μs	
CP_OUT period	t_{CP}	-	1	-	t_H	
CP_OUT pulse duty	t_{WCP}	-	1/2	-	t_H	
HSY_OUT-HOE_OUT timing difference	t_1	-	3.13	-	μs	
HSY_OUT-V_CK timing difference	t_2	-	2.49	-	μs	
HSY_OUT-VOE_OUT timing difference	t_3	-	1.49	-	μs	

HSY_OUT-CP_OUT timing difference	t_4	-	2.98	-	μs	
VO1/2 setup time	t_{SUV}	-	2.00	-	μs	
VO1/2 pulse width	t_{STV}	-	1	-	t_H	
VSY_OUT-VO2 timing difference(UDC="H")	t_{VS1}	-	19	-	t_H	
VSY_OUT-VO1 timing difference(UDC="L")	t_{VS2}	-	19	-	t_H	
HOE_OUT-VO1/2 timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

(III) Zoom in/out display mode

a. 1440 mode

Zoom mode			Horizontal display Start	Vertical display Start
ZX1	ZX2	ZX3		
L	L	L	12.94us	33H
H	L	L	12.98us	45H
L	H	L	12.98us	19H
H	H	L	12.94us	45H
L	L	H	8.83us	19H
H	L	H	12.98us	48H
L	H	H	12.94us	48H
H	H	H	12.94us	19H
REMARK			From falling edge of HSY_OUT to rising edge of STHR(L)	From falling edge of VSY_OUT to rising edge of VO1(2)

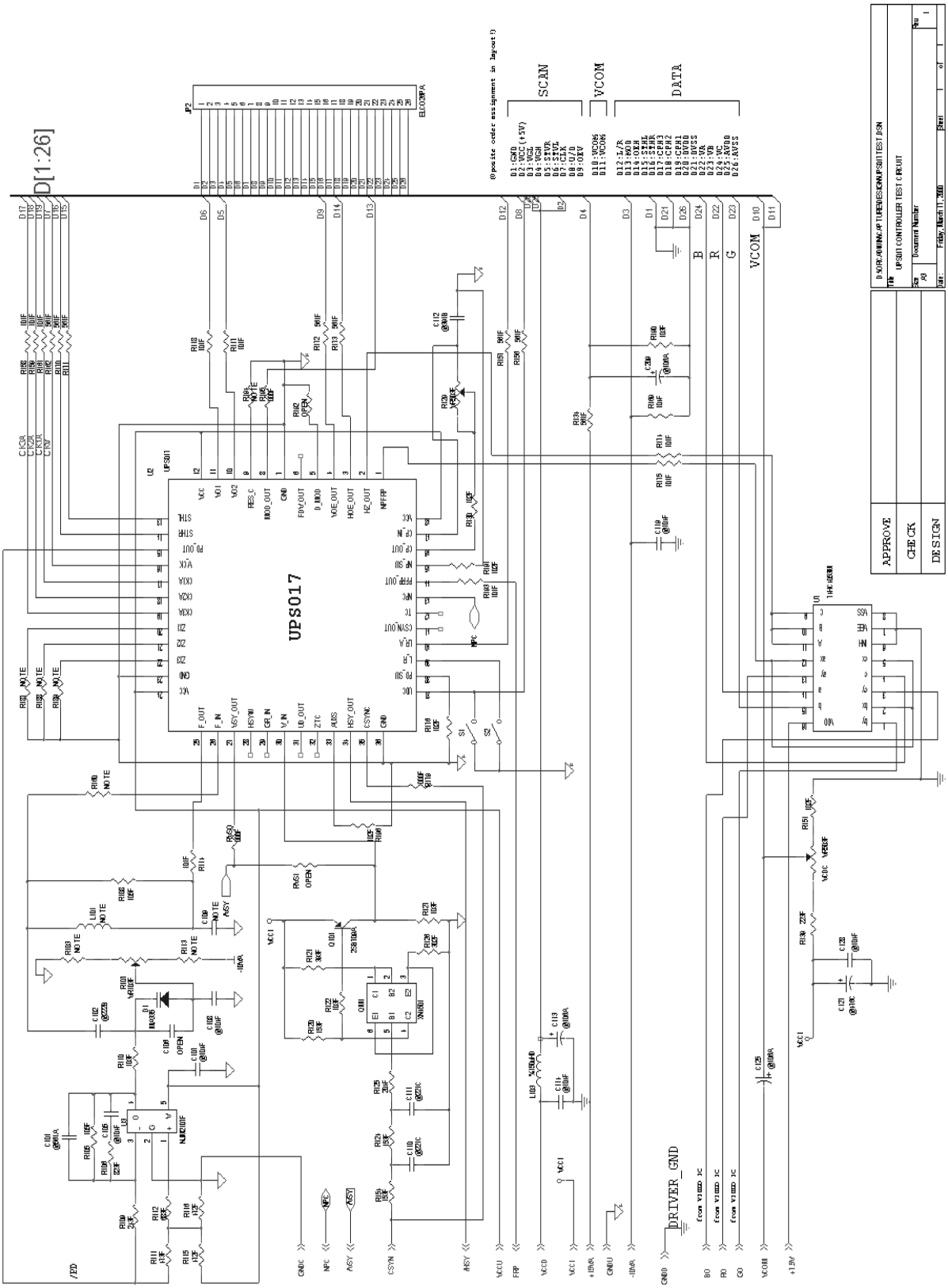
b. 1200 mode

Zoom mode			Horizontal display Start	Vertical display Start
ZX1	ZX2	ZX3		
L	L	L	12.59us	33H
H	L	L	12.65us	45H
L	H	L	12.65us	19H
H	H	L	12.59us	45H
L	L	H	8.65us	19H
H	L	H	12.65us	48H
L	H	H	12.59us	48H
H	H	H	12.59us	19H
REMARK			From falling edge of HSY_OUT to rising edge of STHR(L)	From falling edge of VSY_OUT to rising edge of VO1(2)

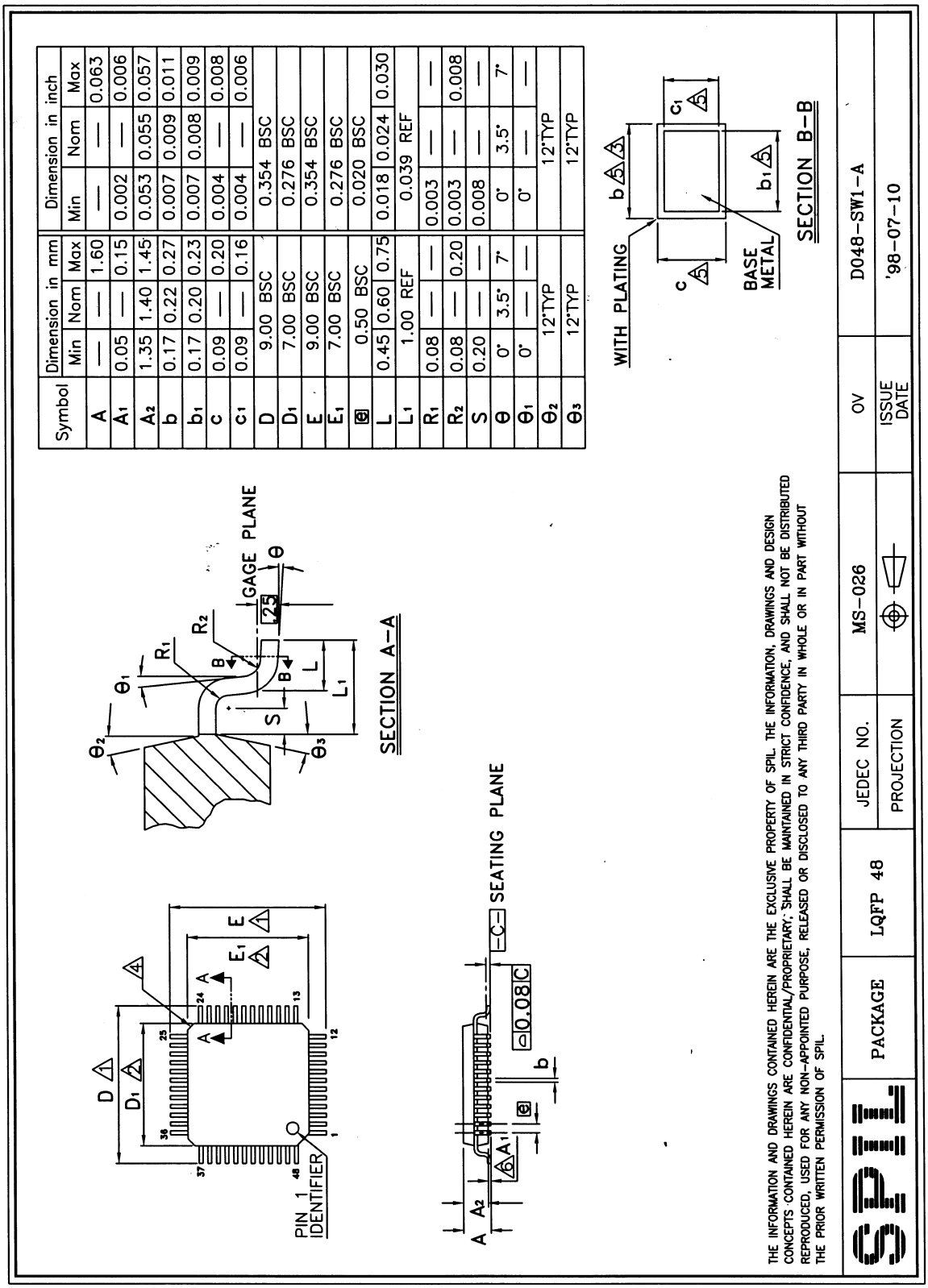
2.Timing diagram

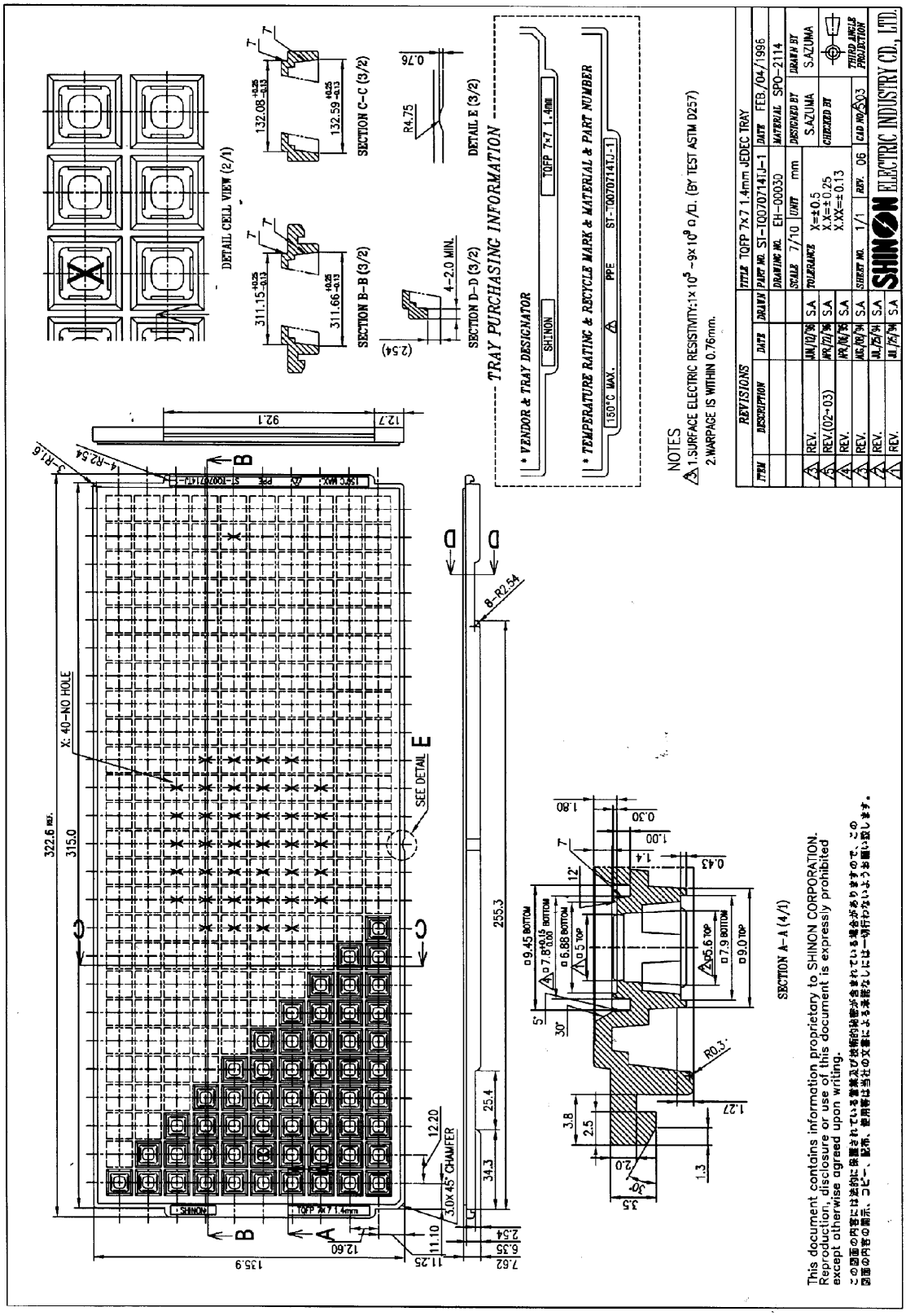
Please refer to the attached drawing. from Fig.1 to Fig.4.

F. Test circuit



G. Package information





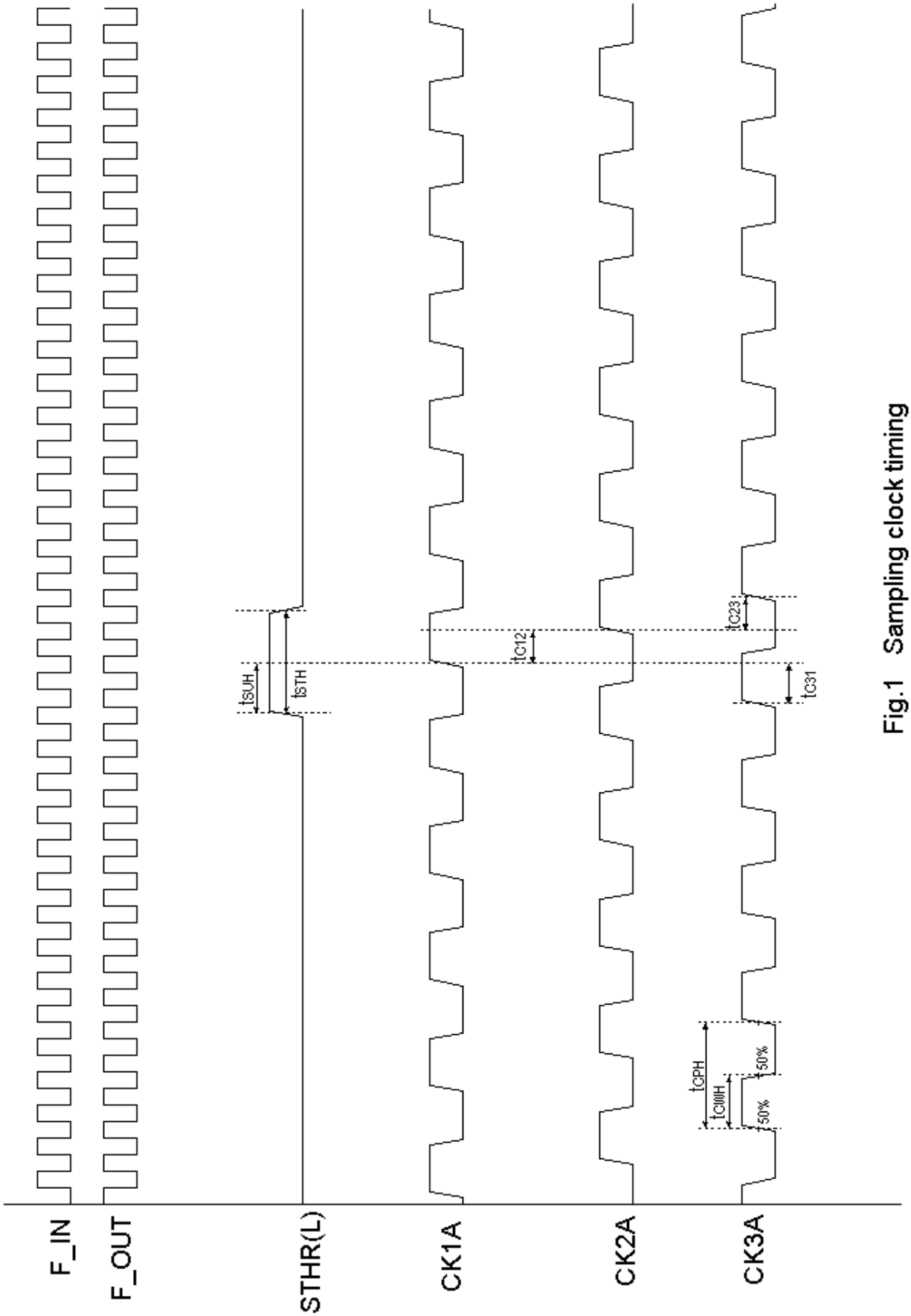


Fig.1 Sampling clock timing

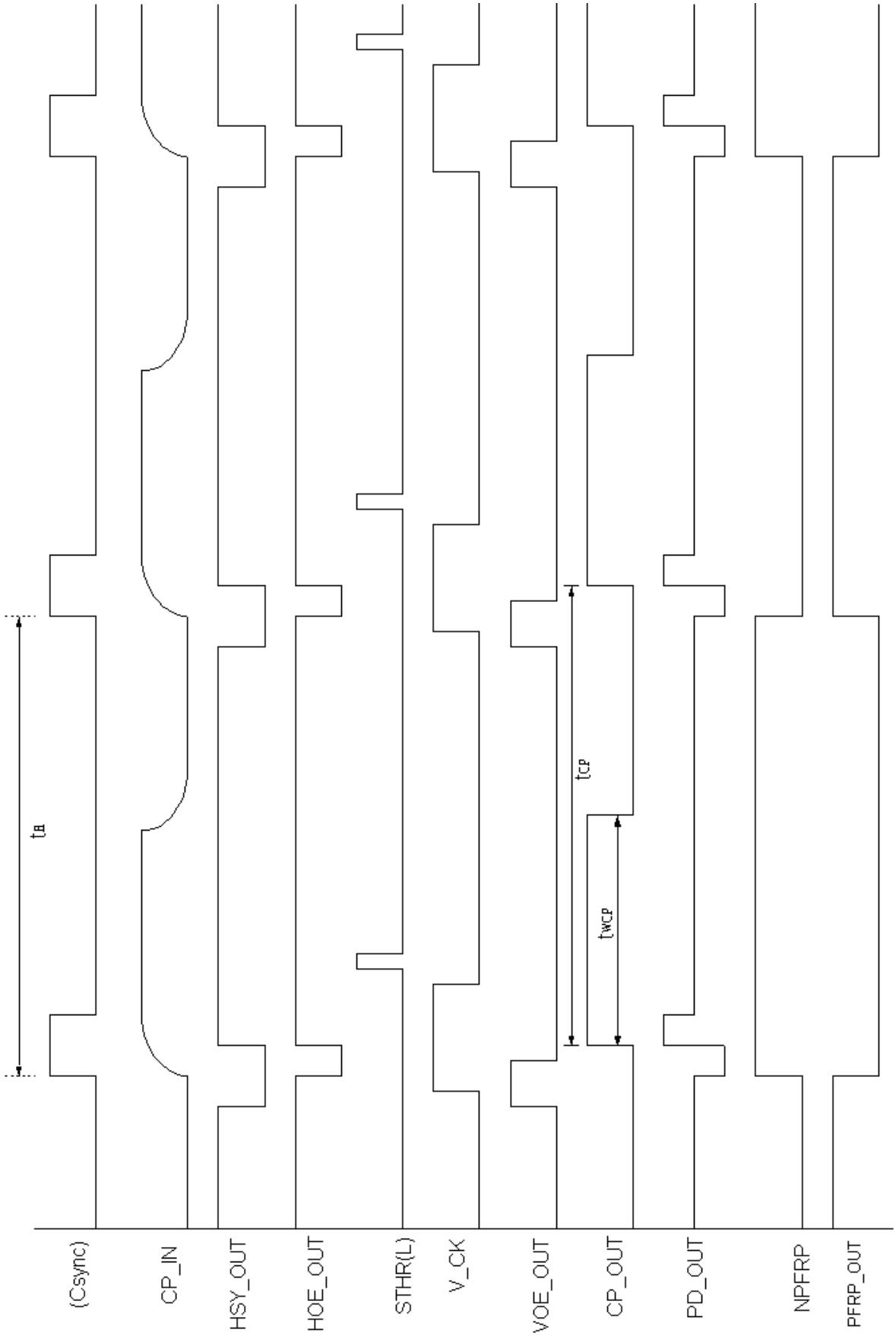


Fig.2 (a) Horizontal timing

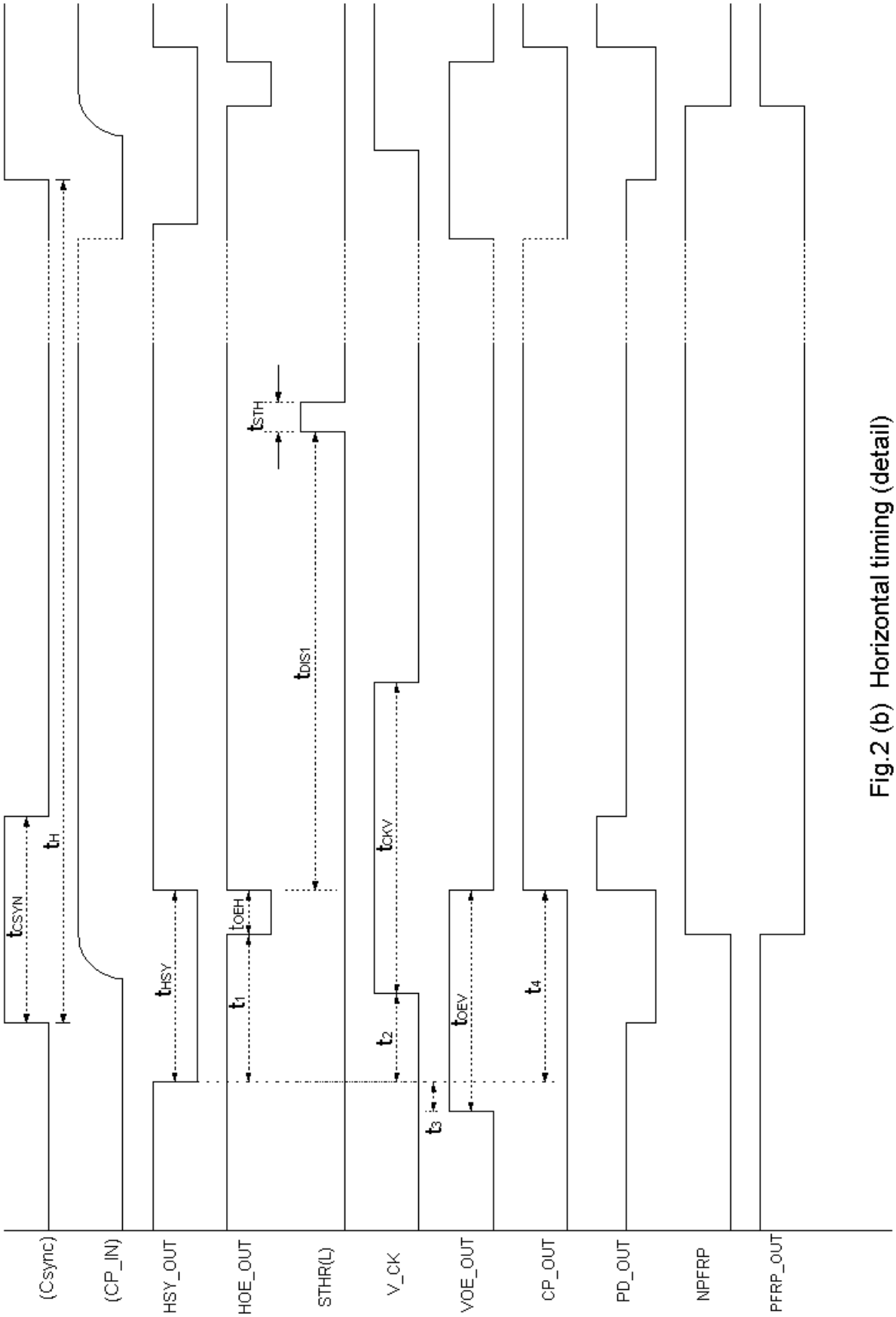


Fig.2 (b) Horizontal timing (detail)

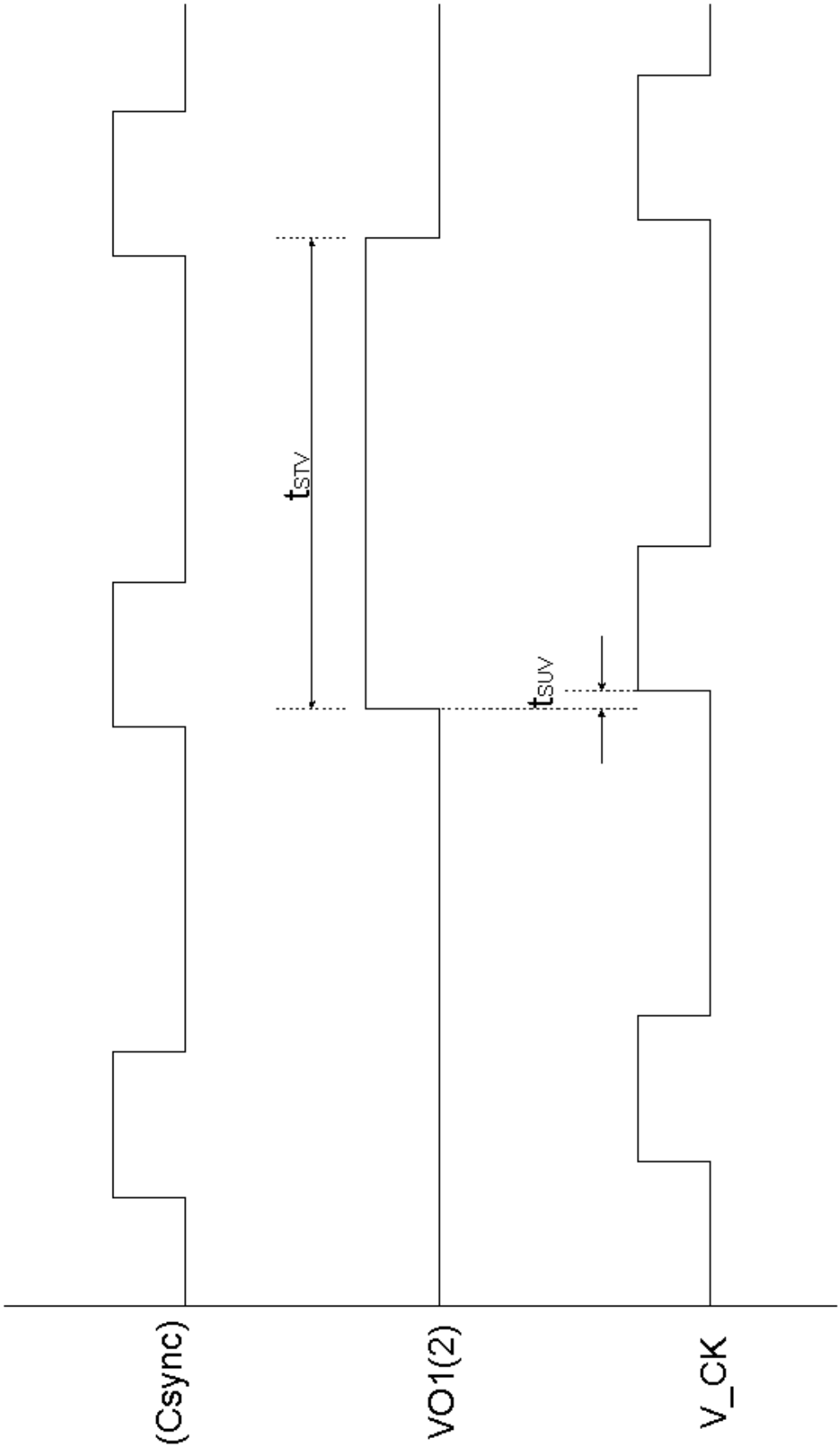


Fig.3 Vertical shift clock timing

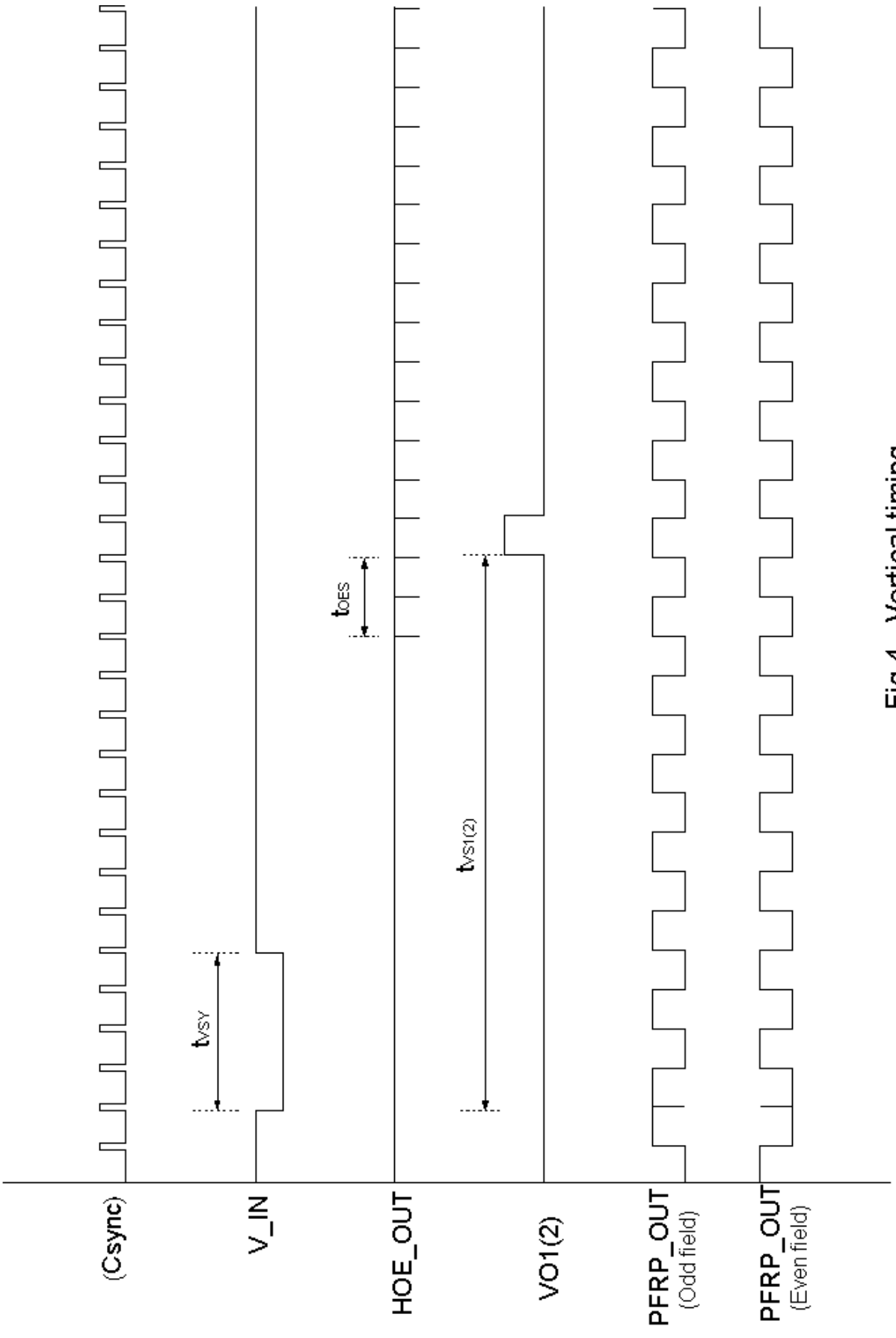


Fig.4 Vertical timing

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