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T-74-11-01

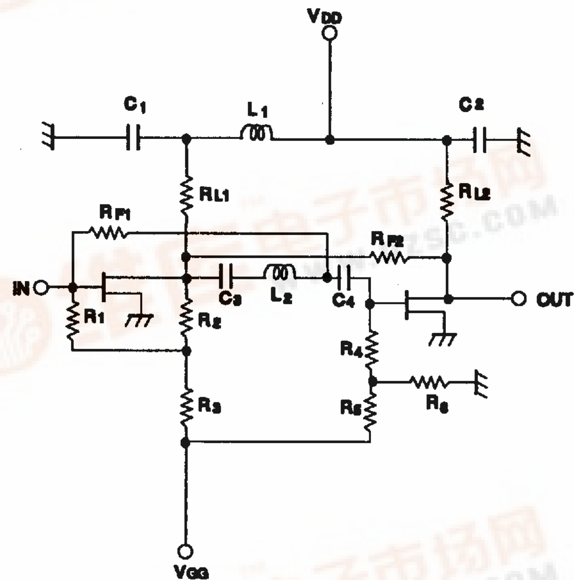
MEDIUM POWER WIDE-BAND AMPLIFIER

UPG101B UPG101P

FEATURES

- **ULTRA WIDE BAND:** 50 MHz to 3 GHz
- **MEDIUM POWER:** +18 dBm TYP at f = 50 MHz to 3 GHz
- **INPUT/OUTPUT IMPEDANCE MATCHED TO 50 Ω**
- **HERMETICALLY SEALED PACKAGE ASSURES HIGH RELIABILITY**
- **WIDE OPERATING TEMPERATURE RANGE**

EQUIVALENT CIRCUIT



DESCRIPTION

The UPG101 is a GaAs monolithic integrated circuit designed as a medium power amplifier from 50 MHz to 3 GHz. The device is suitable for the IF stage in a microwave communication system and measurement equipment where medium power is required.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{DD} = +8 V, V_{GG} = -5 V, f = 0.05 to 3 GHz, Z_S = Z_L = 50Ω)

	PART NUMBER PACKAGE OUTLINE		UPG101B, UPG101P B08, CHIP		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I_{DD}	Drain Bias Current, RF Off	mA	70	100	140
I_{GG}	Gate Bias Current, RF Off	mA		1.0	3.0
G_P	Power Gain	dB	12	14	
ΔG_P	Gain Flatness	dB			±1.5
P_{1dB}	Output Power at 1 dB Gain Compression Point	dBm	+16	+18	
NF	Noise Figure	dB		5	7
RL_{IN}	Input Return Loss	dB	6	8	
RL_{OUT}	Output Return Loss	dB	6	8	
ISOL	Isolation	dB	30	40	
R_{TH}	Thermal Resistance (Channel to Case)	°C/W			33

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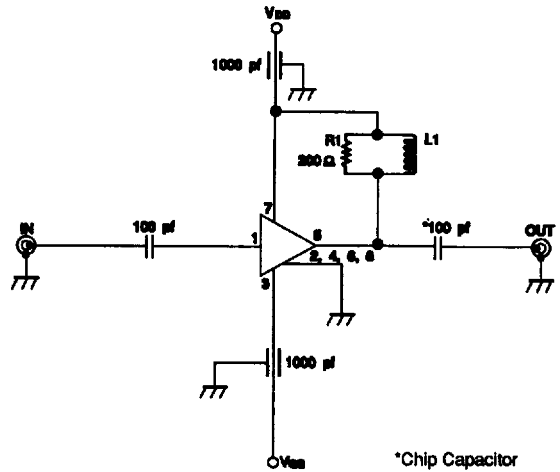
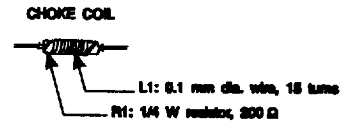
ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD}	Drain VoltageV	+10	
V_{GG}	Gate VoltageV	-8	
V_{IN}	Input VoltageV	-5 to +0.6	
P_{IN}	Input Power	dBm	+15
P_T[1,2]	Total Power Dissipation	W	1.5
T_{OP}	Operating Temperature	°C	-65 to +125
T_{STG}	Storage Temperature	°C	-65 to +175

Notes:
1. $T_{CASE} \leq 125°C$.
2. Maximum allowable power dissipation may be exceeded if V_{DD} is applied without V_{GG} or if V_{GG} is removed before V_{DD}.

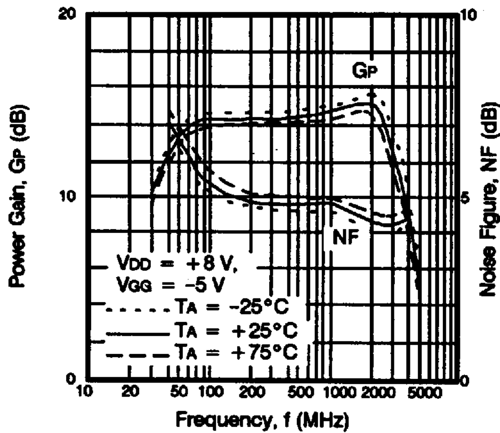
TEST CIRCUIT



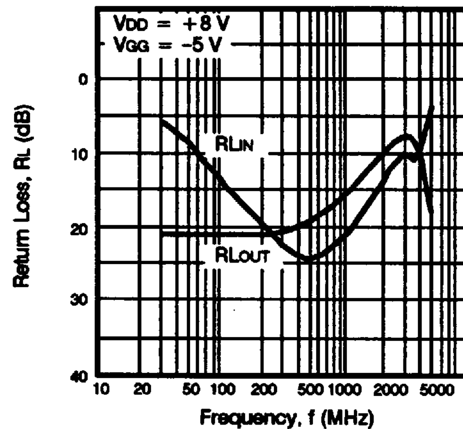


TYPICAL PERFORMANCE CURVES ($T_A = 25°C$)

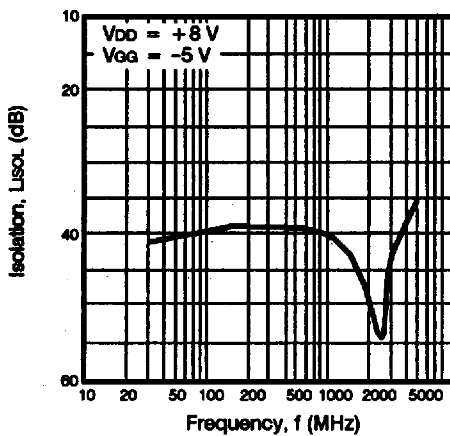
POWER GAIN AND NOISE FIGURE vs. FREQUENCY



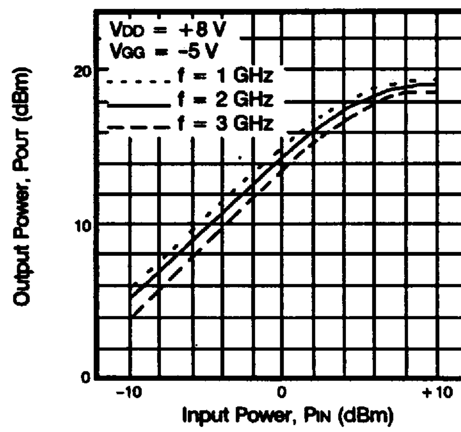
INPUT AND OUTPUT RETURN LOSS vs. FREQUENCY



ISOLATION vs. FREQUENCY

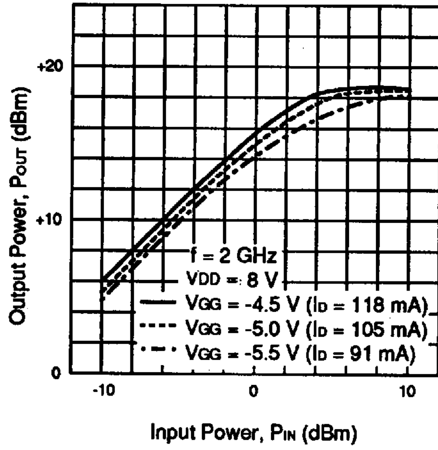


OUTPUT POWER vs. INPUT POWER AND FREQUENCY

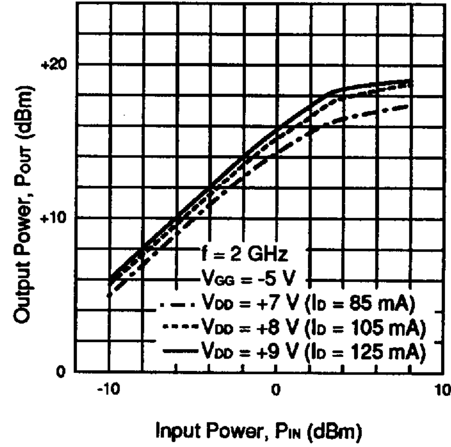


TYPICAL PERFORMANCE CURVES ($T_A = 25°C$)

OUTPUT POWER vs. INPUT POWER AND GATE VOLTAGE

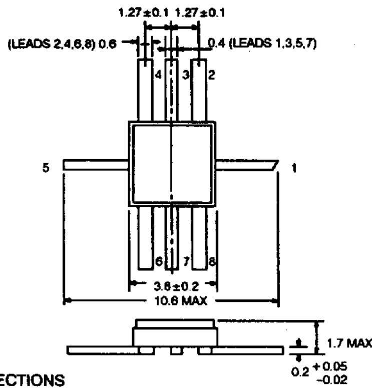


OUTPUT POWER vs. INPUT POWER AND DRAIN VOLTAGE



OUTLINE DIMENSIONS (Units in mm)

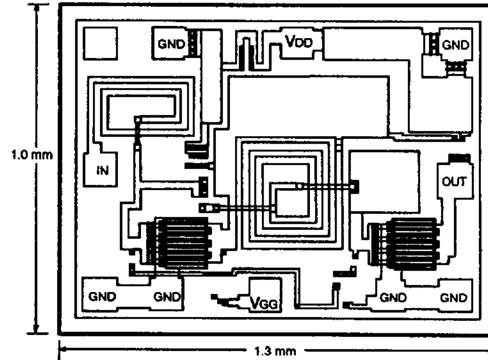
UPG101B
OUTLINE B08



LEAD CONNECTIONS

1. Input
2. GND
3. V_{GG}
4. GND
5. Output
6. GND
7. V_{DD}
8. GND

UPG101P
CHIP



Notes:

Bonding Pad Size: 100 μm Square
Distance Between Chip Edge and Die Edge: 70 μm
Chip Thickness: 140 ±10 μm
Bonding Wire: 25 or 30 μm Diameter Au Wire
Bonding: 10 Wires, TCB at 260 ± 10°C
Mounting: AuSn preform, 0.5 x 0.5 x 0.05 (mm) at 315 ± 10°C

It is critical that GND points be connected to the carrier ground with the shortest possible wire.

CASCADED AMPLIFIER CIRCUIT DIAGRAM[1]