T-74-13-01

NEC®

LOW NOISE WIDE-BAND AMPLIFIER

UPG100B UPG100P

FEATURES

- **ULTRA WIDE BAND:** 50 MHz to 3 GHz
- **LOW NOISE:** 2.7 dB TYP at f = 50 MHz to 3 GHz
- **INPUT/OUTPUT IMPEDANCE MATCHED TO 50 Ω**
- **HERMETIC SEALED PACKAGE ASSURES HIGH RELIABILITY**

DESCRIPTION AND APPLICATIONS

The UPG100 is a GaAs monolithic integrated circuit designed as a low noise amplifier from 50 MHz to 3 GHz. The device is most suitable for the IF stage of microwave communication and measurement equipment that require a low noise amplifier.

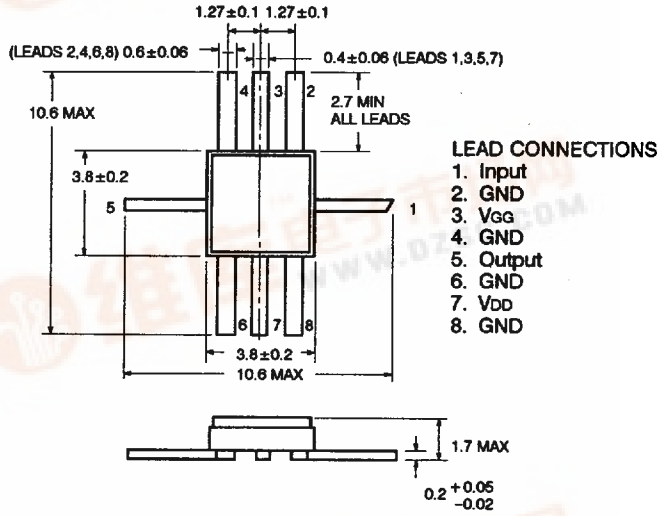
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD}	Drain Voltage	V	+8
V_{GG}	Gate Voltage	V	-8
V_{IN}	Input Voltage	V	-3 to +0.6
P_{IN}	Input Power	dBm	+15
P_T*	Total Power Dissipation	W	1.5
T_{OP}	Operating Temperature	°C	-65 to +125
T_{STG}	Storage Temperature	°C	-65 to +175

*T_{CASE} (T_C) ≤ 125°C

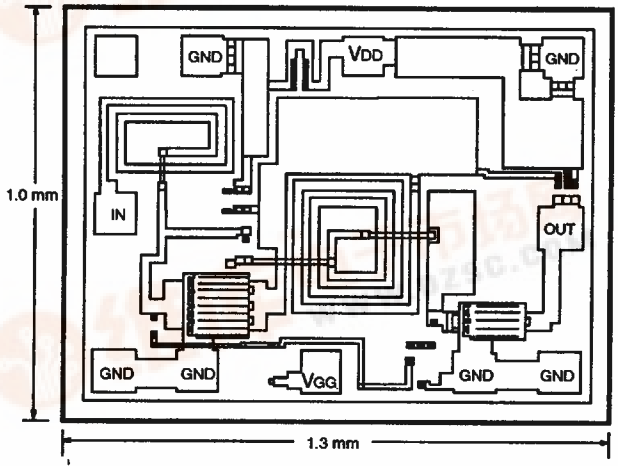
OUTLINE DIMENSIONS (Units in mm)

OUTLINE B08



LEAD CONNECTIONS
1. Input
2. GND
3. V_{GG}
4. GND
5. Output
6. GND
7. V_{DD}
8. GND

UPG100P (CHIP)



Notes: Bonding Pad Size: 100 µm Square
Distance between Bonding Pad Outer Edge and Die Edge: 70µm Typical
Chip Thickness: 140 ± 10 µm

RECOMMENDED CHIP ASSEMBLY CONDITIONS

DIE ATTACHMENT

Atmosphere:	N_2 gas
Temperature:	320 ± 5°C
Preform Material:	AuSn: 0.5 x 0.5 x 0.05 (mm), 1 piece (Hard solder such as AuSi or AuGe which has a higher melting point than AuSn should not be used)
Base Material:	CuW, Cu, KOVAR (Other material should not be used)

Epoxy Die Attach is not recommended.

BONDING

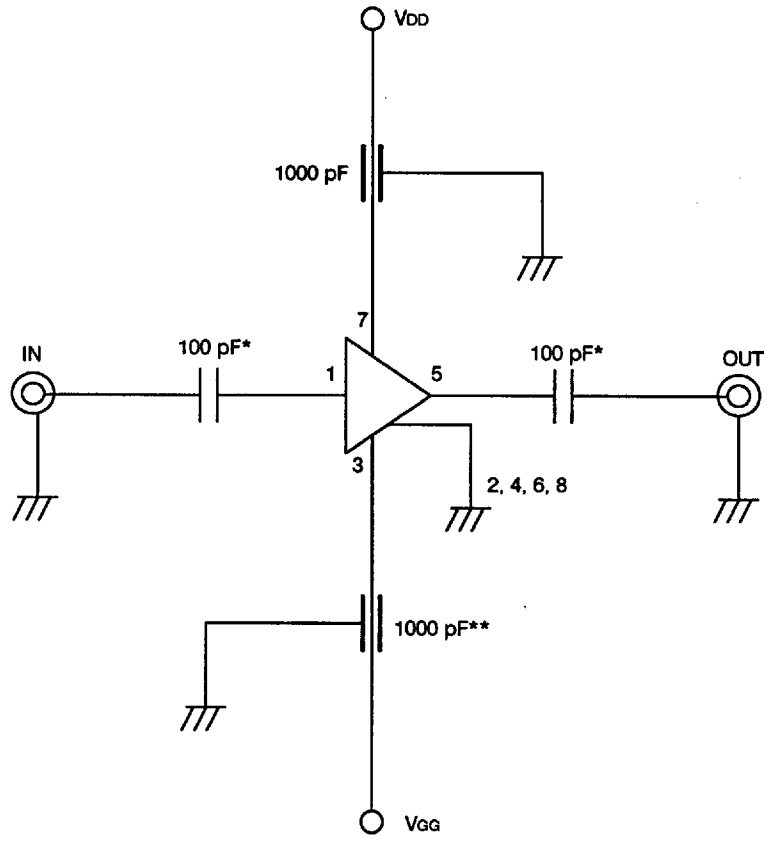
Machine:	TCB (USB is not recommended)
Wire:	30 µm diameter Au wire, 10 wires
Temperature:	260 ± 5°C
Stage Force:	31 ± 3 g
Atmosphere:	N_2 gas

It is critical that GND points be connected to the ground with the shortest possible wire.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER PACKAGE OUTLINE			UPG100B, UPG110P B08 , CHIP		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I_{DD}	Drain Bias Current at V_{DD} = +5 V, V_{GG} = -5 V, RF OFF	mA	30	45	60
I_{GG}	Gate Bias Current at V_{DD} = +5 V, V_{GG} = -5 V, RF OFF	mA		0.7	1.5
G_P	Power Gain at V_{DD} = +5 V, V_{GG} = -5 V, f = 0.05 to 3 GHz	dB	14	16	
ΔG_P	Gain Flatness at V_{DD} = +5 V, V_{GG} = -5 V, f = 0.05 to 3 GHz	dB			±1.5
NF	Noise Figure at V_{DD} = +5 V, V_{GG} = -5 V, f = 0.05 to 3 GHz	dB		2.7	3.5
R_{LIN}	Input Return Loss at V_{DD} = +5 V, V_{GG} = -5 V, f = 0.05 to 3 GHz	dB	7	10	
R_{LOUT}	Output Return Loss at V_{DD} = +5 V, V_{GG} = -5 V, f = 0.05 to 3 GHz	dB	7	10	
L_{ISOL}	Isolation at V_{DD} = +5 V, V_{GG} = -5 V, f = 0.05 to 3 GHz	dB	30	40	
P_{1dB}	Output Power at 1 dB Gain Compression Point, V_{DD} = +5 V, V_{GG} = -5 V, f = 0.05 to 3 GHz	dBm	+3	+6	

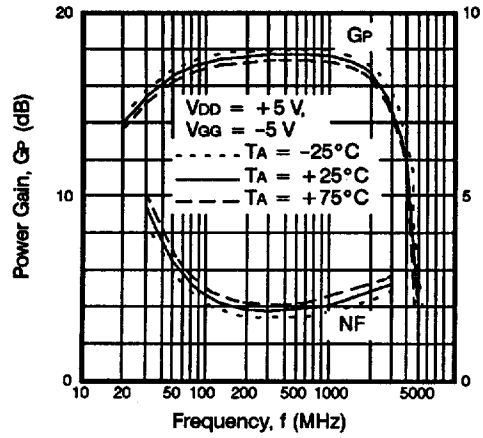
TEST CIRCUIT



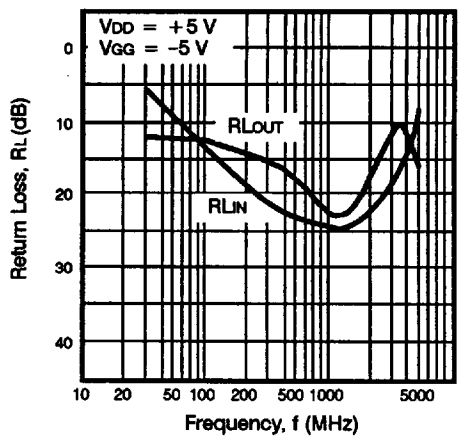
*Chip Capacitor
**Recommended when cascading UPG100 with NEC's UPG100, 101, 103B's.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C)

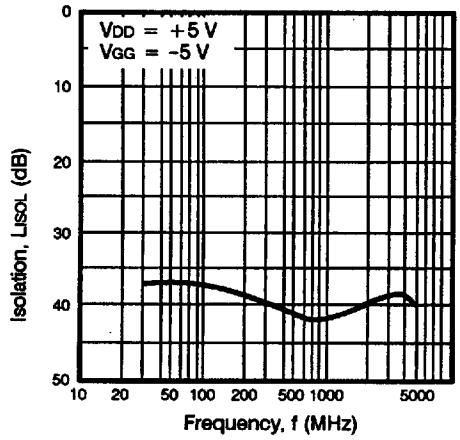
POWER GAIN AND NOISE FIGURE vs. FREQUENCY



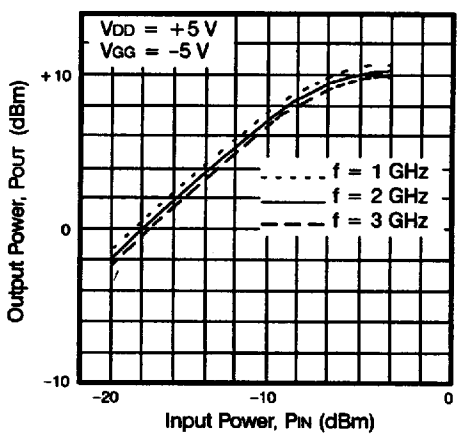
INPUT AND OUTPUT RETURN LOSS vs. FREQUENCY



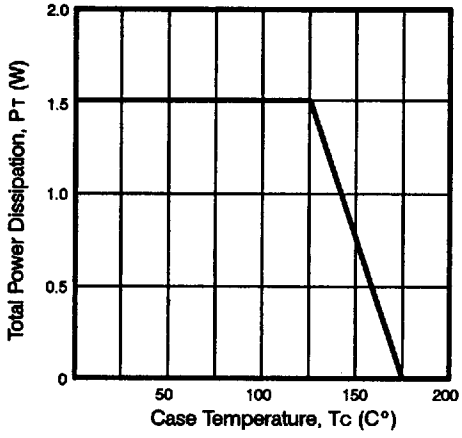
ISOLATION vs. FREQUENCY



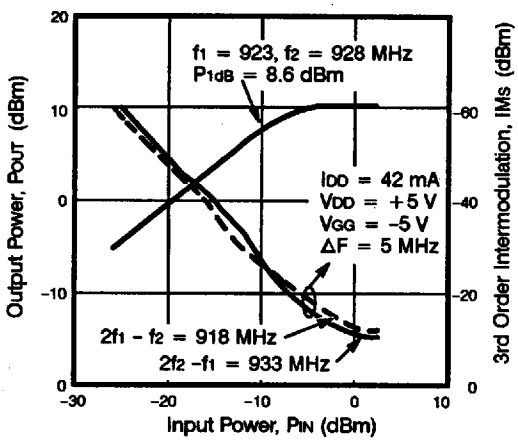
OUTPUT POWER vs. INPUT POWER



D.C. POWER DERATING CURVE



3RD ORDER INTERMODULATION vs. OUTPUT POWER and INPUT POWER



Note: For self-biasing information, please refer to Application Note AN1011, available from California Eastern Laboratories.