


UNISONIC TECHNOLOGIES CO., LTD
UF630
MOSFET

9A, 200V, 0.4Ω , N-CHANNEL POWER MOSFETS

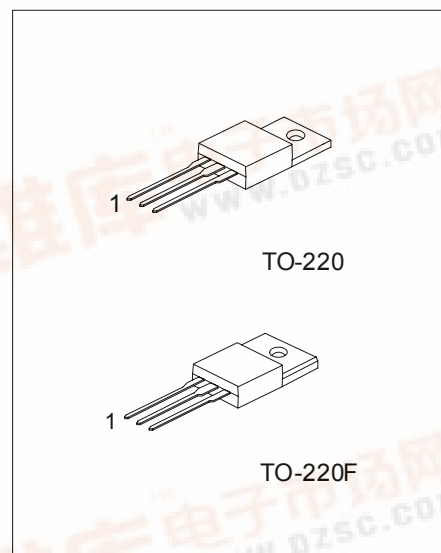
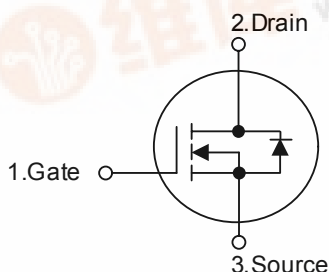
■ DESCRIPTION

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

■ FEATURES

- * 9A, 200V, Low $R_{DS(ON)}$ (0.4Ω)
- * Single Pulse Avalanche Energy Rated
- * Rugged - SOA is Power Dissipation Limited
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance

■ SYMBOL



*Pb-free plating product number: UF630L

■ ORDERING INFORMATION

Order Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
UF630-TA3-T	UF630L-TA3-T	TO-220	G	D	S	Tube
UF630-TF3-T	UF630L-TF3-T	TO-220F	G	D	S	Tube

UF630L-TA3-T 		(1) T: Tube (2) TA3: TO-220, TF3: TO-220F (3) L: Lead Free Plating Blank: Pb/Sn
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■ ABSOLUTE MAXIMUM RATINGS (T_c = 25°C, Unless Otherwise Specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage (T _J =25°C~125°C)		V _{DS}	200	V
Drain to Gate Voltage (R _{GS} = 20kΩ, T _J =25°C~125°C)		V _{DGR}	200	V
Gate to Source Voltage		V _{GS}	±20	V
Drain Current	Continuous	I _D	9	A
	Ta = 100°C		6	A
	Pulsed	I _{DM}	36	A
Maximum Power Dissipation (Ta = 25°C)		P _D	75	W
Derating above 25°C			0.6	W/°C
Single Pulse Avalanche Energy Rating (V _{DD} =20V, starting T _J =25°C, L=3.37mH, R _G =50Ω, peak I _{AS} = 9A)		E _{AS}	150	mJ
Operation and Storage Temperature		T _J , T _{STG}	-40 ~ +150	°C

Note: 1. Signified recommend operating range that indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits.

2. Absolute maximum ratings indicate limits beyond which damage to the device may occur.

■ ELECTRICAL SPECIFICATIONS (T_C=25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 16)	200			V
Gate to Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA	2		4	V
On-State Drain Current (Note 1)	I _{D(ON)}	V _{DS} > I _{D(ON)} × R _{DS(ON)MAX} , V _{GS} = 10V	9			A
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V			25	μA
		V _{DS} =0.8xRated BV _{DSS} , V _{GS} =0V, T _J = 125°C			250	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V			±100	nA
Drain to Source On Resistance (Note 1)	R _{DS(ON)}	I _D = 5A, V _{GS} = 10V (Figure 14, 15)		0.25	0.85	Ω
Forward Transconductance (Note 1)	g _{FS}	V _{DS} > I _{D(ON)} × R _{DS(ON)MAX} , I _D = 5A (Figure 18)	3	4.8		S
Turn-On Delay Time	t _{DLY(ON)}	V _{DD} = 90V, I _D ≈9A, R _{GS} = 9.1Ω, V _{GS} = 10V R _L = 9.6Ω (Note 2)			30	ns
Rise Time	t _R				50	ns
Turn-Off Delay Time	t _{DLY(OFF)}				50	ns
Fall Time	t _F				40	ns
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10V, I _D = 9A, V _{DS} = 0.8 x Rated BV _{DSS} I _{g(REF)} = 1.5mA (Figure 20) (Note 3)		19	30	nC
Gate to Source Charge	Q _{GS}			10		nC
Gate to Drain "Miller" Charge	Q _{GD}			9		nC
Input Capacitance	C _{ISS}			600		pF
Output Capacitance	C _{OSS}	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz (Figure 17)		250		pF
Reverse - Transfer Capacitance	C _{RSS}			80		pF

NOTE : 1. Pulse Test: Pulse width≤300μs, Duty Cycles≤2%.

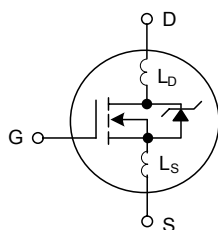
2. MOSFET Switching Times are Essentially Independent of Operating Temperature.

3. Gate Charge is Essentially Independent of Operating Temperature.

■ INTERNAL PACKAGE INDUCTANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Internal Drain Inductance	L_D		3.5		nH
Measured from the contact screw on tab to center of die			4.5		nH
Internal Source Inductance	L_S		7.5		nH
Measured from the source lead(6mm from header) to source bond pad					

Remark: Modified MOSFET symbol showing the internal devices inductances as below.



■ THERMAL DATA

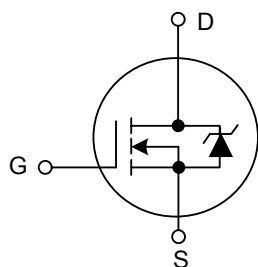
PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction-Ambient	θ_{JA}	80	°C/W
Thermal Resistance Junction-Case	θ_{JC}	1.67	

■ SOURCE TO DRAIN DIODE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source to Drain Diode Voltage (Note 1)	V_{SD}	$T_J = 25^\circ\text{C}$, $I_{SD} = 9.0\text{A}$, $V_{GS} = 0\text{V}$ (Figure 19)			2	V
Continuous Source to Drain Current	I_{SD}	Note 2			8	A
Pulse Source to Drain Current	I_{SDM}				36	A
Reverse Recovery Time	t_{RR}	$T_J = 150^\circ\text{C}$, $I_{SD} = 9.0\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		450		ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^\circ\text{C}$, $I_{SD} = 9.0\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		3		μC

NOTE : 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

2. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.



■ TEST CIRCUITS AND WAVEFORMS

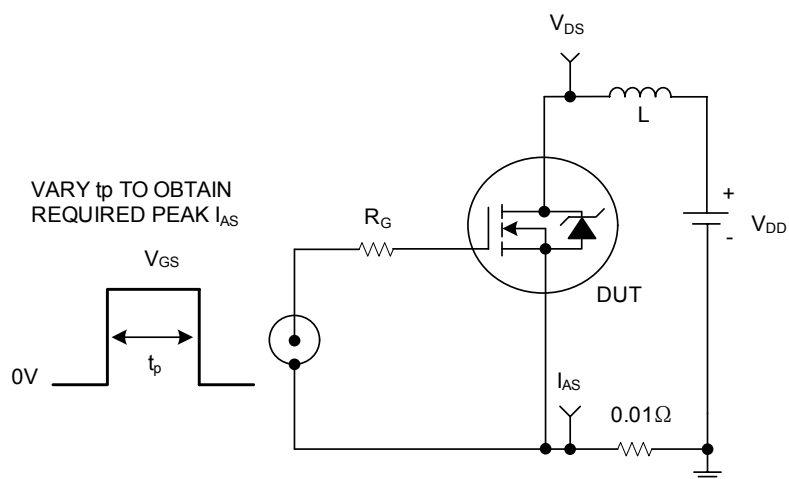


FIGURE 1. UNCLAMPED ENERGY TEST CIRCUIT

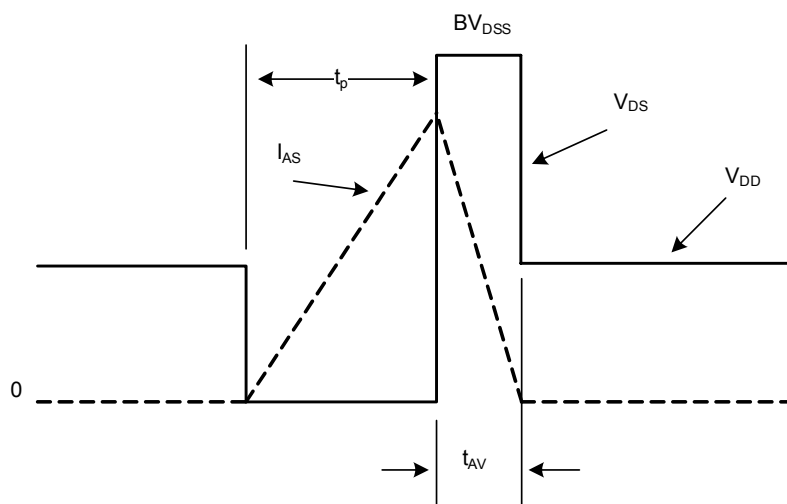


FIGURE 2. UNCLAMPED ENERGY WAVEFORMS

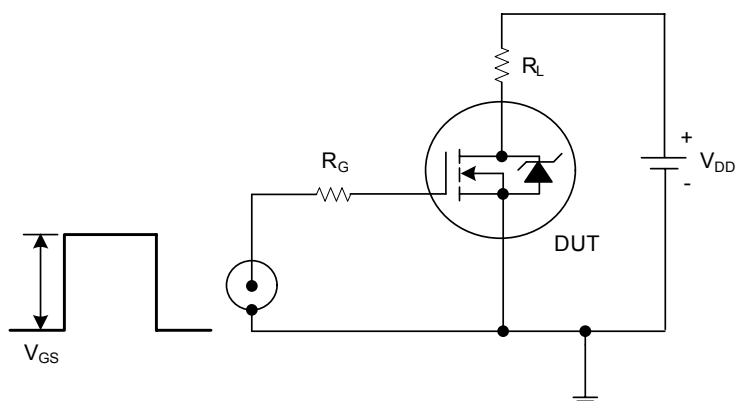


FIGURE 3. SWITCHING TIME TEST CIRCUIT

■ TEST CIRCUITS AND WAVEFORMS(cont.)

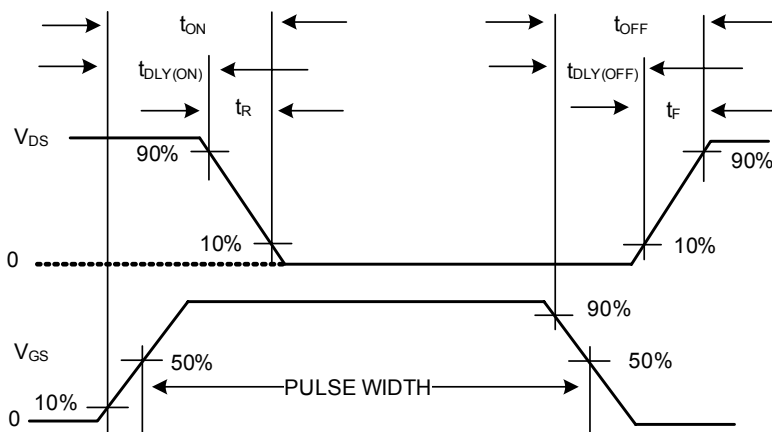


FIGURE 4. RESISTIVE SWITCHING WAVEFORMS

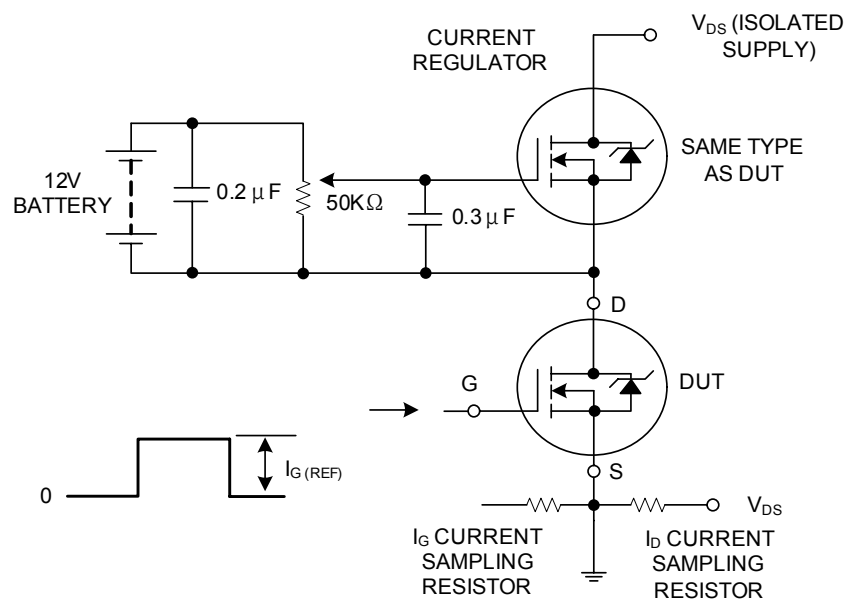


FIGURE 5. GATE CHARGE TEST CIRCUIT

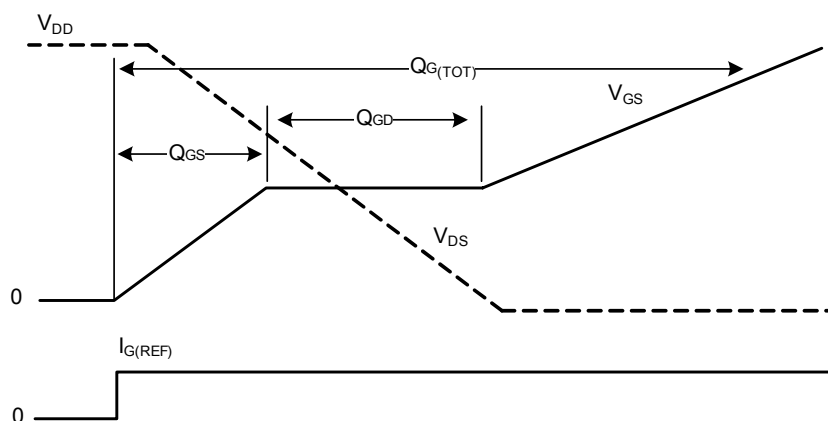


FIGURE 6. GATE CHARGE WAVEFORMS

■ TYPICAL CHARACTERISTICS

FIGURE 7. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

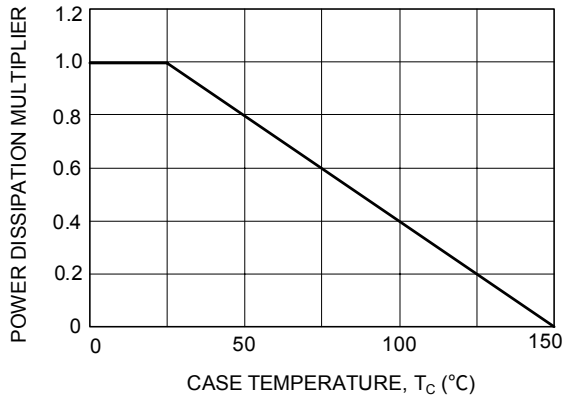


FIGURE 8. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

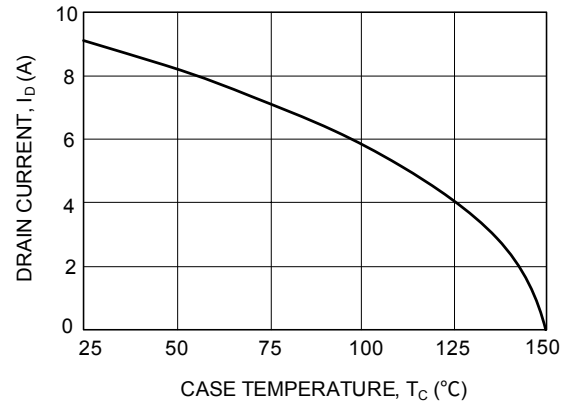


FIGURE 9. NORMALIZED TRANSIENT THERMAL IMPEDANCE

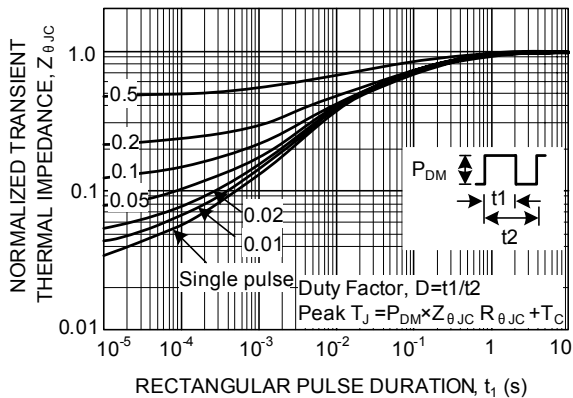


FIGURE 10. FORWARD BIAS SAFE OPERATING AREA

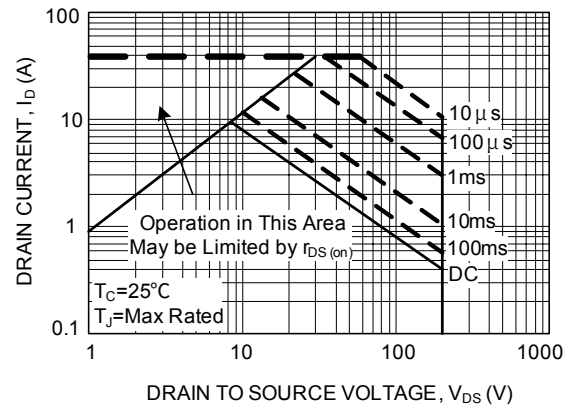


FIGURE 11. OUTPUT CHARACTERISTICS

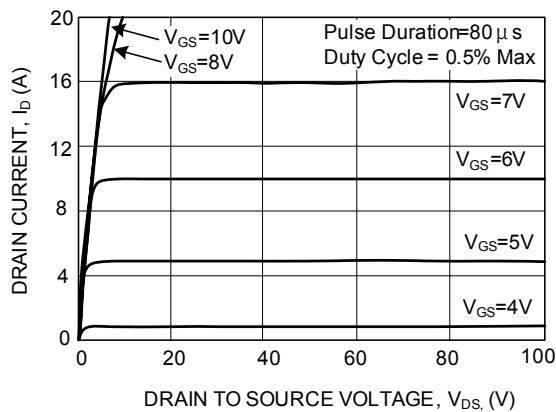
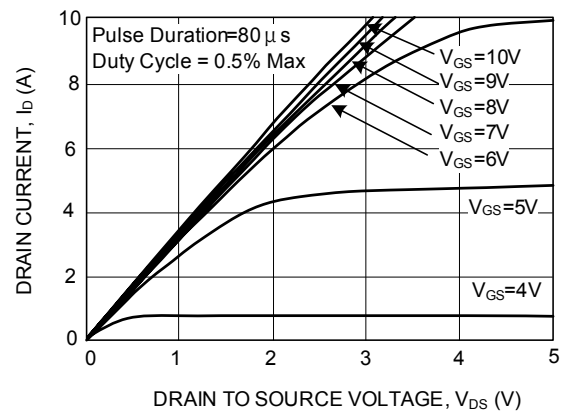


FIGURE 12. SATURATION CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (cont.)

FIGURE 13. TRANSFER CHARACTERISTICS

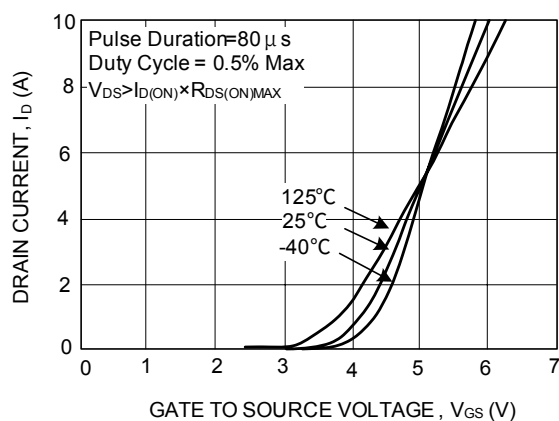


FIGURE 14. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

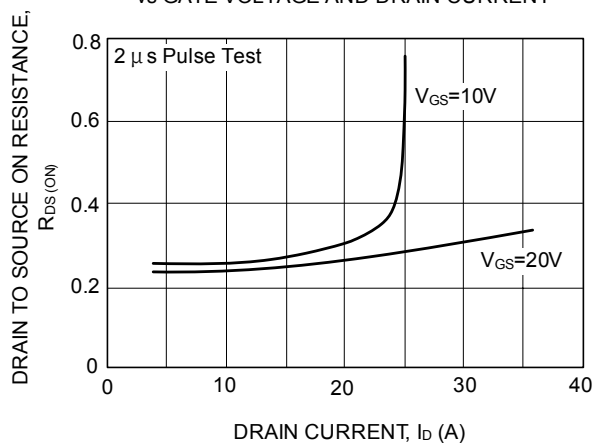


FIGURE 15. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

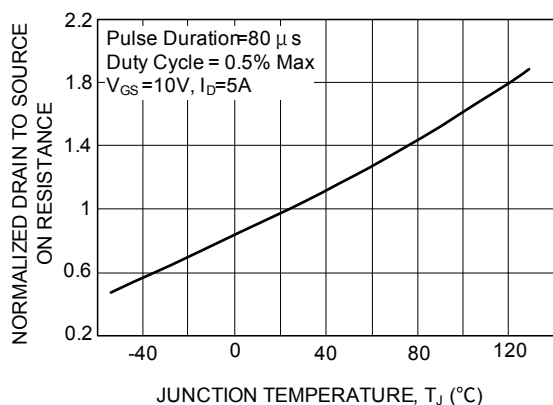


FIGURE 16. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

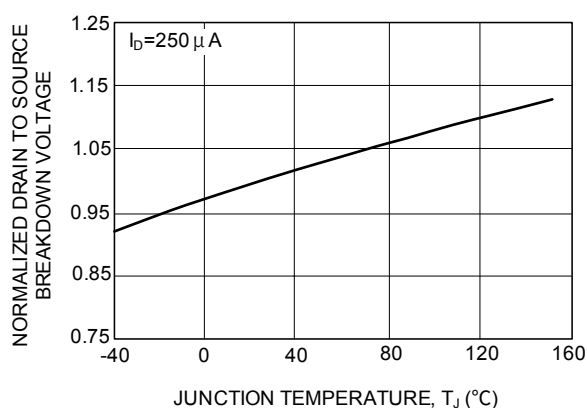


FIGURE 17. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

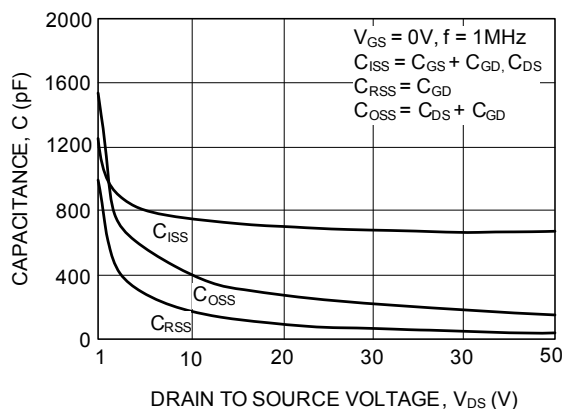
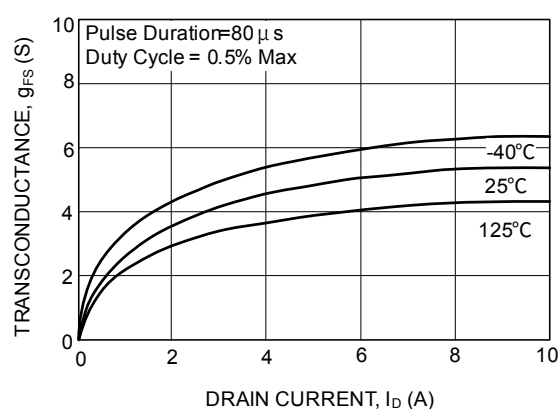


FIGURE 18. TRANSCONDUCTANCE vs DRAIN CURRENT



■ TYPICAL CHARACTERISTICS (cont.)

FIGURE 19. SOURCE TO DRAIN DIODE VOLTAGE

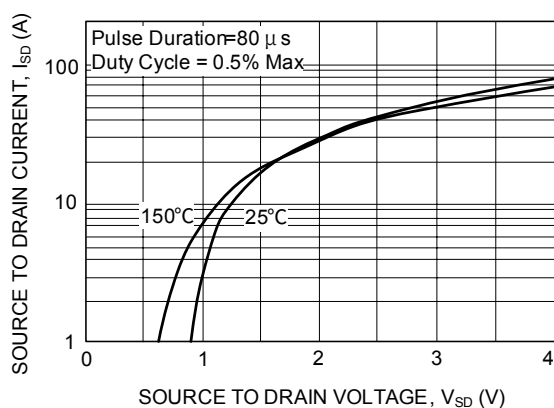
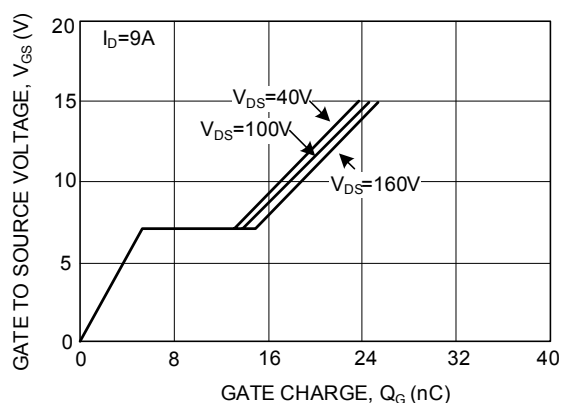


FIGURE 20. GATE TO SOURCE VOLTAGE vs GATE CHARGE



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