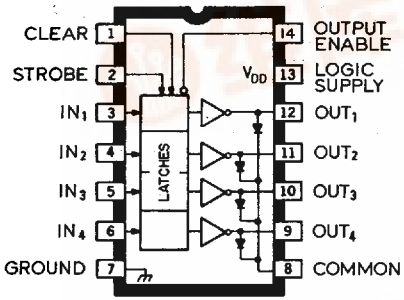
5800 AND 5801

T-52-13-90

BiMOS II LATCHED DRIVERS

UCN5800L

UCN5800A



Dwg. No. A-10,499D

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{CE} . . . . . 50 V
Supply Voltage, V_{DD} . . . . . 15 V
Input Voltage Range,
V_{IN} . . . . . -0.3 V to V_{DD} + 0.3 V
Continuous Collector Current,
I_C . . . . . 500 mA
Package Power Dissipation,
P_D . . . . . See Graph
Operating Temperature Range,
T_A . . . . . -20°C to +85°C
Storage Temperature Range,
T_S . . . . . -55°C to +150°C

Note that the UCN5800A (dual in-line package) and UCN5800L (small-outline IC package) are electrically identical and share a common pin number assignment.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

The UCN5800A/L and UCN5801A/EP latched-input BiMOS ICs merge high-current, high-voltage outputs with CMOS logic. The CMOS input section consists of 4 or 8 data ('D' type) latches with associated common CLEAR, STROBE, and OUTPUT ENABLE circuitry. The power outputs are bipolar npn Darlingtons. This merged technology provides versatile, flexible interface. These BiMOS power interface ICs greatly benefit the simplification of computer or microprocessor I/O. The UCN5800A and UCN5800L each contain four latched drivers; the UCN5801A and UCN5801EP contain eight latched drivers.

The UCN5800A/L and UCN5801A/EP supersede the original BiMOS latched-input driver ICS (UCN4400A and UCN4801A). These second-generation devices are capable of much higher data input rates and will typically operate at better than 5 MHz with a 5 V logic supply. Circuit operation at 12 V affords substantial improvement over the 5 MHz figure.

The CMOS inputs are compatible with standard CMOS and NMOS circuits. TTL circuits may mandate the addition of input pull-up resistors. The bipolar Darlington outputs are suitable for directly driving many peripheral/power loads: relays, lamps, solenoids, small dc motors, etc.

All devices have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will withstand at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

The UCN5800A is furnished in a standard 14-pin DIP; the UCN5800L in a surface-mountable SOIC; the UCN5801A in a 22-pin DIP with 0.400" (10.16 mm) row centers; the UCN5801EP in a 28-lead PLCC. All devices are also available for operation between -40°C and +85°C. To order, change the prefix from 'UCN' to 'UCQ'.

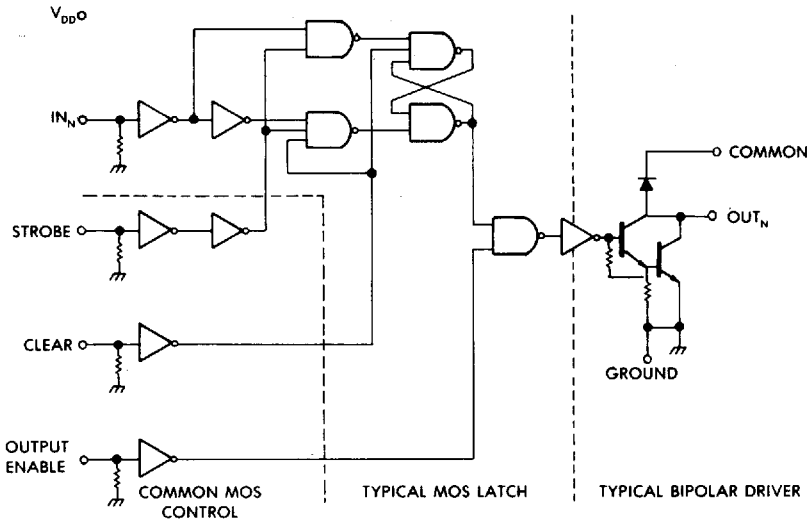
FEATURES

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

Always order by complete part number: **UCN5801EP** .

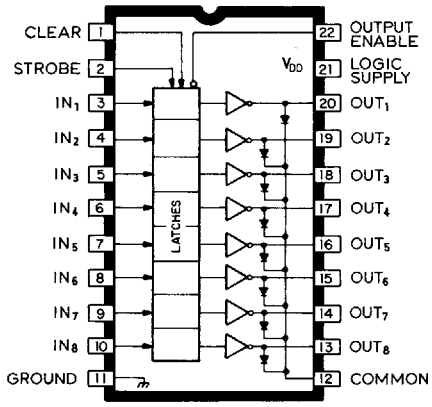
5800 AND 5801
BiMOS II LATCHED DRIVERS

FUNCTIONAL BLOCK DIAGRAM

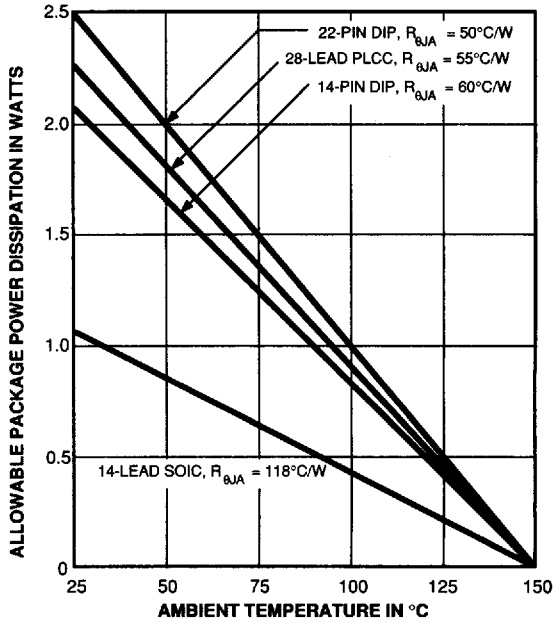


Dwg. No. A-10,495A

UCN5801A



Dwg. No. A-10,498D



Dwg. No. GP-023

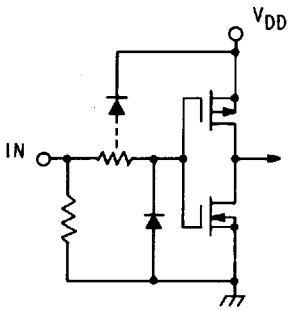
5800 AND 5801
BiMOS II LATCHED DRIVERS

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V, T_A = +25°C	—	—	50	µA
		V_{CE} = 50 V, T_A = +70°C	—	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	0.9	1.1	V
		I_C = 200 mA	—	1.1	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	—	V
		V_{DD} = 10 V	8.5	—	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	200	—	kΩ
		V_{DD} = 10 V	50	300	—	kΩ
		V_{DD} = 5.0 V	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	1.0	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	0.9	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	—	200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	50	100	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V, T_A = +25°C	—	—	50	µA
		V_R = 50 V, T_A = +70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.7	2.0	V

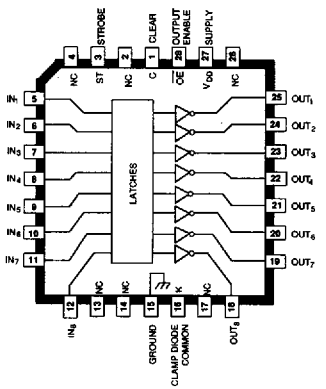
NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

TYPICAL INPUT CIRCUIT



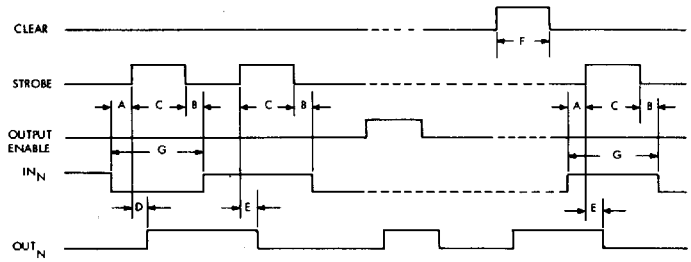
Dwg. No. A-12,520

UCN5801EP



Dwg. No. PP-037

5800 AND 5801
BiMOS II LATCHED DRIVERS



Dwg. No. A-10,895A

TIMING CONDITIONS
(Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) . . . . . **50 ns**
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) . . . . . **50 ns**
C. Minimum Strobe Pulse Width . . . . . **125 ns**
D. Typical Time Between Strobe Activation and Output On to Off Transition . . . . . **500 ns**
E. Minimum Time Between Strobe Activation and Output Off to On Transition . . . . . **500 ns**
F. Minimum Clear Pulse Width . . . . . **300 ns**
G. Minimum Data Pulse Width. . . . . **225 ns**

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

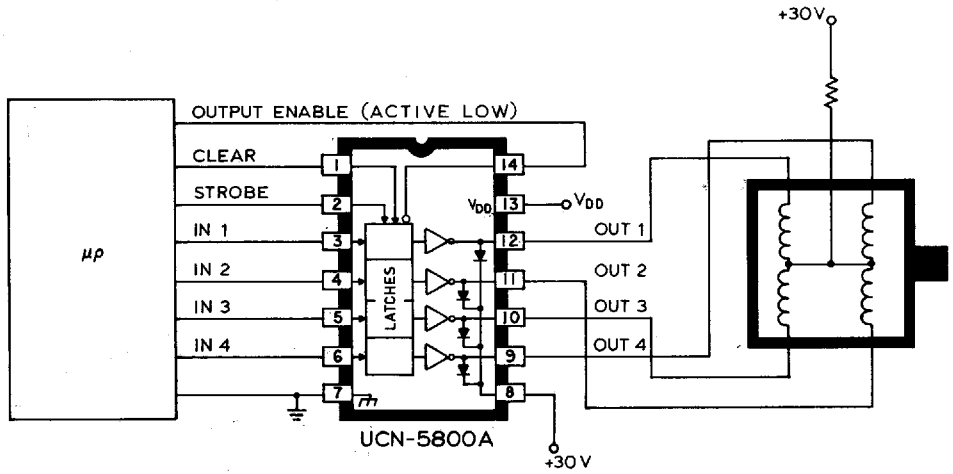
TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_{IN} t-1	OUT_{IN} t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant
t-1 = previous output state
t = present output state

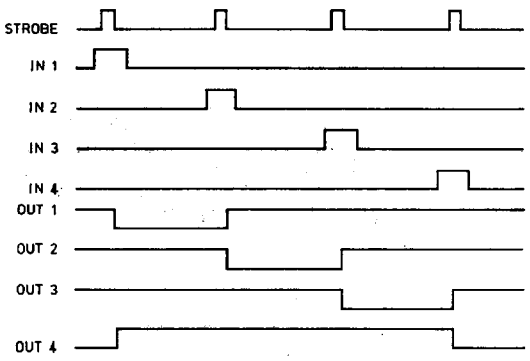
5800 AND 5801
BiMOS II LATCHED DRIVERS

TYPICAL APPLICATION
UNIPOLAR STEPPER-MOTOR DRIVE



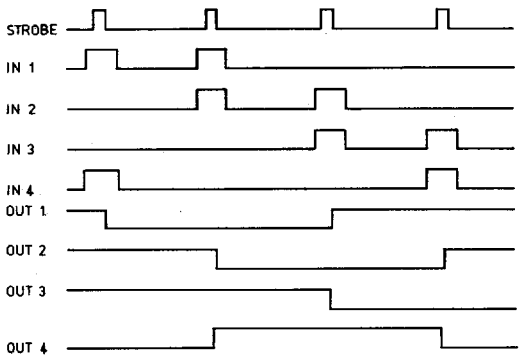
Dwg. No. B-1537

UNIPOLAR WAVE DRIVE



Dwg. No. A-11,446

UNIPOLAR 2-PHASE DRIVE



Dwg. No. A-11,447