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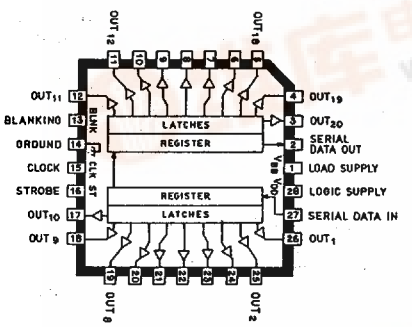
5812-F

T-52-13-09

BiMOS II 20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS

UCN5812EPF



Dwg. No. A-14,356

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} . . . . . 15 V
Driver Supply Voltage, V_{BB} . . . . . 60 V
(suffix '-1') . . . . . 80 V
Continuous Output Current Range,
I_{OUT} . . . . . -40 to +15 mA
Input Voltage Range,
V_{IN} . . . . . -0.3 V to V_{DD} +0.3 V
Package Power Dissipation, P_D
(UCN5812AF) . . . . . 3.12 W*
(UCN5812EPF) . . . . . 1.92 W†
Operating Temperature Range,
T_A . . . . . -20°C to +85°C
Storage Temperature Range,
T_S . . . . . -55°C to +150°C

* Derate at rate of 25 mW/°C above T_A = + 25°C
† Derate at rate of 15 mW/°C above T_A = + 25°C

Caution: Allegro CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Note that the UCN5812AF (dual in-line package) and UCN5812EPF (PLCC package) are electrically identical and share a common pin number assignment.

The UCN5812AF/EPF combine a 20-bit CMOS shift register, data latches, and control circuitry with high-voltage bipolar source drivers and active DMOS pull-downs for reduced supply current requirements. Although designed primarily for vacuum-fluorescent displays, the high-voltage, high-current outputs also allow them to be used in other peripheral power driver applications. They are improved versions of the original UCN5812A/EP.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. Data input rates are typically over 5 MHz with a 5 V logic supply, and over 7.5 MHz at 12 V. Especially useful for inter-digit blanking, the BLANKING input disables the output source drives and turns on the DMOS sink drivers. Use with TTL may require the use of appropriate pull-up resistors to ensure an input logic high.

A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Similar devices are available as the UCN5810AF/LWF (10 bits), UCN5811A (12 bits), and UCN5818AF/EPF (32 bits).

The output source drivers are high-voltage PNP-NPN Darlingtons with a minimum breakdown of 60 V and are capable of sourcing up to 40 mA. Selected devices (suffix '-1') feature 80 V minimum breakdowns. The DMOS active pull-downs are capable of sinking up to 15 mA.

The UCN5812AF is supplied in a 28-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. For surface-mounting, the UCN5812EPF is furnished in 28-lead plastic chip carrier (quad pack) with 0.050"(1.22 mm) centers. Copper lead-frames, reduced supply current requirements and lower output saturation voltages, allow continuous operation, with all outputs sourcing 25 mA, of the UCN5812AF over the operating temperature range, and the UCN5812EPF up to +75°C. All 60 V devices (without the '-1' suffix) are also available for operation between -40°C and +85°C. To order, change the prefix from 'UCN' to 'UCQ'.

FEATURES

- High-Speed Source Drivers
- 60 V or 80 V Source Outputs
- Active DMOS Pull-Downs
- Low-Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- 3.3 MHz Minimum Data Input Rate
- Reduced Supply Current Requirements
- Improved Replacement for TL5812

Always order by complete part number, e.g., **UCN5812AF-1** .

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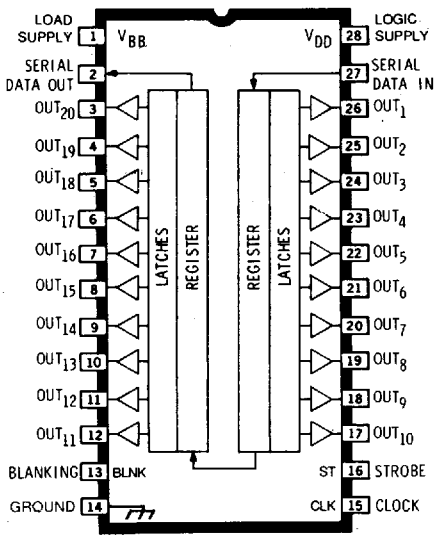
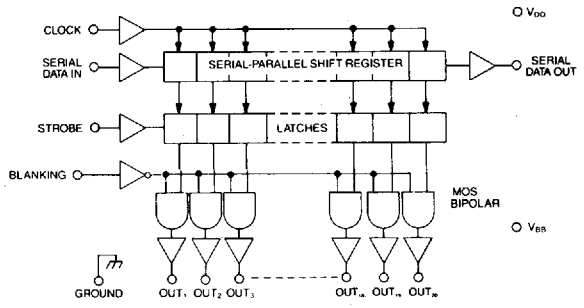
5812-F
20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS

UCN5812AF

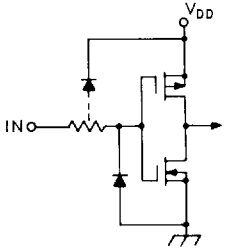


Dwg. No. A-12,270

FUNCTIONAL BLOCK DIAGRAM

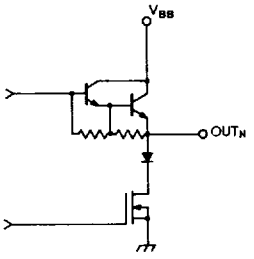


TYPICAL INPUT CIRCUIT



Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,219

5812-F
20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS

ELECTRICAL CHARACTERISTICS at T_A = + 25°C, V_{BB} = 60 V (UCN5812AF/EPF) or 80 V (suffix '-1') unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA, V_{BB} = 60 V	58	58.5	—	58	58.5	—	V
		I_{OUT} = -25 mA, V_{BB} = 80 V*	78	78.5	—	78	78.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	2.0	3.0	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	2.0	3.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.0	3.5	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-0.1	-1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	300	—	200	500	µA
	$I_{DD(0)}$	All Outputs Low	—	100	300	—	200	500	µA
	$I_{BB(1)}$	Outputs High, No Load	—	1.5	2.5	—	1.5	2.5	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF, 50% to 50%	—	2000	—	—	1000	—	ns
	t_{PLH}	C_L = 30 pF, 50% to 50%	—	1000	—	—	850	—	ns
Output Fall Time	t_f	C_L = 30 pF, 90% to 10%	—	1450	—	—	650	—	ns
Output Rise Time	t_r	C_L = 30 pF, 10% to 90%	—	650	—	—	700	—	ns

Negative current is defined as coming out ot (sourcing) the specified device pin.

* UCN5812AF-1 and UCN5812EPF-1 only.

5812-F
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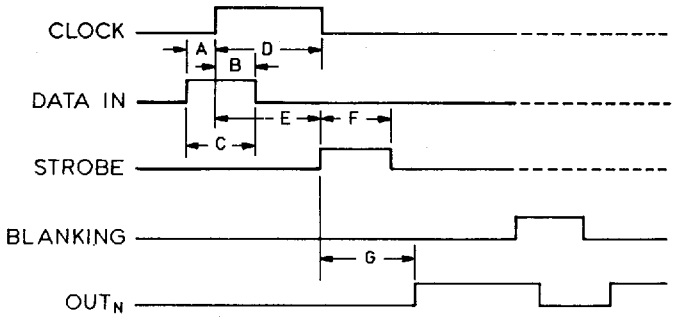

Dwg. No. 12,649A

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . **75 ns**
C. Minimum Data Pulse Width . . . . . **150 ns**
D. Minimum Clock Pulse Width . . . . . **150 ns**
E. Minimum Time Between Clock Activation and Strobe . . . . . **300 ns**
F. Minimum Strobe Pulse Width . . . . . **100 ns**
G. Typical Time Between Strobe Activation and Output Transistion . . . . . **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON, the information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	⌐¬	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⌐¬	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	¬⌐	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State