UCD9240 Digital Point of Load System Controller

FEATURES

- Controls up to 8 power stages and up to 4 voltage feedback control loops.
- Supports PMBus version 1.1.
- Flexible configuration, device can control:
  - Four single or dual power stages,
  - Two 4-phase power stages, or
  - One 2,4,6, or 8-phase power stage.
- Supports switching frequencies up to 2MHz.
- Supports conversion ratio of 12 to 1 at 2MHz with 250 psec duty-cycle resolution.
- +/-1mV feed-back resolution.
- Hardware accelerated digital 3-pole/3-zero compensator.
- Internal regulator drives an external pass element, giving a wide supply voltage range.
- 12-bit digital monitoring of power supply parameters, including:
  - Vin,
  - Vout, each rail,
  - Iout, each power stage (phase),
  - External Temperature, each stage.
- Multiple levels of current fault protection:
  - External current fault inputs,
  - Fast analog comparators monitor current sense voltage,
  - Digital current sense monitor of average current.
- Eight Synchronous Rectifier Enable (SRE) outputs.
- Able to synchronize PWM clocks between multiple UCD9240 devices.
- Enhanced non-volatile memory with ECC
- Programmable soft start and soft stop ramps under closed loop control.
- Supports multiple soft-start and soft-stop configuration including pre-bias start-up.
- Supports voltage tracking.
- Supports current sharing on multi-phase power stages.
- Supports phase shedding on multi-phase power stages based on average current.
- Programmable fan control outputs.
- Programmable margining and sequencing.
- Power+ Designer, a full featured PC based design tool to simulate, configure, and monitor power supply performance.

APPLICATIONS

- Industrial / ATE
- Networking Equipment
- Servers
- Storage Systems
- Telecommunications Equipment

DESCRIPTION

The UCD9240 is a digital synchronous buck PWM controller that can control up to 8 power stages in multi-phase configuration or up to 4 feedback outputs with two phases per output. This device provides enhanced configurability and control for point of load (POL) applications. The device is configured via PMBus with the Power+ Designer GUI.

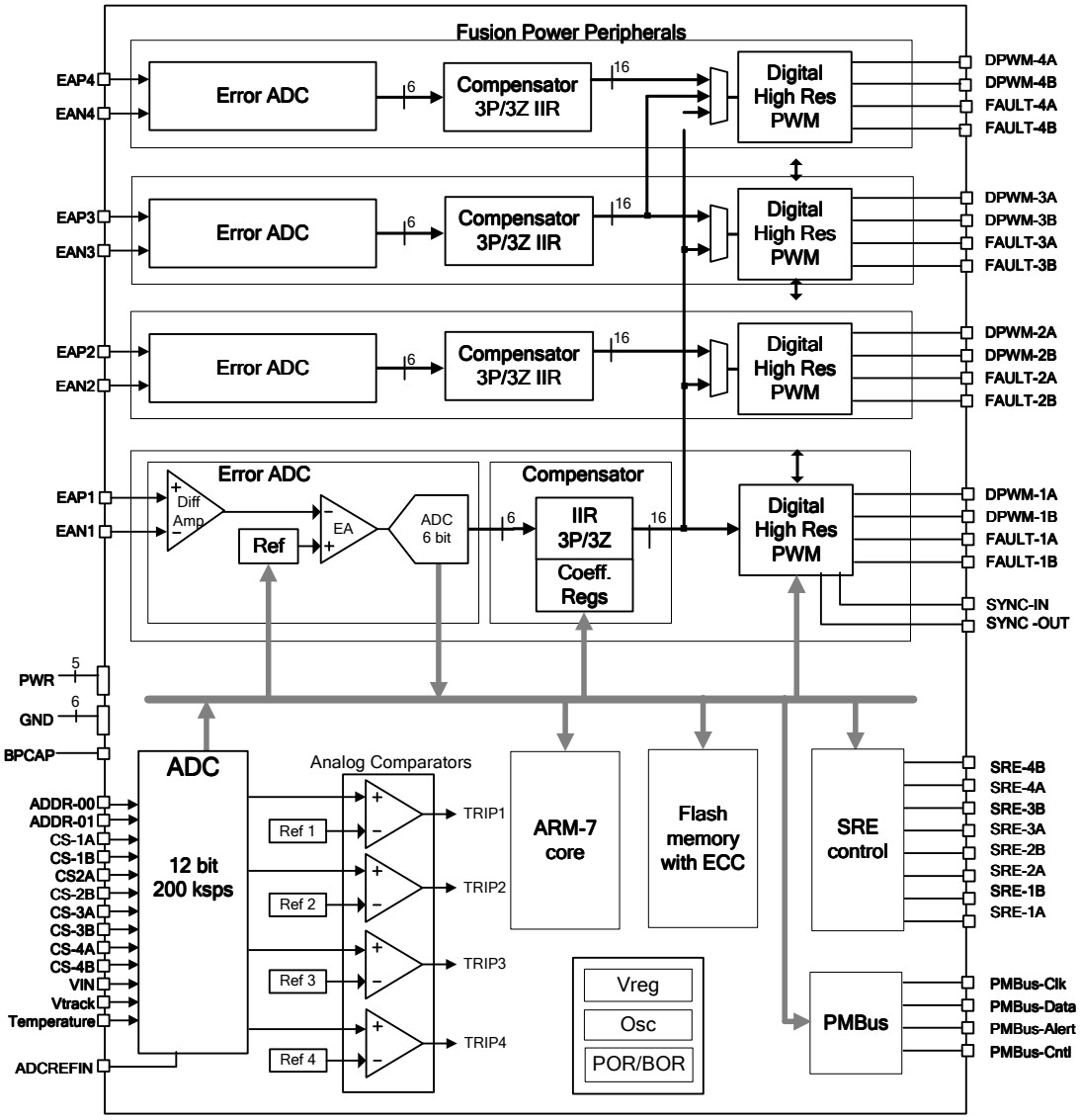
The switching frequency, output configuration and feedback compensation are programmed through the Power+ Designer. This allows the UCD9240 to support multiple converter arrangements and to meet dynamic converter performance for a broad range of POL applications.

Each high speed digital control loop has a dedicated 3-pole/3-zero compensator and 250ps PWMs. This architecture enables wide input to output voltage conversion ratio's at switching frequency of up to 2MHz.

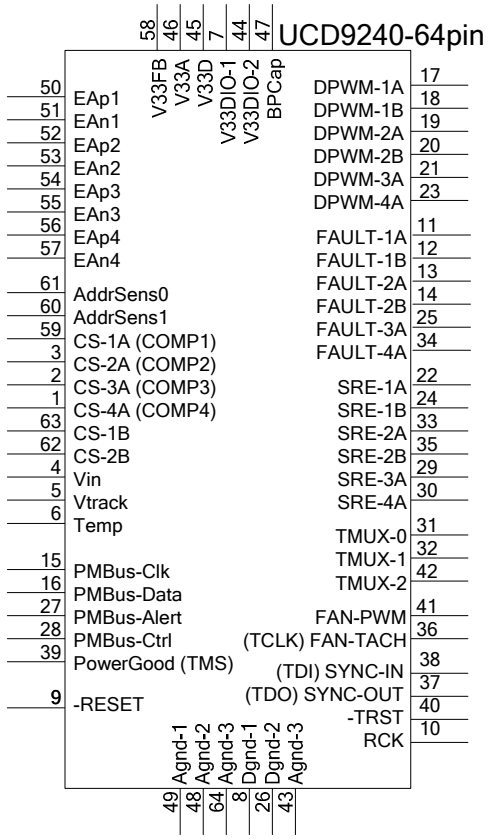
Additionally, the UCD9240 is able to monitor and manage power supply operating conditions and report the status to the host system through the PMBus. The management parameters are configurable through the Power+ Designer. The design tool allows the power supply designer to easily configure the control loop characteristics and generate the expected performance by displaying Bode plots for each controlled power stage.

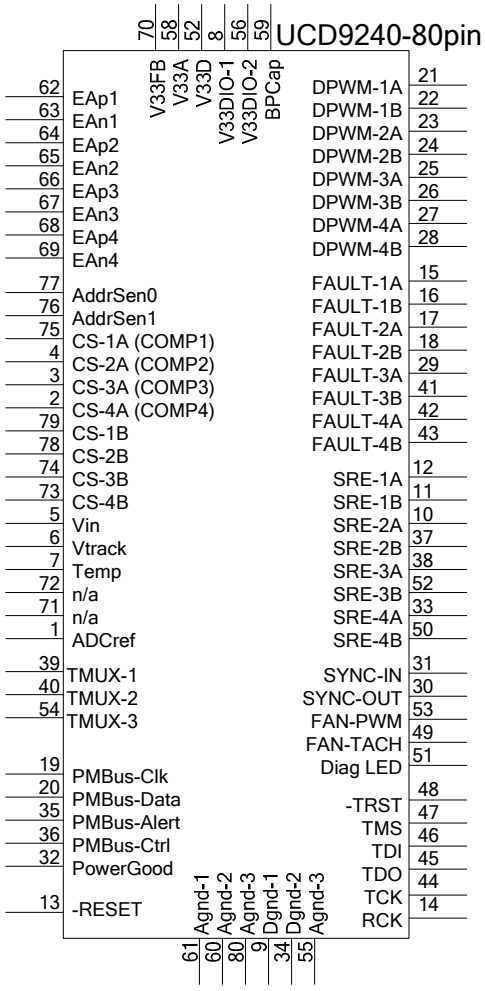
On multi-phase power stage outputs, the UCD9240 incorporates current balancing. The average current in each phase is monitored and the duty cycle for each phase adjusted to balance the average current. In addition, the UCD9240 supports "shedding" one or more phases (ganged power stages) commanded through PMBus or by average current demand. When a phase is dropped or added the UCD9240 automatically adjusts the phase of each PWM output to minimize output ripple as well as any needed change in loop compensation.

FUNCTIONAL BLOCK DIAGRAM



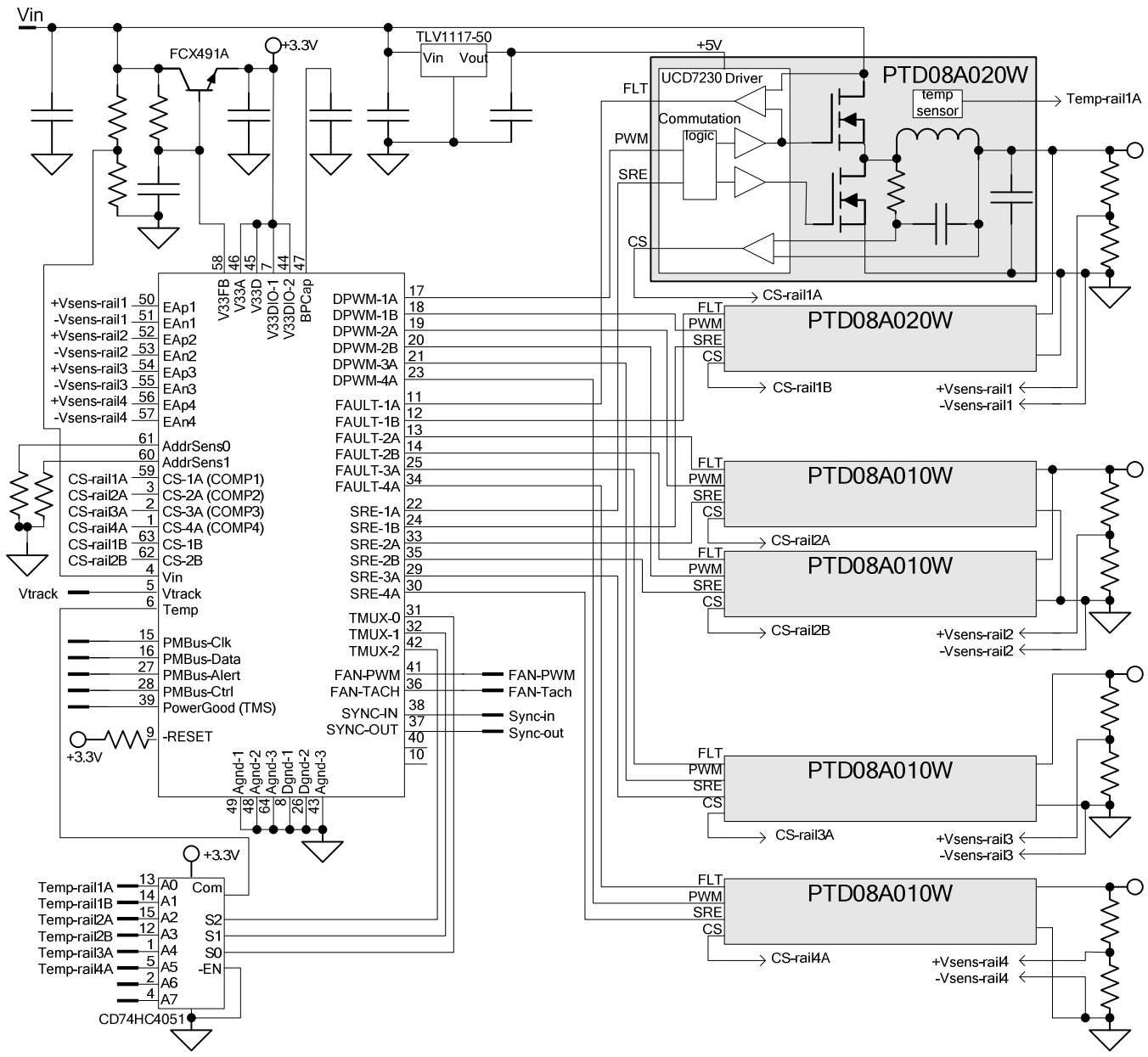
64-PIN AND 80-PIN I/O ASSIGNMENTS





The UCD9240 is available in a plastic 64-pin QFN package (RGC) and an 80-pin TQFP package (PFC).

TYPICAL APPLICATION SCHEMATIC



The diagram above shows the UCD9240 Power Supply Controller working in a system which requires the regulation of four independent power supplies. The loop for each power supply is created by the respective voltage outputs feeding into the Error ADC differential inputs, and completed by DPWM outputs feeding into the UCD7230 drivers which are on the PTD08A0x0 modules in the above diagram.

PIN DESCRIPTIONS

64-Pin Package Pin #	signal	80-Pin Package Pin #	signal	I/O	Description
50	EAp1	62	EAp1	I	Error Analog, differential voltage, Positive channel #1 input.
51	EAn1	63	EAn1	I	Error Analog, differential voltage, Negative channel #1 input.
52	EAp2	64	EAp2	I	Error Analog, differential voltage, Positive channel #2 input.
53	EAn2	65	EAn2	I	Error Analog, differential voltage, Negative channel #2 input.
54	EAp3	66	EAp3	I	Error Analog, differential voltage, Positive channel #3 input.
55	EAn3	67	EAn3	I	Error Analog, differential voltage, Negative channel #3 input.
56	EAp4	68	EAp4	I	Error Analog, differential voltage, Positive channel #4 input.
57	EAn4	69	EAn4	I	Error Analog, differential voltage, Negative channel #4 input.
61	AddrSens0	77	AddrSens0	I	PMBus address sense. Least significant address bits
60	AddrSens1	76	AddrSens1	I	PMBus address sense. Most significant address bits.
59	CS-1A	75	CS-1A	I	Power stage 1A current sense input, Analog comparator 1.
3	CS-2A	4	CS-2A	I	Power stage 2A current sense input, Analog comparator 2.
2	CS-3A	3	CS-3A	I	Power stage 3A current sense input, Analog comparator 3.
1	CS-4A	2	CS-4A	I	Power stage 4A current sense input, Analog comparator 4.
63	CS-1B	79	CS-1B	I	Power stage 1B current sense input.
62	CS-2B	78	CS-2B	I	Power stage 2B current sense input.
4	Vin	5	Vin	I	Vin sense input.
5	Vtrack	6	Vtrack	I	Voltage Tracking
6	Temp	7	Temp	I	Temperature sense input
		74	CS-3B	I	Power stage 3B current sense input.
		73	CS-4B	I	Power stage 4B current sense input.
		72		I	NA analog input
		71		I	NA analog input
		1	ADCref		ADC Decoupling Cap Ground reference.
17	dPWM-1A	21	dPWM-1A	O	DPWM 1A output.
18	dPWM-1B	22	dPWM-1B	O	DPWM 1B output.
19	dPWM-2A	23	dPWM-2A	O	DPWM 2A output.
20	dPWM-2B	24	dPWM-2B	O	DPWM 2B output.
21	dPWM-3A	25	dPWM-3A	O	DPWM 3A output.
		26	dPWM-3B	O	DPWM 3B output.
23	dPWM-4A	27	dPWM-4A	O	DPWM 4A output.
		28	dPWM-4B	O	DPWM 4B output.
11	FAULT-1A	15	FAULT-1A	I	External Fault input 1A
12	FAULT-1B	16	FAULT-1B	I	External Fault input 1B
13	FAULT-2A	17	FAULT-2A	I	External Fault input 2A
14	FAULT-2B	18	FAULT-2B	I	External Fault input 2B
25	FAULT-3A	29	FAULT-3A	I	External Fault input 3A
		41	FAULT-3B	I	External Fault input 3B
34	FAULT-4A	42	FAULT-4A	I	External Fault input 4A
		43	FAULT-4B	I	External Fault input 4B
22	SRE-1A	12	SRE-1A	O	Synchronous Rectifier Enable 1A
24	SRE-1B	11	SRE-1B	O	Synchronous Rectifier Enable 1B
33	SRE-2A	10	SRE-2A	O	Synchronous Rectifier Enable 2A
35	SRE-2B	37	SRE-2B	O	Synchronous Rectifier Enable 2B
29	SRE-3A	38	SRE-3A	O	Synchronous Rectifier Enable 3A
		52	SRE-3B	O	Synchronous Rectifier Enable 3B
30	SRE-4A	33	SRE-4A	O	Synchronous Rectifier Enable 4A
		50	SRE-4B	O	Synchronous Rectifier Enable 4B
		51	diag LED	O	Diagnostic LED
31	TMUX-0	39	TMUX-0	O	Temperature multiplexer select S0
32	TMUX-1	40	TMUX-1	O	Temperature multiplexer select S1
42	TMUX-2	54	TMUX-2	O	Temperature multiplexer select S2

41	FAN-PWM	53	FAN-PWM	O	Fan control PWM output.
		49	PowerGood	O	Power Good signal
		32	FAN-Tach	I	Fan tachometer input

		30	Sync_Out	O	Sync output from DPWM #?.
		31	Sync_In	I	Sync input to DPWM #?.
10	NC	14	NC	O	No connect
36	FAN-Tach	44	NC	I	DVss.
37	Sync_Out	45	NC	O	No connect
38	Sync_In	46	NC	I	DVss.
39	PowerGood	47	NC	I/O	No connect or DVss.
40	NC	48	NC	I/O	No connect or DVss

9	nRESET	13	nRESET	I	Low Active device reset input.
15	PMBus_Clk	19	PMBus_Clk	I/O	PMBus Clk (Must have pull-up to 3.3V)
16	PMBus_Data	20	PMBus_Data	I/O	PMBus Data (Must have pull-up to 3.3V)
27	PMBus_Alert	35	PMBus_Alert	O	PMBUS Alert
28	PMBus_Cntrl	36	PMBus_Cntrl	I	PMBUS Cntl

58	V33FB	70	V33FB	I	3.3V linear regulator Feedback connection.
46	V33A	58	V33A	I	Analog 3.3 V supply
45	V33D	57	V33D	I	Digital Core 3.3V supply
7	V33DIO	8	V33DIO	I	Digital I/O 3.3V supply.
44	V33DIO	56	V33DIO	I	Digital I/O 3.3V supply.
47	BPCap	59	BPCap	I	1.8V Bypass Capacitor Connection.

49	AVss	61	AVss	I	Analog Ground.
48	AVss	60	AVss	I	Analog Ground.
64	AVss	80	AVss	I	Analog Ground.
8	DVss	9	DVss	I	Digital Ground.
26	DVss	34	DVss	I	Digital Ground.
43	DVss	55	DVss	I	Digital Ground.

ELECTRICAL SPECIFIACTIONS

Recommended operating conditions

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
V33D,V33DIO,V33A	Supply voltage during operation	3.0	3.3	3.6	V
T_A	Operating free-air temperature range	-40		125	C

Absolute Maximum Ratings[1]

Voltage applied at V33D to DVss	-0.3 V to 3.6 V
Voltage applied at V33A to AVss	-0.3 V to 3.6 V
Voltage applied to any pin (see NOTE)	-0.3 V to V_{33D} + 0.3 V
Storage temperature, T_{STG}	-40C to 150C

Electrical Characteristics

Supply Current

SYMBOL	PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNIT
I_{33a}	Supply current	V33A = 3.3V			15	mA
I_{33dio}	Supply current	V33DIO = 3.3V				mA
I_{33d}	Supply current	V33D = 3.3V		40		mA
I_{33d}	Supply current	V33D = 3.3V storing configuration parameters in flash memory		TBD		mA

Regulator Inputs/Outputs

SYMBOL	PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNIT
Vreg BPCap	Bypass Capacitor Voltage			1.8		V
V33	3.3V Linear Regulator		3.25	3.3	3.35	V
V33FB	3.3V linear Reg Feedback			4.0	4.6	V
I33FB	Series pass base drive	Vin = 12V		10		mA
Beta	Series NPN pass device		40			

Bias Supply Generator

Two supply voltages, 3.3 and 1.8 V, are required. An internal series pass regulator generates 1.8 V from the 3.3 V supply. It requires a 0.1 to 1 uF bypass capacitor from BPCap to ground. The 3.3 V can either be supplied from an external source, or generated from Vin with regulation circuitry built into the UCD9240 that drives an external series pass NPN transistor. Transistor beta must be at least 40. The typical application circuit shows the base of

[1] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE: All voltages referenced to V_{SS}.

the external NPN connected to a pull up resistor and the VD33FB pin. The NPN emitter becomes the 3.3 V supply for the chip and should be bypassed to ground with 4 to 5 uF.

Analog Inputs/Outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EAPn, EANn	Vsense Differential Voltage Range		0.0	0.8	1.6	V
	Maximum Vsense excursion		-0.3		2.0	V
EAP-EAN	Small Signal Error voltage resolution	during start/stop ramp during run mode		4.0 1.0		mV mV
	Error Voltage Accuracy	"DAC commanded to be 1V"	.99	1	1.01	V
	Input impedance	ground reference	TBD			ohm
	Input capacitance	differential			TBD	pF
I_{BIAS}	Bias current PMBus Addr pins		9		11	uA
V_{ADDR}	PMBus Address programming bins	See Table 2	0.141		2.50	uA
V_{RANGE}: CSxx	voltage range for current sense input		0		2.5	V
V_{RANGE}: Vin, Vtrack, Vtemp	input voltage range		0		2.5	V
$V_{OVERCURRENT}$: CS1-A, CS2-A, CS3-A, CS4-A	Analog Overcurrent Threshold			2.0		V
C_I[2]	Current Sense Input capacitance			5	10	pF
ADCRefIn	External Reference (80-pin package)	(Not currently supported in the Firmware!)	1.8		V33A	V

Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{retention}$	Retention of configuration parameters	T_J = 25C	100			Years
$t_{(reset)}$	Pulse length needed at Reset		2			µS
Fault Detection Latency						
$t_{(FAULT)}$	time to disable PWM output	High level on FAULT pin			20	nS
t(CLF)	time to disable PWM output	Step change in CS voltage from 1.0V to 2.5V			20	nS
t(OC)	time to disable PWM output due to overcurrrent detection on average KKK	Step change in CS voltage from 50% of PMBus programmed over-current threshold to 150% of threshold			800	uS

[2] Not production tested. Limits verified by design.

Digital Inputs/Outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OH}= +6 mA[3], V_{33DIO} = 3.0 V			Dgnd + 0.25	V
V_{OH}	High-level output voltage	I_{OH} = -6 mA[4], V_{33DIO} = 3.0 V	V_{33dio} – 0.6			V
VIH	High-level input voltage	V33DIO = 3.0 V	2.1			V
VIL	Low-level input voltage	V33DIO = 3.5 V			1.0	V

PMBus/SMBus/I2C

The timing characteristics and timing diagram for the communications interface that supports I^2C, SMBus and PMBus is shown below.

Table 1 I^2C/SMBus/PMBus Timing Characteristics

T_A = -40°C to 85°C, 3.0V < V_{DD} < 3.6V; Typical values at T_A = 25°C and V_{CC} = 2.5V (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FSMB	SMBus/PMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
FI2C	I^2C operating frequency	Slave mode, SCL 50% duty cycle	10		400	kHz
FMAS	SMBus master clock frequency	Master mode, No clock low slave extend		51.2		kHz
$t_{(BUF)}$	Bus free time between start and stop		4.7			us
$t_{(HD:STA)}$	Hold time after (repeated) start		4.0			us
$t_{(SU:STA)}$	Repeated start setup time		4.7			us
$t_{(SU:STO)}$	Stop setup time		4.0			us
$t_{(HD:DAT)}$	Data hold time	Receive Mode	0			ns
		Transmit Mode	300			ns
$t_{(SU:DAT)}$	Data setup time		250			ns
$t_{(TIMEOUT)}$	Error signal/detect	See (5) below	25		35	us
$t_{(LOW)}$	Clock low period		4.7			us
$t_{(HIGH)}$	Clock high period	See (6) below	4.0		50	us
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time	See (7) below			25	us
$t_{(LOW:MEXT)}$	Cumulative clock low master extend time	See (8) below			10	us
t_f	Clock/data fall time	See (9) below			300	ns
t_r	Clock/data rise time	See (10) below			1000	ns

[3] The maximum total current, IOHmax and IOLmax, for all outputs combined, should not exceed +/-12 mA to hold the maximum voltage drop specified.

4 The maximum total current, IOHmax and IOLmax, for all outputs combined, should not exceed +/-48 mA to hold the maximum voltage drop specified.

[5] The UCD9110 times out when any clock low exceeds $t_{(TIMEOUT)}$.

[6] $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction involving UCD9110 that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0]=0).

[7] $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.

[8] $t_{(LOW:MEXT)}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.

[9] Rise time t_r = VILMAX – 0.15) to (VIHMIN + 0.15)

[10] Fall time t_f = 0.9V_{DD} to (VILMAX – 0.15)

The coefficients of the filter sections are generated thru modeling the power stage and load in the Power+ Designer. Several banks of filter coefficients can be downloaded to the device which can automatically switch them based on on the operation of the power stage.

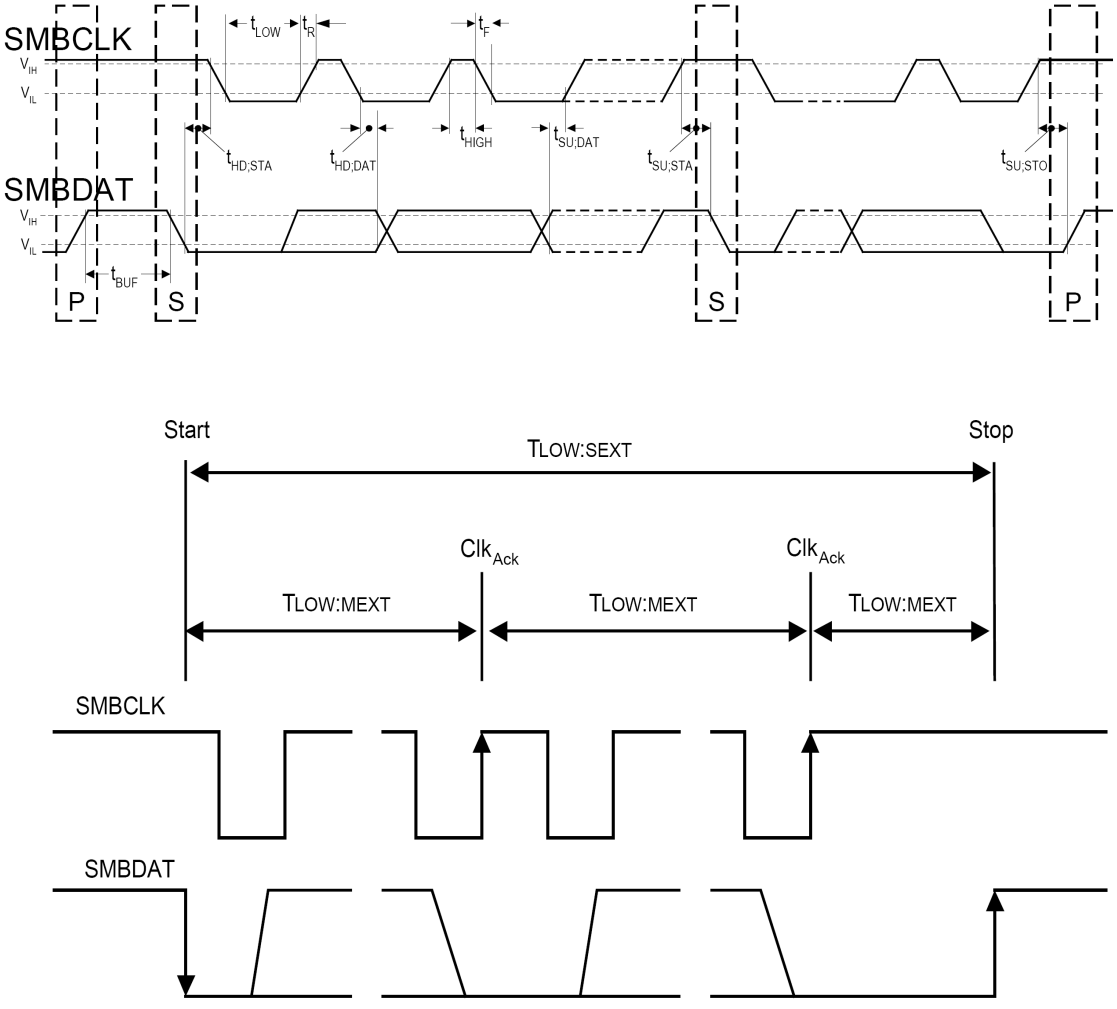


Figure 1 I²C/SMBus/PMBus Timing Diagram

FUNCTION OVERVIEW

The UCD9240 contains four Fusion Power Peripherals (FPP). Each FPP can be configured to drive from one to eight power stages. Each FPP consists of differential feedback input, circuits used to set the output regulation voltage, error measurement circuits, digital hardware accelerated for a 3-pole/3-zero compensator and a digital PWM engine. Each controller is configured through a PMBus serial interface.

PMBus Interface

The PMBus is a serial interface specifically designed to support power management. It is based on the SMBus interface, which is built on I^2C physical specification. The UCD9240 supports the interface through dedicated hardware and firmware in the ARM-7 digital supervisory processor.

The UCD9240 supports revision 1.1 of the PMBus standard. Wherever possible, standard PMBus commands are used to support the function of the device. For unique features of the UCD9240, MFR_SPECIFIC commands are defined to configure or activate those features.

The firmware for the UCD9240 is PMBus compliant, in accordance with the "Compliance" section of the PMBus specification. The firmware is also compliant with the SMBus 1.1 specification, including support for the SMBus ALERT function. The hardware can support either 100 kHz or 400 kHz signaling, though at present the firmware defaults to 100 kHz.

PMBus Address Decode via ADC12 Reading

Two pins are allocated to decode the PMBus address. At power-up the device applies I_{BIAS} to each address detect pin and the voltage on that pin is captured by the internal 12-bit ADC. The PMBus address is calculated as follows.

$$\text{PMBus Address} = 12*\text{bin}(V_{AD01}) + \text{bin}(V_{AD00})$$

Where $\text{bin}(V_{AD0x})$ is the address bin for one of 12 address as shown in

Table 2

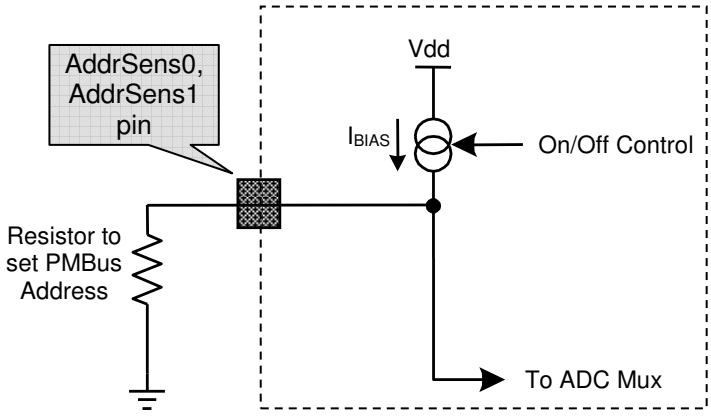


Figure 2 PMBus Address Detection Method

Table 2 PMBus Address bins

Address	Voltage	Resistor
12	2.299	209
11	1.815	165
10	1.463	133
9	1.177	107
8	0.953	86.6
7	0.749	68.1
6	0.604	54.9
5	0.486	44.2
4	0.383	34.8
3	0.308	28.0
2	0.249	22.6
1	0.196	17.8
0	0.157	14.3

A low impedance (short) on the address pin the produces a voltage below the minimum voltage will cause the PMBus address to default to address 0x0B. A high impedance (open) on the address pin that produces a voltage above the maximum voltage will also cause the PMBus address to default to address 0x0B.

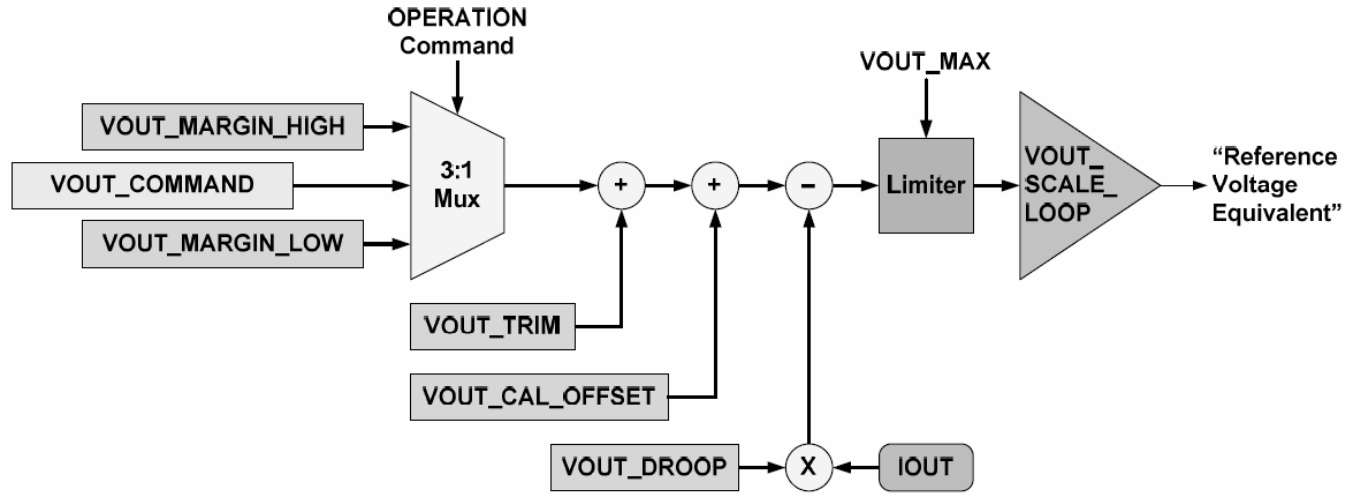


Figure 3 PMBus Voltage Adjustment Methods

Output Voltage Adjustment

The Output Voltage is programmed by issuing VOUT_COMMAND, VOUT_TRIM or VOUT_MARGIN, … commands on the PMBus..

Soft-Start, Soft-Stop and Normal Operation

During the soft-start or soft-stop the internal gain is changed to have +-8mV resolution This allows the ADC to have a wider dynamic range during the start/stop ramp. During normal operation the gain is adjusted to +-1mv resolution for tighter regulation.

Digital Compensator

Each voltage rail controller in the UCD9240 includes a digital compensator. The compensator is a digital filter consisting of a second order infinite impulse response (IIR) filter section cascaded with a first order IIR filter section. based design tool program:

The development tool for the UCD9240 comes with the "POWER+DESIGNER", which can be used to assist in defining the compensator coefficients. The design tool allows the compensator to be described in terms of the pole frequencies, zero frequencies and gain desired for the control loop. In addition, the Design Tool can be used to characterize the power stage so that the compensator coefficients can be chosen based on the total loop gain for each feedback system. The coefficients of the filter sections are generated thru modeling the power stage and load in the Power+ Designer.

Additionally, the UCD9240 allows for several banks of filter coefficients which can be configured to switch automatically based on the operation of the power stage.

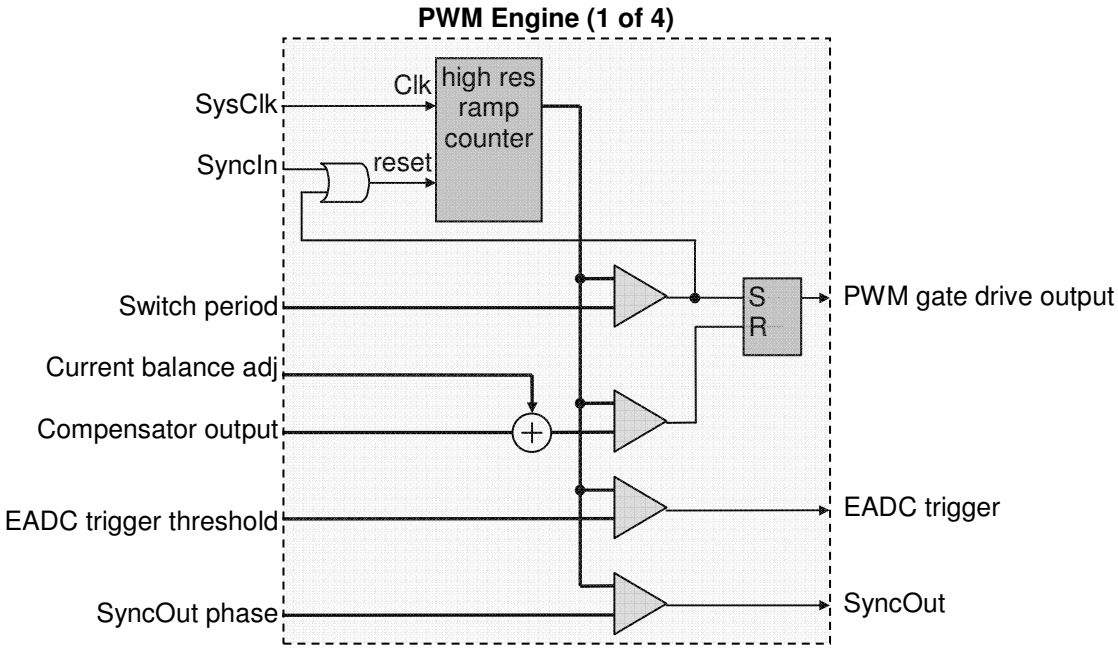
The compensator also allows the minimum and maximum duty cycle to be programmed. This again is done by issuing a PMBus command to the device.

PWM Engine

The output of the compensator feeds the high resolution PWM engine. The PWM engine produces the pulse width modulated gate drive output from the device. In operation, the compensator calculates the necessary duty cycle as a 16-bit number representing a value from 0.0 to 1.0. This duty cycle value is multiplied by the period to generate the duty period. The resolution of the duty period is 250 psec.

When the UCD9240 is configured to drive multiple power stage circuits from one compensator, each gate drive output pulse width is adjusted to correct for current imbalance between the connected power stage sections. This is done by monitoring the current using input on the current sense pins and increasing the pulse width of the PWM signal driving the power stage with the lowest current and decreasing the pulse width of the PWM signal driving the power stage with the highest measured current.

Each PWM engine can be synchronized to another PMW engine or to an external sync signal via the SYNC_IN and SYNC_OUT pins. An input sync signal causes a PWM ramp timer to reset. Sync signal outputs from each of the four PWM engines occur when the ramp timer crosses a programmed threshold. In this way the phase of multiple power stage drive signals can be tightly controlled. The synchronization behavior is programmed through a MFR_SPECIFIC PMBus command.



The switching frequency is set by issuing the FREQUENCY_SWITCH PMBus command.

Fault Handling

The UCD9240 has several fault handling features. The following faults are handled.

1. Vin is monitored for over-voltage or under-voltage.
2. A logic high signal from an external source, such as the gate driver IC will cause a fault and immediately shut down the PWM engine. The response to the event is programmed through a PMBus command.
3. The device contains programmable internal analog comparators that monitor the current sense inputs. If the current sense input exceeds the programmed threshold the PWM signal is shut down.
4. Monitoring and averaging the current sense inputs for each multiphase power stage that makes up an output rail. Over current and under current (negative) thresholds are programmed via PMBus for each rail. The response to the event is also programmed through a PMBus command.
5. Temperature is periodically measured and compared to the PMBus configured over-temperature threshold.

Temperature Measurement

The UCD9240 has the ability to measure current and temperature in the controlled power stage. The pin *Temp* and the select pins *TMUX0-2* are used to control an external analog multiplexer which cycles through each of the power stage temperature measurement signals. It can be programmed to accept the output from either a linear device such as an LM20 temperature sensor or a diode forward voltage.

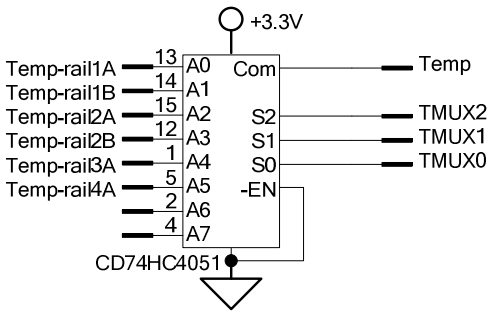


Figure 4 Temperature Mux (4-rail, 6-phase example)

Current Measurement

Pins CS1-A, CS1-B, CS2-A, CS2-B, CS3-A, CS3-B, CS4-A, and CS4-B are used to measure output or inductor current in each of the controlled power stages. MFR_SPECIFIC PMBus commands are used to calibrate each measurement. When the measured current exceeds either the over-current or undercurrent threshold a FAULT is declared the UCD9240 performs the PMBus programmed fault recovery. ADC current measurements are digitally filtered (averaged) before compared against the FAULT threshold.

In response to a PMBus request for a current reading, the device will return an average current value. When the UCD9240 is configured to drive a multi-phase power converter, the device will add the average current measurement for each of the power stages tied to a power rail.

Current Sense Detection

Several mechanisms are provide to sense output current. This allows for the design of power systems with multiple layers of protection.

1. A logic high signal on the FAULT input will immediately drive the PWM signal for the associated page (rail/output) low. The SRE signal will be driven low between TDB and TBD usec later. An intelligent gate driver such as the UCD7230 can be used to generate the FAULT signal. The UCD7230 monitors the voltage drop across the high side FET and if it exceeds a resistor programmed threshold, the UCD7230 activates the CLF output and turns off the FET drives. The CLF can be used to drive the FAULT input on the UCD9240.

   Typically, the FAULT input is used to monitor and protect against a short circuit in one of the switches or the load. Therefore this threshold is set to the highest current setting of the multiple over-current settings.

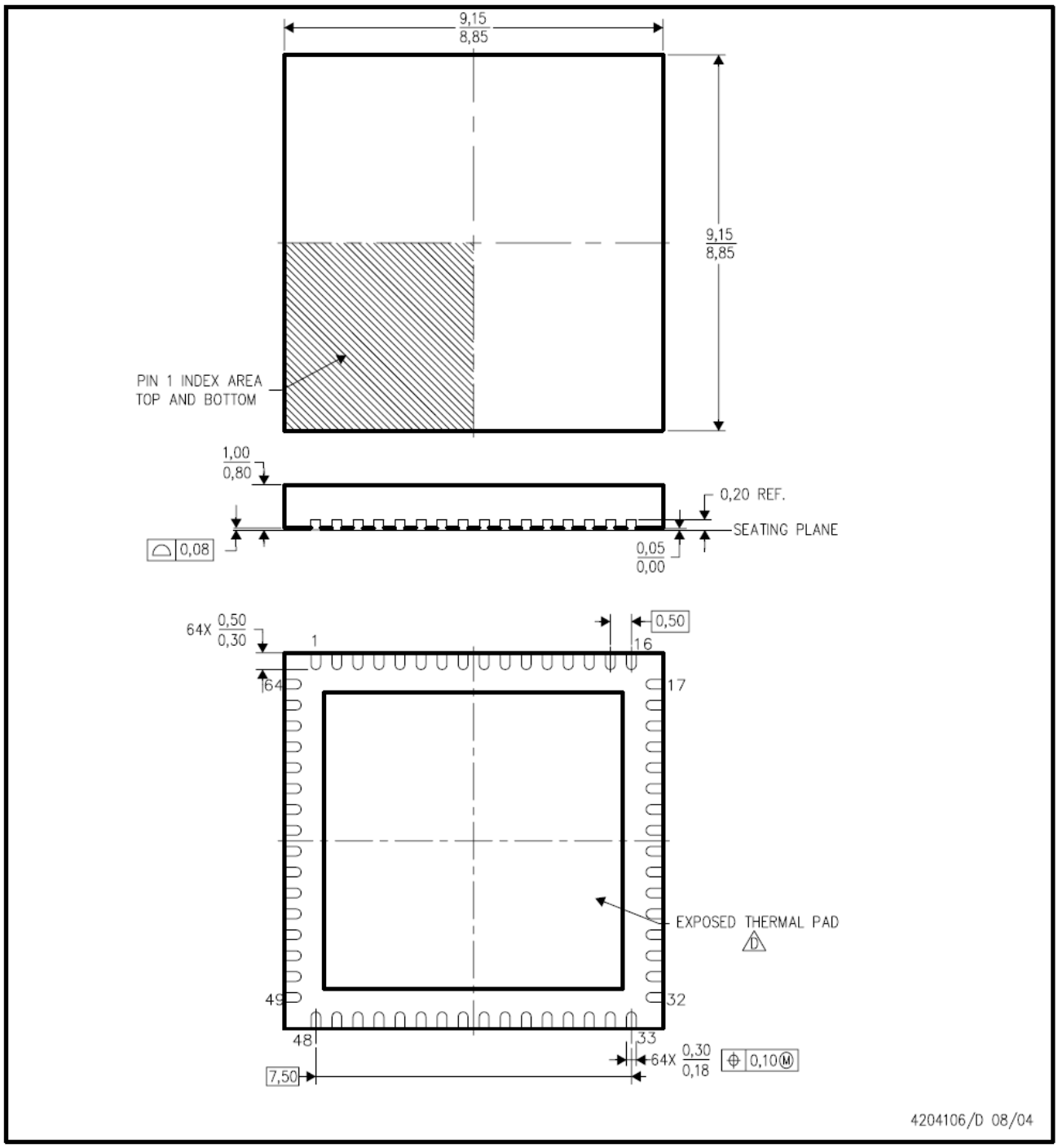
2. Four of the current sense inputs are wired to an internal analog comparator, one for each page (rail/output). The threshold for the current sense input is set to 2.0V. This input can be used to detect the output of a current sense amplifier such as the amplifier in the UCD7230 which monitors the current in the power stage inductor. If the current sense voltage exceeds 2.0V the corresponding PWM output is immediately driven low. The SRE signal will be driven low between TDB and TBD usec later. The over-current threshold condition is programmed by choosing the appropriate divider network on the input to the CSx.y pin. This forms the "middle" level of over-current protection.

3. Each Current Sense input to the UCD9240 is also monitored by the 12-bit ADC. This measured value is averaged and compared with a PMBus programmable threshold. This threshold is typically the lowest over-current setting and set closest to the maximum allowed current for the design.

PACKAGING

64-pin Package

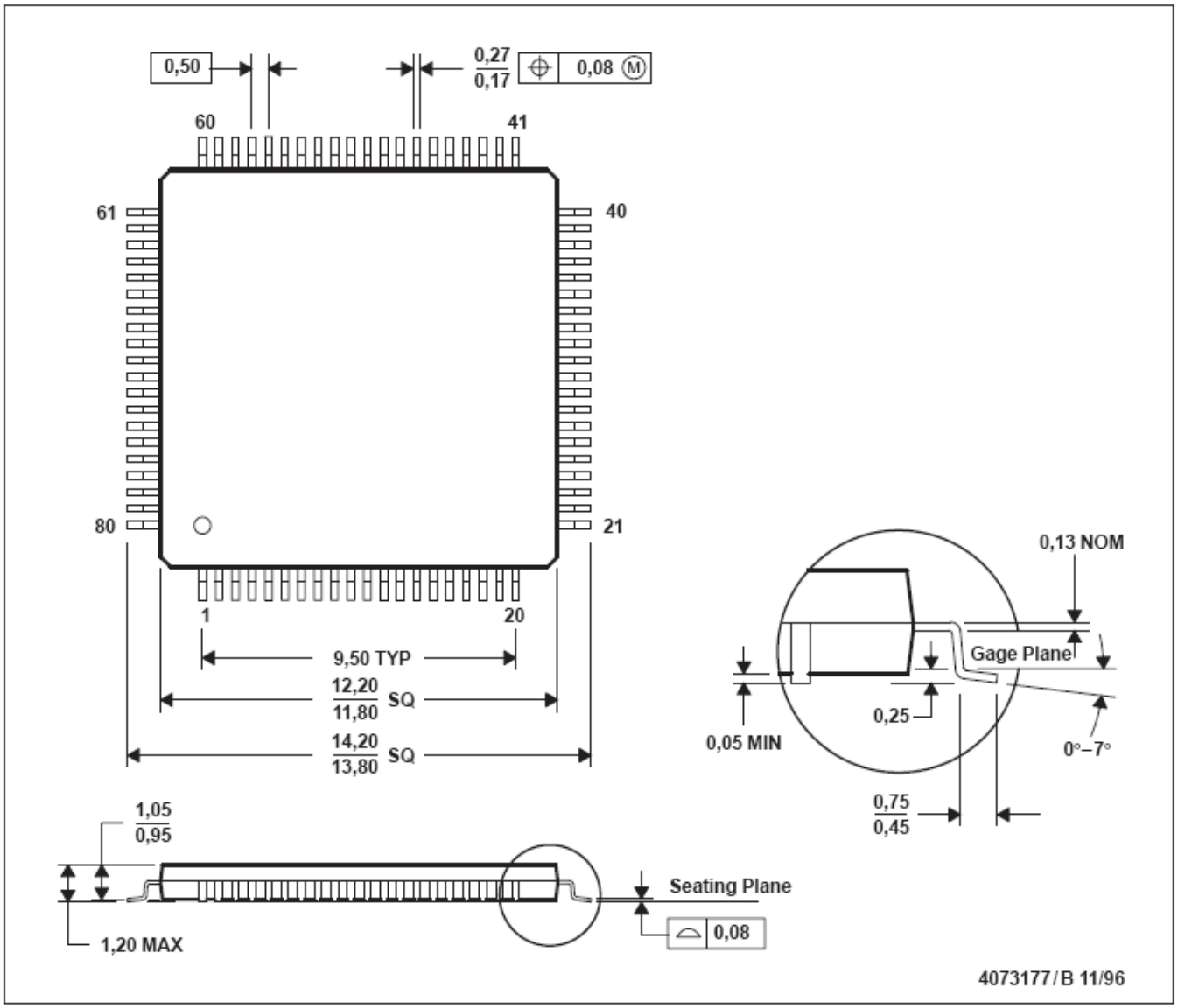
RGC (S–PQFP–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK



Notes: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, no-leads (QFN) package configuration.

80-pin Package

PFC (S-PQFP-G80) PLASTIC QUAD FLATPACK



Notes: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Ordering Information

Part Number	Package	Operating Temp. Range, T_A
UCD9240PHR	80-pin QFP	TBD
UCD9240RHBR	64-pin QFN	

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UCD9240RGCR	PREVIEW	QFN	RGC	64	2000	TBD	Call TI	Call TI
UCD9240RGCT	PREVIEW	QFN	RGC	64	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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