Digital Control Compatible Synchronous Buck ±4-A Drivers with Current Sense Conditioning Amplifier

FEATURES

- Input from Digital Controller Sets Operating Frequency and Duty Cycle
- Up to 2-MHz Switching Frequency
- Dual Current Limit Protection with Independently Adjustable Thresholds
- Fast Current Sense Circuit with 25-ns Propagation Delay and Adjustable Blanking Interval Prevents Catastrophic Current Levels
- Digital Output Current Limit Flag
- Low Offset, Gain of 25, Differential Current Sense Amplifier
- 3.3-V, 10-mA Internal Regulator
- Dual ±4-A TrueDrive™ High-Current Drivers
- 10-ns Typical Rise/Fall Times with 2.2-nF Loads
- 25-ns Input-to-Output Propagation Delay
- 25-ns Current Sense-to-Output Propagation Delay
- 4.5-V to 15.5-V Supply Voltage Range

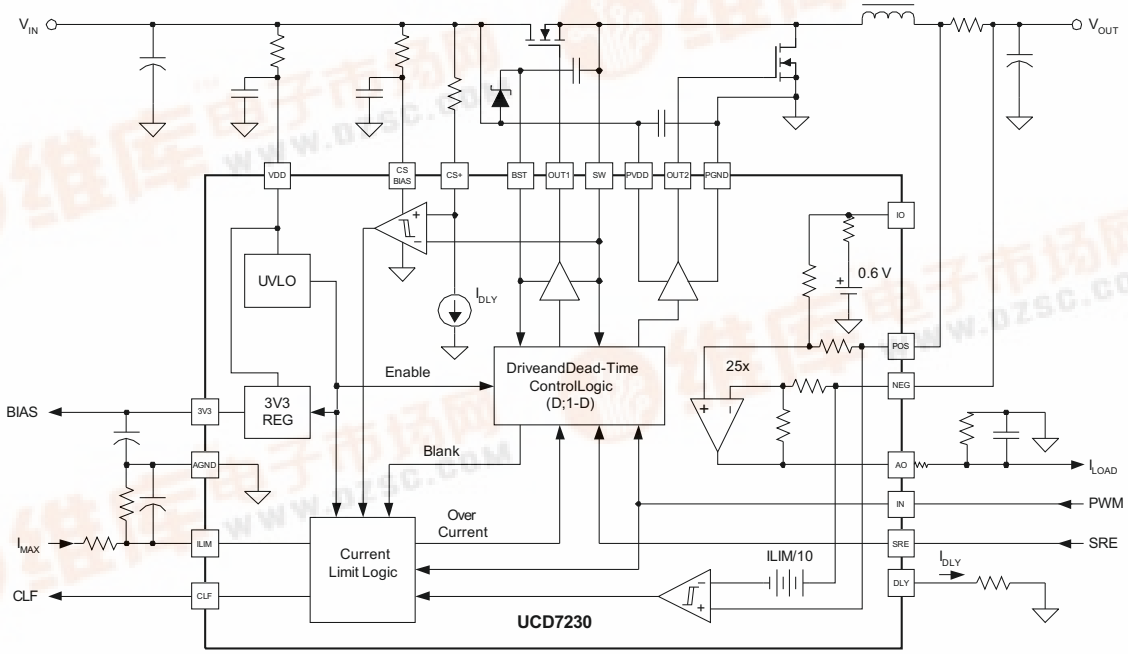
APPLICATIONS

- Digitally-Controlled Synchronous-Buck Power Stages for Single and Multi-Phase Applications
- Especially Suited for Use with UCD91xx or UCD95xx Contollers
- High-Current Multi-Phase VRM/EVRD Regulators for Desktop, Server, Telecom and Notebook Processors
- Digitally-Controlled Synchronous-Buck Power Supplies Using µCs or the TMS320TM DSP Family

DESCRIPTION

The UCD7230 is part of the UCD7K family of digital control compatible drivers for applications utilizing digital control techniques or applications requiring fast local peak current limit protection.

PRODUCT PREVIEW



The UCD7230 is a 4-A MOSFET gate driver specifically designed for synchronous buck applications. It is ideally suited to provide the bridge between digital controllers such as the UCD91xx or the UCD95xx and the power stage. With 25-ns cycle-by-cycle current limit protection, the UCD7230 device protects the power stage from faulty input signals or excessive load currents.

The UCD7230 includes high-side and low-side 4-A gate drivers which utilize Texas Instrument's TrueDrive™ output architecture. This architecture delivers rated current into the gate capacitance of a MOSFET during the Miller plateau region of the switching. Furthermore, the UCD7230 offers a low offset differential amplifier with a fixed gain of 25. This amplifier greatly simplifies the task of conditioning small current sense signals inherent in high efficiency buck converters.

The UCD7230 includes a 3.3-V, 10-mA linear regulator to provide power to digital controllers such as the UCD91xx. The UCD7230 is compatible with standard 3.3-V I/O ports of the UCD91xx, the TMS320TM family DSPs, μCs, or ASICs.

The UCD7230 is offered in PowerPAD™ HTSSOP or space-saving QFN packages. Package pin out has been carefully designed for optimal board layout

SIMPLIFIED APPLICATION DIAGRAMS

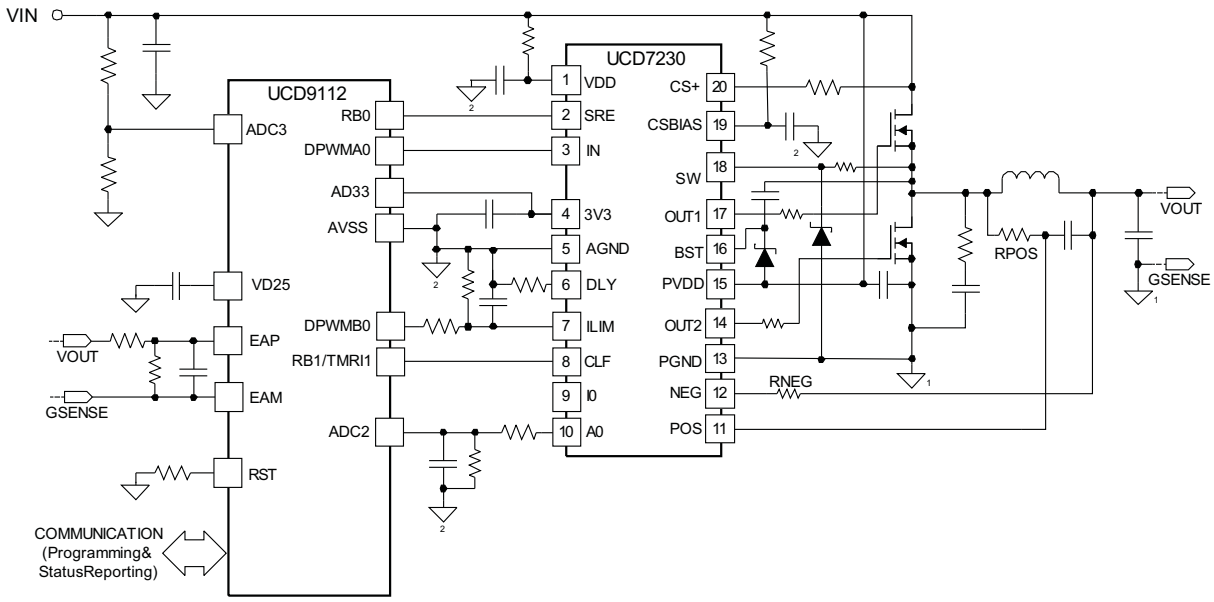


Figure 1. Single-Phase Synchronous Buck Converter using UCD9112 and one UCD7230

PRODUCT PREVIEW

SIMPLIFIED APPLICATION DIAGRAMS (continued)

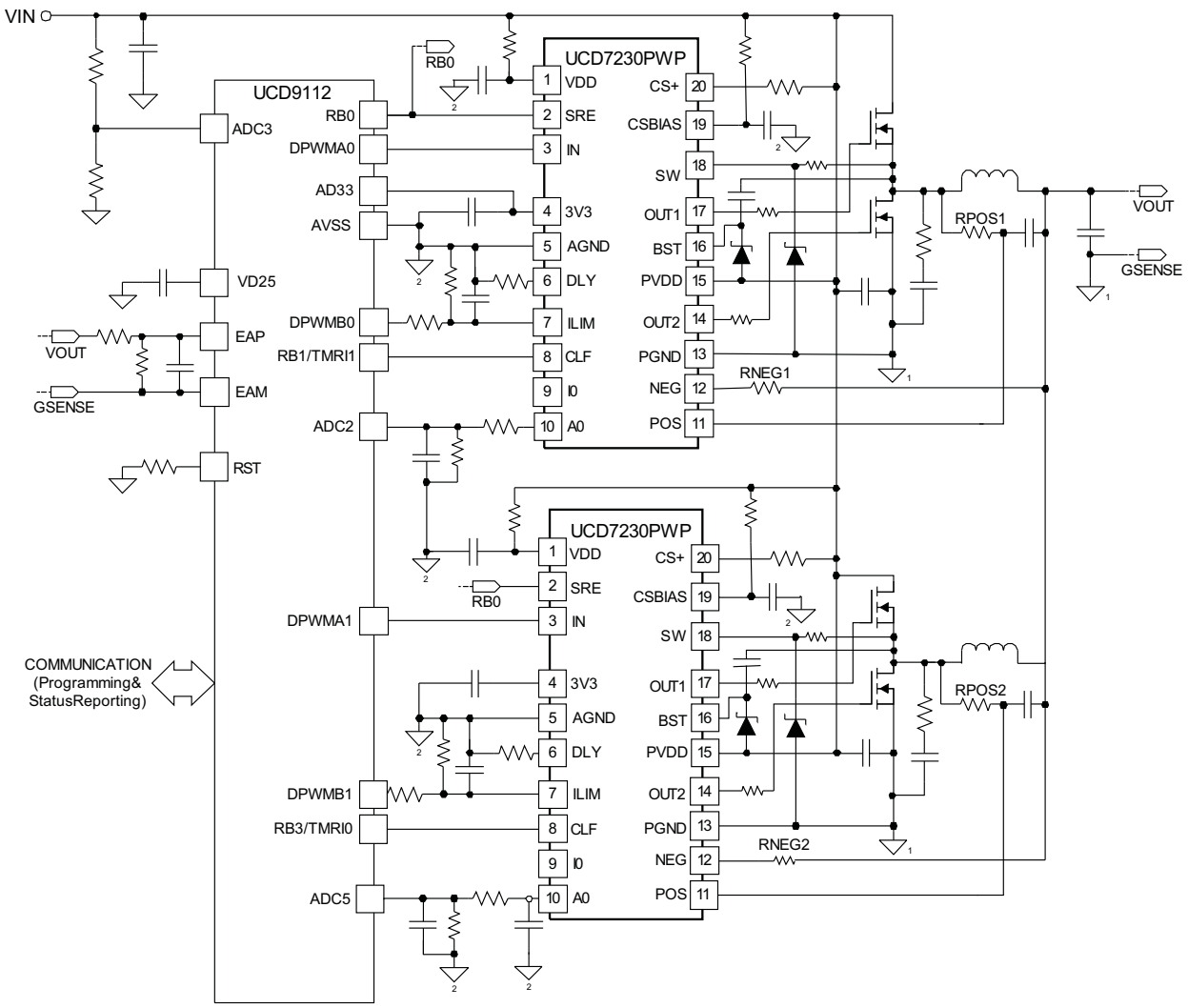
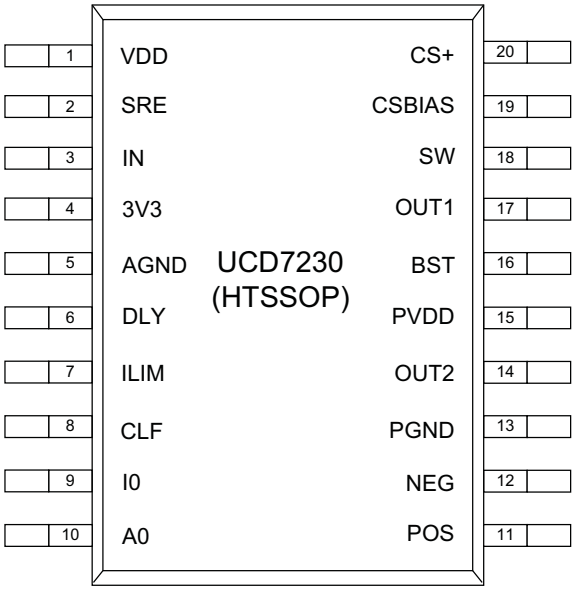
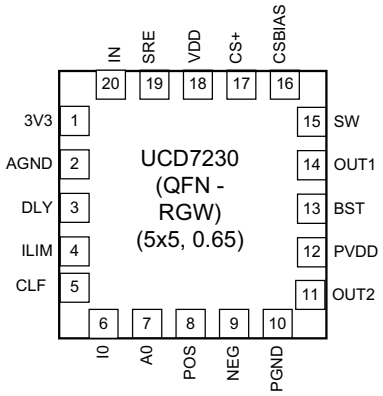


Figure 2. Multi-Phase Synchronous Buck Converter using UCD9112 and two UCD7230

PRODUCT PREVIEW

CONNECTION DIAGRAMS





ORDERING INFORMATION(1)(2)

TEMPERATURE RANGE	PACKAGED DEVICES	
	PowerPAD™ HTSSOP-20 (PWP)	QFN-20 (RGW)
-40°C to + 125°C	UCD7230PWP	UCD7230RGW

(1) These products are packaged in Pb-Free and green lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255-260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.

(2) HTSSOP-20 (PWP), and QFN-20 (RGW) packages are available taped and reeled. Add R suffix to device type (e.g. UCD7230PWPR) to order quantities of 2,000 devices per reel for the PWP package and 1,000 devices per reel for the RSA and RGW packages.

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITION	VALUE	UNIT
V_{DD}	Supply voltage		16	V
I_{DD}	Supply current	Quiescent	20	mA
		Switching, T_A = 25°C, T_J = 125°C, V_{DD} = 12 V	200	
V_O	Output gate drive voltage	OUT1, BST	-1 V to 36	V V
		OUT2	-1 V to VDD+0.3	
$I_{OUT(sink)}$	Output gate drive current	OUT1	4.0	A
$I_{OUT(source)}$		OUT1	-2.0	
$I_{OUT(sink)}$		OUT2	4.0	
$I_{OUT(source)}$		OUT2	-4.0	
	Analog inputs	SW	-1 to 20	V
		CS+	-0.3 to 20	
		CSBIAS	-0.3 to 16	
		POS, NEG	-0.3 to 5.6	
		ILIM, DLY, I0	-0.3 to 3.6	
	Analog output	A0	-0.3 to 3.6	
	Digital I/O's	IN, SRE, CLF	-0.3 to 3.6	
	Power dissipation	T_A = 25°C (PWP-20 package)	2.67	W
		T_A = 25°C (QFN-20 package)		
T_J	Junction operating temperature		-55 to 150	°C
T_{stg}	Storage temperature		-65 to 150	
HBM	ESD rating	Human body model	2000	V
CDM		Charged device model	500	
	Lead temperature (soldering, 10 sec)		300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult company packaging information for thermal limitations and considerations of packages.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

V_{DD} = P_{VDD} = 12 V, 4.7-µF from V_{DD} to A_{GND}, 1 µF from P_{VDD} to P_{GND}, 0.1 µF from CS+ to AGND, 0.22 µF from BST to SW, T_A = T_J = -40°C to +125°C, R_{CS+} = 5 kΩ, R_{DLY} = 50 kΩ over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
	Supply current, off	V_{DD} = 4.2 V		400	500	µA
	Supply current	Outputs not switching IN = LOW		4	TBD	mA
LOW-VOLTAGE UNDER-VOLTAGE LOCKOUT						
	VDD UVLO ON	V_{DD} rising	4.25	4.5	4.75	V
	VDD UVLO OFF	V_{DD} falling	4.05	4.5	4.75	
	VDD UVLO hysteresis		150	250	350	mV
REFERENCE / EXTERNAL BIAS SUPPLY						
	3V3 initial set point	T_A = 25°C	3.267	3.3	3.333	V
	3V3 over temperature		3.234	3.3	3.366	
	3V3 load regulation	I_{LOAD} = 1 mA to 10 mA, V_{DD} = 5V		1	7	mV
	3V3 line regulation	V_{DD} = 4.75 V to 12 V, I_{LOAD} = 10 mA		1	7	
	Short circuit current	V_{DD} = 4.75 V to 12 V	11	17		mA
	3V3 OK threshold, ON	3.3 V rising	2.9	3	3.1	V
	3V3 OK threshold, OFF	3.3 V falling	2.7	2.8	2.8	
INPUT SIGNAL (IN)						
INHigh	Positive-going input threshold voltage		1.65		2.08	V
INLow	Negative-going input threshold voltage		1.16		1.5	
INHigh – INLow	Input voltage hysteresis		0.6		0.8	
	Input resistance to AGND		50	100	150	kΩ
	Frequency ceiling		2			MHz
CURRENT LIMIT (ILIM)						
	ILIM internal voltage setpoint	I_{LIM}=OPEN	0.51	0.55	0.58	V
	ILIM input impedance		25	50	75	kΩ
	CLF output high level	I_{LOAD} = 7 mA	2.64			V
	CLF output low level	I_{LOAD} = 7 mA			0.66	
	Propagation delay from IN to reset CLF	2nd IN rising to CLF falling after a current limit event		15	20	ns
CURRENT SENSE COMPARATOR (OUTPUT SENSE)						
	CS threshold (POS - NEG)	I_{LIM} = open		55		mV
		I_{LIM} = 3.3 V		100		
		I_{LIM} = 0.75 V		75		
		I_{LIM} = 0.25 V		25		
	Propagation delay from POS to OUT1 falling(1)	I_{LIM} = open, CS = threshold + 60 mV		60		ns
	Propagation delay from POS to OUT2 rising(1)	I_{LIM} = open, CS = threshold + 60 mV		80		
	Propagation delay from POS to CLF(1)	I_{LIM} = open, CS = threshold + 60 mV		50		

(1) As designed and characterized. Not 100% tested in production.

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = P_{VDD} = 12 V, 4.7-µF from V_{DD} to A_{GND}, 1 µF from P_{VDD} to P_{GND}, 0.1 µF from CS+ to AGND, 0.22 µF from BST to SW, T_A = T_J = -40°C to +125°C, R_{CS+} = 5 kΩ, R_{DLY} = 50 kΩ over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE COMPARATOR (INPUT SENSE)						
	CS threshold	R_{DLY} = 50 kΩ (CSBIAS-CS+)		120		mV
		R_{DLY} = 100 kΩ (CSBIAS-CS+)		60		
	CS blanking time(2)	R_{DLY} = 50 kΩ , IN rising to OUT1, IN falling to OUT2		125		ns
	Rdelay range		25	50	100	kΩ
	Propagation delay from CS+ to OUT1(2)	CS = threshold + 60mV		60		ns
	Propagation delay from CS+ to OUT2(2)			60		
	Propagation delay from CS+ to CLF(2)			50		
CURRENT SENSE AMP						
	Closed loop dc gain (current sense resistor method)	I0 = FLOAT; V_{POS} = 1.26 V; V_{NEG} = 1.25 V	23	25	27	V/V
	Closed loop dc gain (lossless current sense method)	I0 = FLOAT; V_{POS}= 1.26 V; V_{NEG} = 1.25 V; R_{POS} = 1 kΩ		24		
	Input impedance	Differential, POS – NEG		50		kΩ
V_{CM}	Input Common Mode Voltage Range	$V_{CM(max)}$ is limited to (V_{DD}-1.2V)	-0.3		5.6	V
V_{IO}	Input Offset Voltage	I0 = FLOAT; V_{POS} = V_{NEG} = 1.25 V		1		mV
A0_Vol	Minimum Output Voltage	V_{POS} = 1.2 V; V_{NEG} = 1.3 V; A0_I_{SINK} = 250 µA		0.15	0.2	V
A0_Voh	Maximum Output Voltage	V_{POS} =1.3 V; V_{NEG} = 1.2 V; A0_ I_{SOURCE} = 500 µA	3	3.1	3.3	
POS	Input Bias Current	I0 = FLOAT; V_{POS} = V_{NEG} = 5.0 V, R_{POS} = 1 kΩ		10		uA
NEG		I0 = FLOAT; V_{POS} = V_{NEG} = 5.0 V		10		
POS		I0 = FLOAT; V_{POS} = V_{NEG} = 0.8 V, R_{POS} = 1 kΩ		2		
NEG		I0 = FLOAT; V_{POS} = V_{NEG} = 0.8 V		2		
ZERO CURRENT REFERENCE (IO)						
	Reference voltage	Measured at I0	0.54	0.6	0.66	V
	IO output offset voltage	IO open, POS = NEG = open, measure AO - IO		25		mV
	Input transition voltage	With respect to IO reference	45	50	55	
	Input transition current	Initial source current into pin to use an external I0 voltage		5		uA
I_O	Output impedance	I_{ZERO} = 0.6 V	7	10	14	kΩ

(2) As designed and characterized. Not 100% tested in production.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = P_{VDD} = 12 V, 4.7-µF from V_{DD} to A_{GND}, 1 µF from P_{VDD} to P_{GND}, 0.1 µF from CS+ to AGND, 0.22 µF from BST to SW, T_A = T_J = -40°C to +125°C, R_{CS+} = 5 kΩ, R_{DLY} = 50 kΩ over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW-SIDE OUTPUT DRIVER (OUT2)						
	Source current(3)	V_{DD} = 12 V, IN = high, OUT2 = 5 V		4		A
	Sink current (3)	V_{DD} = 12 V, IN = low, OUT2 = 5 V		4		
	Source current(3)	V_{DD} = 4.75 V, IN = high, OUT2 = 0		2		
	Sink current (3)	V_{DD} = 4.75 V, IN = low, OUT2 = 4.75 V		3		
	Rise time	C_{LOAD} = 2.2 nF, V_{DD} = 12 V		10		ns
	Fall time	C_{LOAD} = 2.2 nF, V_{DD} = 12 V		10		
	Output with VDD <UVLO	V_{DD} = 1.0 V, Isink = 10 mA		0.8	1.2	V
	Propagation delay from IN to OUT2	C_{LOAD} = 2.2 nF, V_{DD} = 12 V, IN falling		60		ns
HIGH-SIDE OUTPUT DRIVER (OUT1)						
	Source current(3)	V_{DD} = 12 V, BST = 12 V IN = High, OUT1 = 5 V		2		A
	Sink current (3)	V_{DD} = 12 V, BST = 12 V IN = Low, OUT1 = 5 V		4		
	Source current (3)	V_{DD} = 4.75 V = BST = 4.75 V, IN = High, OUT1 = 0		1		
	Sink current (3)	V_{DD} = 4.75 V, BST = 4.75 V, IN = Low, OUT1 = 4.75 V		3		
	Rise time	C_{LOAD} = 2.2 nF OUT1 to SW, VDD = 12 V		20		ns
	Fall time	C_{LOAD} = 2.2 nF OUT1 to SW, V_{DD} = 12 V		10		
	Propagation delay from IN to OUT1	C_{LOAD} = 2.2 nF, V_{DD} = 12 V, IN rising		40		

(3) As designed and characterized. Not 100% tested in production.

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	UCD7230			
	HTSSOP-20	QFN-20		
VDD	1	18	-	Supply input pin to power the internal circuitry except the driver outputs. The UCD7230 accepts an input range of 4.5 V to 15.5 V.
SRE	2	19	I	Synchronous Rectifier Enable. The SRE pin is a high impedance digital input capable of accepting 3.3-V logic level signals, used to disable the synchronous rectifier switch. The synchronous rectifier is disabled when this signal is low. A Schmitt trigger input comparator desensitizes this pin from external noise.
IN	3	20	I	The IN pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. A Schmitt trigger input comparator desensitizes this pin from external noise.
3V3	4	1	O	Regulated 3.3-V rail. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. Bypass with 0.22-µF ceramic capacitance from this pin to analog ground, AGND.
AGND	5	2	-	Analog ground return.
DLY	6	3	I	Requires a resistor to AGND for setting the current sense blanking time for both the high-side and low-side current sense comparators. The value of this resistor in conjunction with the resistor in series with the CS+ pin sets the high side current sense threshold.
ILIM	7	4	I	Output current limit threshold set pin. The output current threshold is $1/10^{th}$ of the value set on this pin. If left floating the voltage on this pin is 0.55 V. The voltage on the ILIM pin can range from 0.25 V to 1V to set the threshold from 25 mV to 100 mV.
CLF	8	5	O	Current Limit Flag. The CLF signal is a 3.3-V digital output which is latched high after an over current event, triggered by either of the two current sense comparators and reset after two clock pulses received on the IN pin.
IO	9	6	I	Sets the current sense linear amplifier “Zero” output level. The default value is 0.6 V which allows negative current measurement.
AO	10	7	O	Current sense linear amplifier output. The output voltage level on this pin represents the average output current. Any value below the level on the I0 pin represents negative output current.
POS	11	8	I	Non-inverting input of the output current sense amplifier and current limit comparator.
NEG	12	9	I	Inverting input of the output current sense amplifier and current limit comparator.
PGND	13	10	-	Power ground return. This pin should be connected close to the source of the low-side synchronous rectifier MOSFET.
OUT2	14	11	I	The low-side high-current TrueDrive™ driver output. Drives the gate of the low-side synchronous MOSFET between PVDD and PGND.
PVDD	15	12	-	Supply pin provides power for the output drivers. It is not connected internally to the VDD supply rail. The bypass capacitor for this pin should be returned to PGND.
BST	16	13	I	Floating OUT1 driver supply powered by an external Schottky diode from the PVDD pin during the synchronous MOSFET on time.
OUT1	17	14	I	The high-side high-current TrueDrive™ driver output. Drives the gate of the high-side buck MOSFET between SW and BST.
SW	18	15	I/O	OUT1 gate drive return and square wave input to output inductor.
CSBIAS	19	16	I	Supply pin for the high-side current sense comparator.
CS+	20	17	I	Non-inverting Input for the high side current sense comparator. A resistor connected between this pin and the high side MOSFET drain, in conjunction with the DLY resistor sets the high-side current limit threshold.

APPLICATION INFORMATION

Introduction

The UCD7230 is a synchronous buck driver with peak-current limiting. It is a member of the UCD7K family of digital compatible drivers suitable either for applications utilizing digital control techniques or analog applications that require local fast peak current limit protection.

In systems using the UCD7230, the feedback loop is closed externally and the IN signal represents the PWM information required to regulate the output voltage. The PWM signal may be implemented by either a digital or analog controller.

The UCD7230 has two over-current protection features, one that limits the peak current in the high-side switch and one that limits the output current. Both limits are individually programmable. The internal current sense blanking enables ease of design with real-world signals. In addition to over current limit protection, current sense signals can be conditioned by the on board amplifier for use by the system controller.

Supply Requirements

The UCD7230 operates on a supply range of 4.5 V to 15.5 V. The supply voltage should be applied to three pins, PVDD, VDD, and CSBIAS. PVDD is the supply pin for the lower driver, and has the greatest current demands. The supply connection to PVDD is also the point where an external Schottky diode provides current to the high side flying driver. PVDD should be bypassed to PGND with a low ESR ceramic capacitor. In the same fashion, the flying driver should be bypassed between BST and SW.

VDD and CSBIAS are less demanding supply pins, and should be resistively coupled to the supply voltage for isolation from noise generated by high current switching and parasitic board inductance. Use 100 Ω for CSBIAS and 1 Ω for VDD. VDD should be bypassed to AGND with a 4.7-µF ceramic capacitor while CSBIAS should be bypassed to AGND with 0.1 µF. Although the three supply pins are not internally connected, they must be biased to the same voltage. It is important that all bypassing be done with low parasitic inductance techniques to good ground planes.

PGND and AGND are the ground return connections to the chip. Ground plane construction should be used for both pins. For a MOSFET driver operating at high frequency, it is critical to minimize the stray inductance to minimize overshoot, undershoot, and ringing. The low output impedance of the drivers produces waveforms with high di/dt. This induces ringing in the parasitic inductances. It is highly desirable that the UCD7230 and the MOSFETs be collocated. PGND and the AGND pins should be connected to the PowerPAD™ of the package with two thin traces. It is critical to ensure that the voltage potential between these two pins does not exceed 0.3 V.

Although quiescent VDD current is low, total supply current depends on the gate drive output current required for the capacitive load and the switching frequency. Total supply current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from (I_{OUT} = Qg x f), where f is the operating frequency.

APPLICATION INFORMATION (continued)

Reference / External Bias Supply

The UCD7230 includes a series pass regulator to provide a regulated 3.3 V at the 3V3 pin that can be used to power other circuits such as the UCD91xx, a microcontroller or an ASIC. 3V3 can source 10 mA of current. For normal operation, place a 0.22-µF ceramic capacitor between 3V3 and AGND.

Control Inputs

IN and SRE are high impedance digital inputs designed for 3.3-V logic-level signals. They both have 100-kΩ pull-down resistors. Schmitt Trigger input stage design immunizes the internal circuitry from external noise. IN is the command input for the upper driver, OUT1, and can function up to 2 MHz. SRE controls the function of the lower driver, OUT2. When SRE is false (low), OUT2 is held low. When SRE is true, OUT2 is inverted from OUT1 with appropriate delays that preclude cross conduction in the Buck MOSFETs.

Driver Stages

The driver outputs utilize Texas Instruments' TrueDrive™ architecture, which delivers rated current into the gate of a MOSFET when it is most needed, during the Miller plateau region of the switching transition. This provides best switching speeds and reduces switching losses. TrueDrive™ consists of pull-up/ pull-down circuits using bipolar and MOSFET transistors in parallel. This hybrid output stage also allows relatively constant current sourcing even at reduced supply voltages.

The low-side high-current output stage of the UCD7230 device is capable of sourcing and sinking 4-A peak-current pulses and swings from PVDD to PGND. The high-side floating output diver is capable of sourcing 2 A and sinking 4-A peak-current pulses. This ratio of gate currents, common to synchronous buck applications, minimizes the possibility of parasitic turn on of the low-side power MOSFET due to dv/dt currents during the rising edge switching transition.

If further limiting of the rise or fall times to the power device is desired, an external resistance can be added between the output of the driver and the power MOSFET gate. The external resistor also helps remove power dissipation from the driver.

The driver outputs follows the IN and SRE as previously described provided that VDD and 3V3 are above their respective under-voltage lockout thresholds. When the supplies are insufficient, the chip holds both OUT1 and OUT2 low.

It is worth reiterating the need mentioned in the supply section for sound high frequency design techniques in the circuit board layout and bypass capacitor selection and placement. Some applications may generate excessive ringing at the switch-inductor node. This ringing can drag SW to negative voltages that might cause functional irregularities. To prevent this, carefull board layout and appropriate snubbing are essential. In addition, it may be appropriate to couple SW to the inductor with a 1-Ω resistor, and then bypass SW to PGND with a low impedance Schottky diode.

Current Sensing and Overload Protection

Since the UCD7230 is physically collocated with the high-current elements of the power converter, it is logical that current be monitored by the chip. An internal instrumentation amplifier conditions current sense signals so that they can be used by the control chip generating the pwm signal.

POS and NEG are inputs to an instrumentation amplifier circuit. This amplifier has a nominal gain of 25 and presents its output at AO. This can be used to monitor a parallel RC around the buck inductor shown in Figure 3. As long as the R_{POS} x C time constant is the same as the L/R of the inductor and its parasitic equivalent series resistance, then the voltage on C is the same as the I_R drop on the parasitic inductor resistance. Signals in this method can be very small, so the amp is necessary to condition the signals to useful amplitudes. Should more accurate current sensing be required, a sense resistor can be placed between the buck inductor and output capacitor. Since that resistor represents inefficiency to the converter, it will also be a very small value of resistance with small signals, and, again, the amp conditions the signal to useful size.

APPLICATION INFORMATION (continued)

The internal configuration of the instrumentation amplifier is such that AO is 0.6 V when POS – NEG = zero. Because of this output offset, the amplifier can accurately pass information for both positive and negative load current. The offset is controlled by IO. If IO is left to float, the offset is 0.6 V. 0.6 V is present at IO through an internal 10-kΩ resistor and should be bypassed to AGND. If a higher value of offset is desired, a voltage in excess of 0.65 V can be externally applied to IO. Once IO is forced above 0.65 V, the internal 10 kΩ is disconnected, and then the AO output offset is now equal to the voltage at IO. The transfer function of the amplifier is given by:

$$AO = 25(POS - NEG) + IO$$

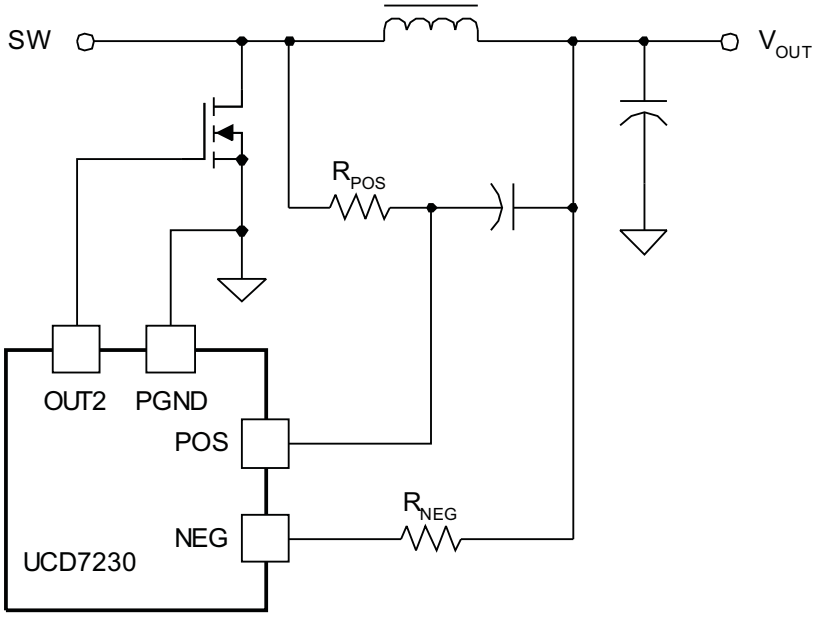


Figure 3. Lossless Average Output Current Sensing Using DC Resistance of the Output Inductor

APPLICATION INFORMATION (continued)

While the amp faithfully passes the sensed current signal, it should be noted that the amplifier is bandwidth limited for normal switching frequencies. Therefore, AO represents a moving average of the sensed current. Should noise filtering be desired, a capacitor, not to exceed 220 pF, can be placed from AO to AGND. There is a 1-kΩ resistor between the amplifier output and A0 for this cap to work with. Alternately, a capacitor can be connected between POS and NEG to filter against the R_{POS} resisance.

Note that inferring inductor current by use of a parallel RC has the following caveats. As long as the R_{POS} x C time constant is the same as L/R, then the voltage across C is the same as the IR drop across the equivalent R of the inductor. If the time constants don't match, the average voltage across C is still the same as the average voltage across R, but the indication of ripple current amplitude will be off. Tolerance of the value of R in the inductor has a direct effect on measurement accuracy, as does the temperature coefficient of R. Copper has a temperature coefficient of approximately 3800 ppm/°C. For a 100 °C rise in winding temperature, the dc resistance of the inductor increases by 38%. The worst case scenario would be a cracked core or under-designed inductor in which cases the core could tend towards saturation. In that scenario, inductor current could change slope drastically and is not correctly modeled by the capacitor voltage.

For impedance matching and best common mode rejection, a resistor, $R_{NEG} = R_{POS}$, should be inserted in series with NEG as shown in Figure 3. R_{POS} slightly lowers the amplifier gain, and therefore should be kept ≤ 1 kΩ.

The amp output can go up to 3.3 V, so reasonable designs limit full scale to 3.0 V. Should attenuation be necessary, use a resistive divider between AO and the control chip A/D input as shown in Figure 4.

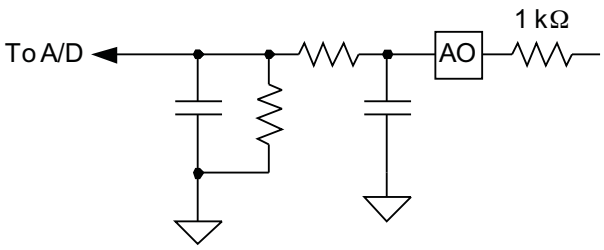


Figure 4. Level Shifting and Filtering the Voltage Representation of the Average Output Current

PRODUCT PREVIEW

APPLICATION INFORMATION (continued)

While the current sense amplifier is useful for accurate current monitoring or controlling overload conditions, extreme overload conditions must be handled in timeframes that are generally much shorter than the A/D of a control chip can achieve. Therefore, there are two comparators on the UCD7230 to sense extreme overload and protect the driven power MOSFETs.

Extreme current overload is handled in two ways by the UCD7230. One is a comparator that monitors the voltage between POS and NEG, or effectively the output current of the converter as shown in Figure 3. The other is a comparator that monitors the voltage drop across the high side MOSFET, or effectively the input current. Should either condition exceed a preset value, OUT1 is immediately turned off for the remainder of the cycle.

To program the current limit, a value of resistance from DLY to AGND must first be chosen to establish a blanking time during which the comparators will be blinded to switching noise. The blanking time starts with the rising edge on IN for the input comparator and from both the rising and falling edge of IN for the output comparator. Blanking time is given by:

$$t_{BLANK}(ns) = 2.5R_{DLY}(k\Omega)$$

where R_{DLY} is the resistor from DLY to AGND. R_{DLY} should be limited to a range of 25 kΩ to 100 kΩ.

Once R_{DLY} has been chosen, the threshold for the input comparator, i.e., the drop allowed across the high-side MOSFET, is given by:

$$V_{CS(in)} = 1.2 \bullet (R_{CS+} / R_{DLY})$$

Where $V_{CS(in)}$ is the threshold of allowed voltage across the high-side MOSFET and R_{CS+} is a resistor connected from CS+ to the drain of the high-side MOSFET.

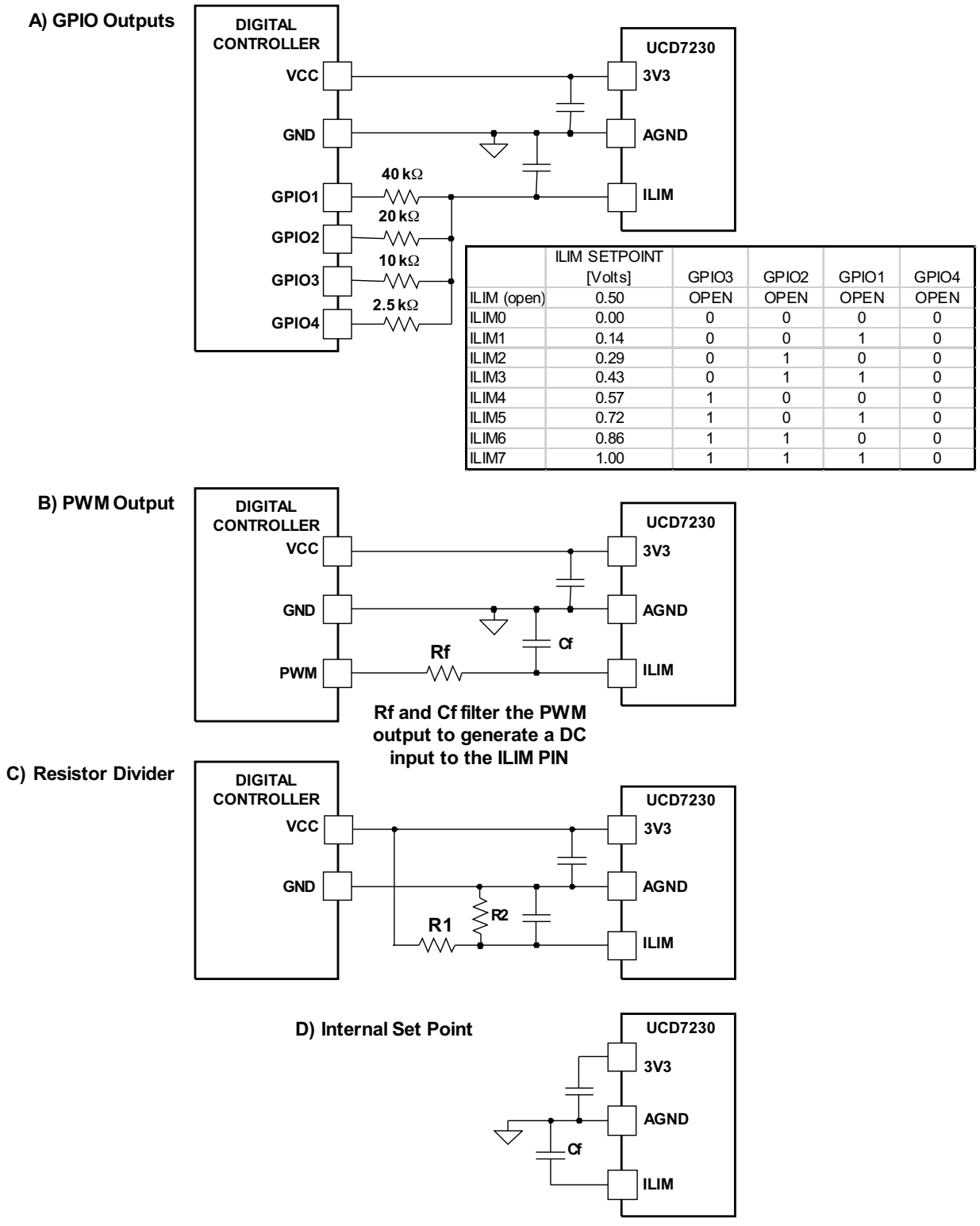
The blanking time for the output comparator is identical to the input comparator. The output comparator threshold is given by:

$$V_{CS(out)} = I_{LIM} / 10$$

Where $V_{CS(out)}$ is the threshold of allowed voltage between the POS and NEG pins and I_{LIM} is the voltage on the ILIM pin. Note that the ILIM is internally connected to 0.5 V through a 40-kΩ resistor. Any voltage between 0.25 V and 1.0 V can be applied to ILIM. For voltages above 1.0 V, the maximum $V_{CS(out)}$ threshold is clamped to 0.1 V. Possible methods for setting ILIM are shown in Figure 5.

When using the output comparator to monitor the voltage on the parallel sensing capacitor across the inductor, the same caveats apply as described for the current sense amplifier.

APPLICATION INFORMATION (continued)



	ILIM SETPOINT [Volts]	GPIO3	GPIO2	GPIO1	GPIO4
ILIM (open)	0.50	OPEN	OPEN	OPEN	OPEN
ILIM0	0.00	0	0	0	0
ILIM1	0.14	0	0	1	0
ILIM2	0.29	0	1	0	0
ILIM3	0.43	0	1	1	0
ILIM4	0.57	1	0	0	0
ILIM5	0.72	1	0	1	0
ILIM6	0.86	1	1	0	0
ILIM7	1.00	1	1	1	0

Figure 5. Setting the ILIM Voltage with: A) GPIO Outputs, B) PWM Output, C) Resistor Divider, D) Internal Set Point.

APPLICATION INFORMATION (continued)

If either comparator threshold is exceeded, OUT1 is immediately turned off for the remainder of the cycle and CLF is asserted true. Upon the rising edge of IN, the switches resume normal operation, but the CLF assertion is maintained. If a fault is not detected in this switching cycle, then the next rising edge of IN removes the CLF assertion. However, if one of the comparators detects a fault, then CLF assertion continues. It is the privilege of the control device to monitor CLF and decide how to handle the fault condition. Meanwhile, the protection comparators protect the power MOSFET switches on a cycle-by-cycle basis. Note that when a fault condition causes OUT1 to be driven low, and OUT2 behaves as if the input pulse had been terminated normally. In some fault conditions, it is advantageous to drive OUT2 low. SRE can be used to cause OUT2 to remain low at the discretion of the control chip. This can be used to achieve faster discharge of the inductor and also to fully disconnect the converter from the output voltage.

Startup Handshaking

The UCD7230 has a built-in handshaking feature to facilitate efficient start-up of the digitally controlled power supply. At start-up the CLF flag is held high until all the internal and external supply voltages of the device are within their operating range. Once the supply voltages are within acceptable limits, CLF goes low and the device will process input commands. The digital controller should monitor CLF at start-up and wait for CLF to go low before sending pwm information to the UCD7230.

Thermal Management

The usefulness of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a power driver to be used over a particular temperature range, the package must allow for the efficient removal of the heat while keeping the junction temperature within rated limits. The UCD7230 is available in PowerPAD™ HTSSOP and QFN packages to cover a range of application requirements. Both have the exposed pads to remove thermal energy from the semiconductor junction.

As illustrated in Reference [3 & 4], the PowerPAD™ packages offer a lead-frame die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board (PCB) directly underneath the device package, reducing the θJ_A down to 38°C/W. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference [3].

Note that the PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device. The PowerPAD™ should be connected to the quiet ground of the circuit.

PRODUCT PREVIEW

REFERENCES

1. Power Supply Seminar SEM-1600 Topic 6: *A Practical Introduction to Digital Power Supply Control*, by Laszlo Balogh, Texas Instruments Literature No. SLUP224
2. Power Supply Seminar SEM–1400 Topic 2: *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, Texas Instruments Literature No. SLUP133.
3. Technical Brief, *PowerPad Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002
4. Application Brief, *PowerPAD™ Made Easy*, Texas Instruments Literature No. SLMA004

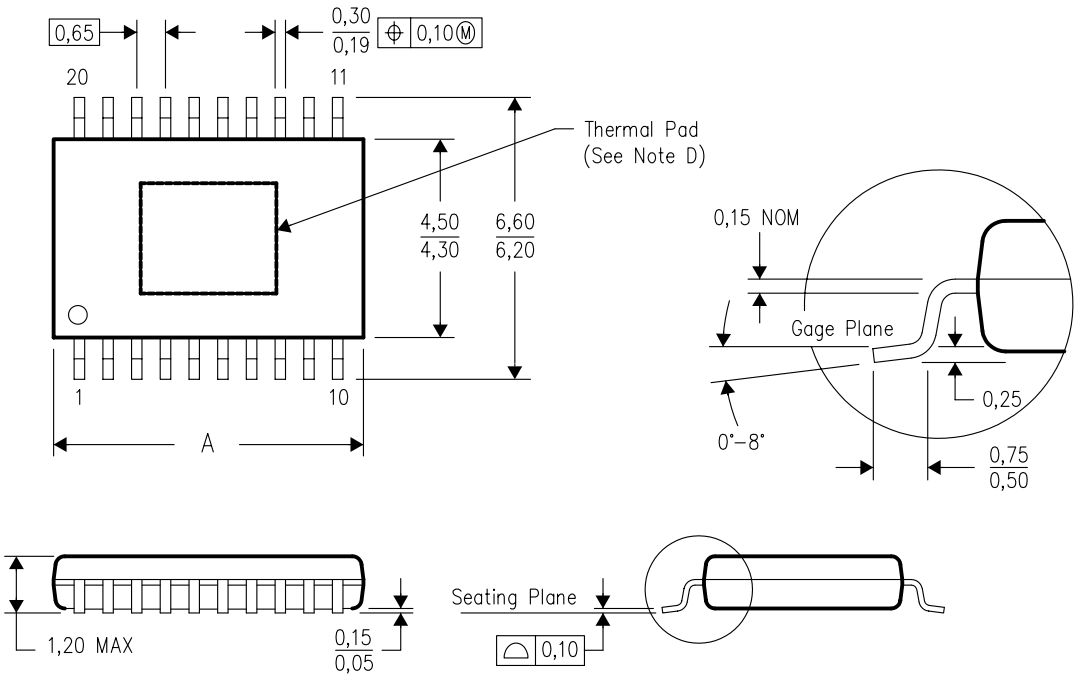
RELATED PRODUCTS

RELATED PRODUCTS

PRODUCT	DESCRIPTION	FEATURES
UCD9501	Digital power controller for high performance multi-loop applications	
UCD9111	Digital power controller for power supply applications	
UCD9112	Digital power controller for power supply applications	

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



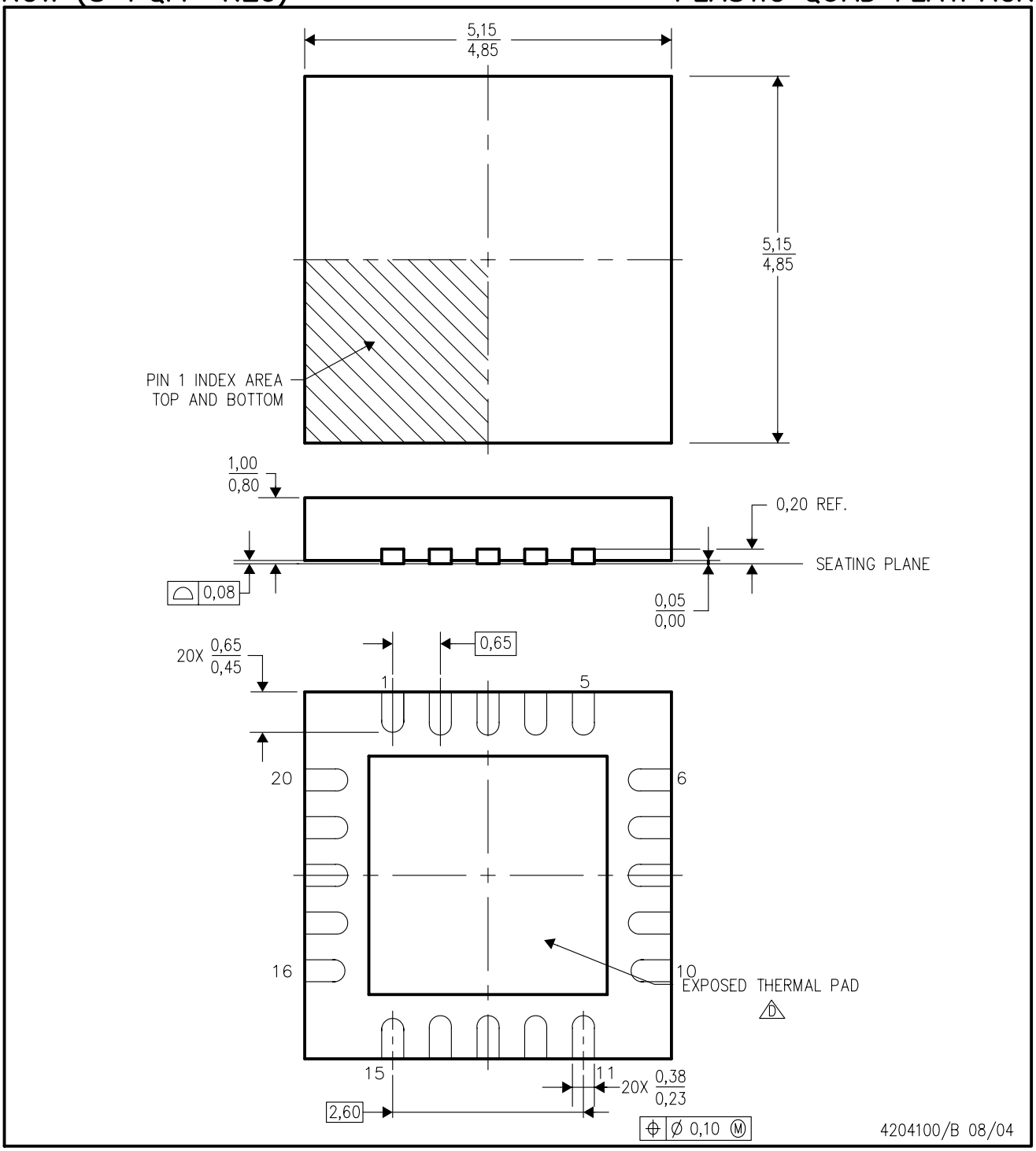
DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

RGW (S–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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