Laser Controller

Description

The U8601B is a very high-speed laser controller circuit for rewritable optical disk systems. It comprises servo amplifier, high frequency modulator, power generators, pulse width generators, serial interface, and operation control unit.

The wideband and high-gain **Servo Amplifier** drives the laser diode up to 180 mA. It performs noise reduction of the laser by a feedback loop via optical path and monitor diode. The reference input current for the servo loop is digitally controlled by power and pulse width generators.

For reduction of laser mode hopping noise during read mode, the **High Frequency Modulator** adds a weak modulation current with 288 to 456 MHz and a maximum swing of 5 mA.

Three **Power Generators** define read, erase, and write power levels with 4-bit resolution each.

In write mode, two **Pulse Width Generators** generate write pulse trains and off pulses. Three different write strategies are supported. The widths of the each first write pulse and of the off pulse width are variable in fractions of the master clock cycle.

Read and write actions are controlled by write gate (WGATE), write data (DATAIN1), writing flag (M3T), and the master clock (MCLK).

Besides the built-in write pulse generation, external digital modulation (mode DEM) as well as external analog modulation (Pin EXTM) are possible.

Parameters for power, pulse widths, and mode sets are programmed via the **Serial Interface**. Data packets of 16 bit length can be received with a maximum clock rate of 10 MHz. Reception is acknowledged by a 17th serial bit.

The **Operation Control Unit** supervises power supply voltage, servo amplifier error signal, current limiter status, and manages laser shutdown, slow start, and idle mode.

Features

- Single + 5 V power supply
- Master clock range 24 MHz to 38 MHz
- Servo system
  – 100 MHz closed loop bandwidth
  – 110 dB DC gain
  – up to 180 mA LD drive current
  – 5 ns rise/fall times
  – servo gain adjustable
- Noise reduction by servo loop and weak high frequency modulation
- Built-in pulse generation for DVD RAM
  – supports 3 write strategies:
    FLC = 1:1:1, 1.5:0.5:1, and 0.5:0.5:1
  – first write pulse width variable in Tw/8 steps
  – off pulse width variable in Tw/4 steps
  – OPE parameter for off pulse enable
- General purpose analog and digital modulation inputs
- On-chip generation of 3 power levels for read, erase, and write operations
- Control of power, pulse width and mode parameters by serial 3-wire interface
- External set resistor for basic power level
- Supervision of power supply, laser current and laser power
- Laser shutdown to prevent laser damage and data loss
- Idle mode for power saving

Ordering Information

Extended Type Number	Package	Remarks
U8601B-B	SSO44	

Block Diagram

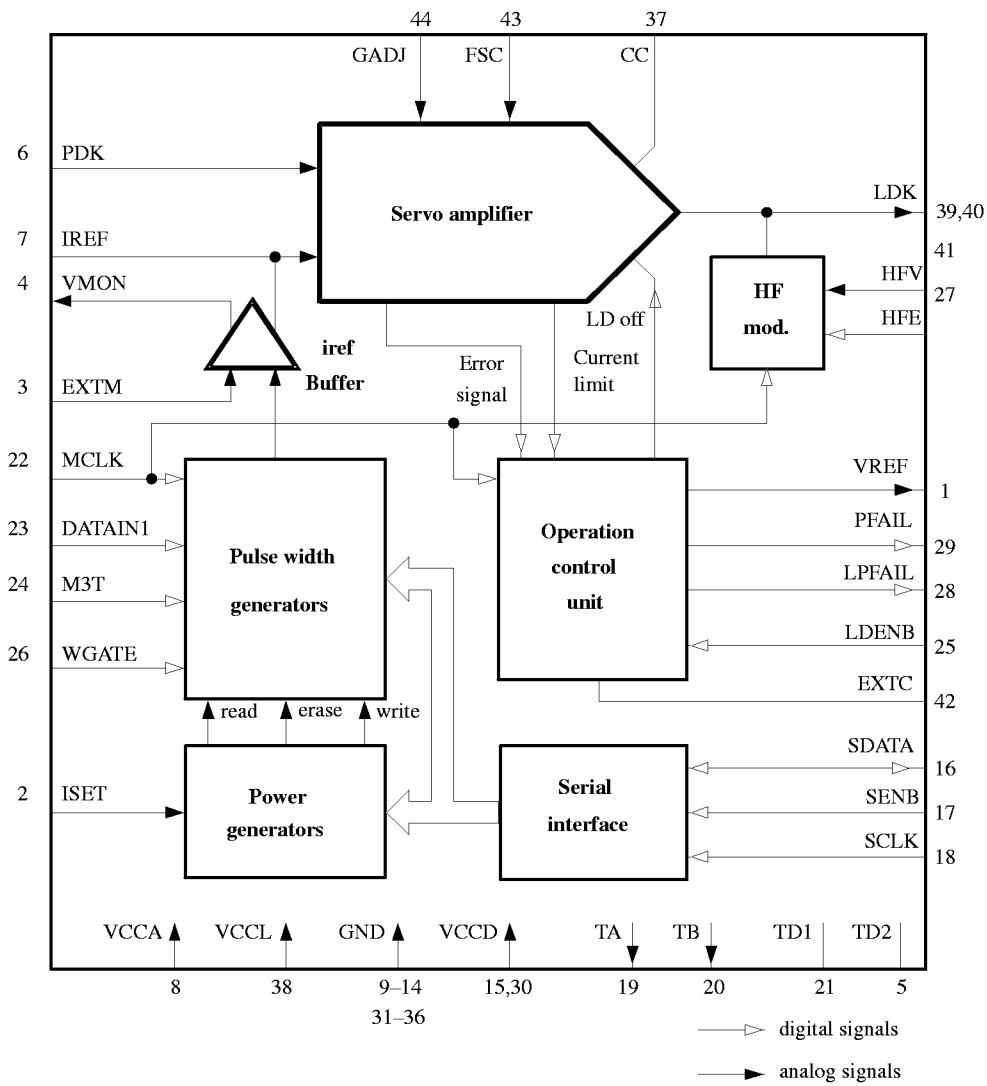


Figure 1. Block diagram

Pin Description

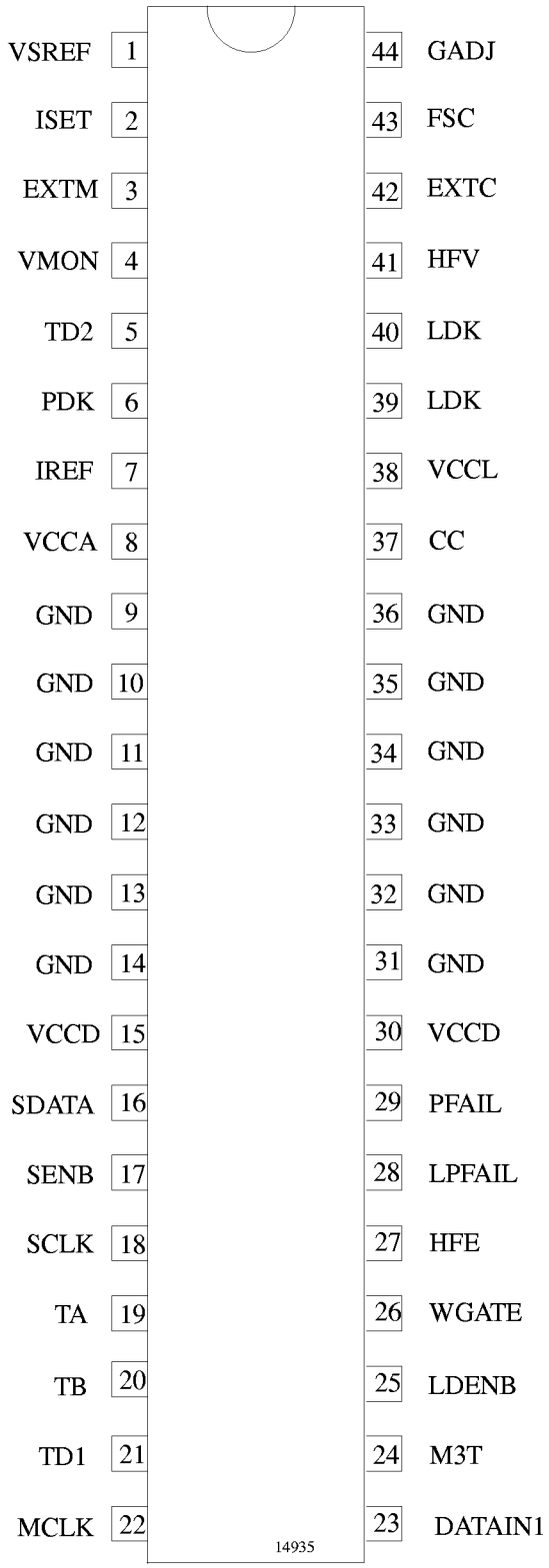


Figure 2. Pinning SSO44

Pin	Symbol	Function
1	VREF	Reference voltage output
2	ISET	Set input for basic power level
3	EXTM	External modulation signal input
4	VMON	Monitor current, servo reference
5	TD2	Test diode 2
6	PDK	PD cathode, servo amplifier input
7	IREF	Connection to servo reference input
8	VCCA	Power supply
9–14	GND	Ground & heat conduction
15	VCCD	Power supply
16	SDATA	Serial data input
17	SENB	Serial port enable input
18	SCLK	Serial clock input
19	TA	Test output A
20	TB	Test output B
21	TD1	Temperature test diode 1
22	MCLK	Master clock input
23	DATAIN1	Write data pulse and DEM input
24	M3T	Writing flag and DEM input
25	LDENB	LD control enable input
26	WGATE	Write mode gate input
27	HFE	HFM enable input
28	LPFAIL	Laser-power fail signal
29	PFAIL	Power-supply fail signal
30	VCCD	Power supply
31–36	GND	Ground & heat conduction
37	CC	Connection to internal low-pass filter
38	VCCL	Power supply
39	LDK	LD cathode, servo amplifier output
40	LDK	LD cathode, servo amplifier output
41	HFV	HFM power-control input
42	EXTC	External slow starter capacitor
43	FSC	Frequency slope control input
44	GADJ	Gain adjust for servo amplifier

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_{CC}	–0.5 to +6.0	V
Supply voltage differences between VCCA, VCCL, and VCCD	ΔV_{CC}	±0.1	V
Input voltage at any input	V_{in}	–0.5 to VCC+0.5	V
LD drive current	I_{LDK}	200	mA
Power dissipation	P_{tot}	1	W
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	–65 to +125	°C

Recommended Operating Conditions

Parameters	Symbol	Value	Unit
Supply-voltage range	V_{CC}	4.75 to 5.25	V
Operating-temperature range	T_{amb}	0 to +75	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction case	R_{thJC}	22	°C/W

DC Characteristics

VCCA = VCCL = VCCD = 5 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply						
Idle mode, VH = 5 V, VE = 0 V, LDENB = low						
Supply current, VCCA	Pin 8	Ii_{VCCA}		9		mA
Supply current, VCCL	Pin 38	Ii_{VCCL}		5		mA
Supply current, VCCD	Pins 15 and 30	Ii_{VCCD}		7		mA
Active mode, LDENB = HFE = high, WGATE = low, power data = preset, RSET = 11.2 kΩ, f_{MCLK} = 24 MHz, I_{LDK} = 50mA						
Supply current, VCCA	Pin 8	I_{VCCA}	40	48	52	mA
Supply current, VCCL	Pin 38	I_{VCCL}	18	26	32	mA
Supply current, VCCD	Pins 15 and 30	I_{VCCD}	18	27	32	mA
Supply current vs. I_{LDK}	I_{LDK} > 50 mA Pin 38	$\Delta I_{LDK}/\Delta I_{VCCL}$		0.04		mA/mA
Servo amplifier						
Bias voltage	Figure 13 Pin 6	V_{PDK}	2.5		4.0	V
Temperature drift	iref ≥ 50 µA Pin 6	ΔV_{PDK}		0.8		mV/°C
Offset voltage	Pins 6 and 7	$V_{PDK}-V_{IREF}$	–5		5	mV
Offset current	iref = 0 µA, I_{LDK} = 50 mA Pin 6	$Ioff_{PDK}$	–5		5	µA
Input voltage range	Pin 43	V_{FSC}	1.5		3.0	V
	Pin 44	V_{GADJ}	1.5		3.0	V
Bias voltage	Pin 37	V_{CC}		2.5		V

DC Characteristics (continued)

VCCA = VCCL = VCCD = 5 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Limiting current	Pins 39 and 40	I_{LDKlim}	180		300	mA
Voltage compliance	Pins 39 and 40	V_{LDK}	1.0		5.5	V
iref buffer						
Voltage compliance	Pin 4	V_{VMON}	3.5			V
Bias voltage	I_{EXTM} = 1 mA Pin 3	V_{EXTM}		0.8		V
Input current	Pin 3	I_{EXTM}			2	mA
Current ratio	Pin 3	iref / I_{EXTM}		0.6	0.8	–
HF modulator						
Bias voltage	Pin 41	V_{HFV}		1.6		V
Input current	Pin 41	I_{HFV}			1	mA
Current ratio, output current swing / control input current	Pins 40 and 41	i_{LDKhfm} / I_{HFV}		6		–
Power generators RSET = 11.2 kΩ						
Offset voltage	Pins 1 and 2	V_{ISET}– V_{VREF}	–3		3	mV
External resistor	|offset| < 3 mV Pin 2	RSET		11.2		kΩ
	|offset| < 50 mV Pin 2	RSET	7			kΩ
Temperature drift of iref	Pin 4	ΔI_{VMON}		0.3		%/°C
Read level, LSB	Pin 4	Ir1	2	4	6	µA
Read level, rdata = 9 (preset)	Pin 4	Ir9	32		40	µA
Erase level, LSB	Pin 4	Ie1	12	16	20	µA
Erase level, edata = 9 (preset)	Pin 4	Ie9	128		160	µA
Write level, LSB	Pin 4	Iw1	21	28	35	µA
Write level, wdata = 9 (preset)	Pin 4	Iw9	238		266	µA
Offset current, read level	WGATE = 0 Pin 4	Ir0			0.3	µA
Offset current, erase level	WGATE = 1 Pin 4	Ie0			0.8	µA
Ratio, erase/read level	Preset levels Pin 4	ie/ir	3.7	4	4.3	–
Ratio, write/read level	Preset levels Pin 4	iw/ir	6.3	7	7.7	–
Reference voltage						
Output voltage	Pin 1	V_{VREF}	2.4	2.5	2.6	V
Temperature drift	T_{amb} = 0 to 75°C Pin 1	TD_{VREF}	–200		200	µV/°C
Power supply rejection ratio	VCC = 4.5 to 5.5 V Pin 1	PSRR	–20		20	mV/V
Source resistance	Pin 1	r_{VREF}			10	Ω
Limiting current	Pin 1	$I_{VREFlim}$	3		10	mA

DC Characteristics (continued)

VCCA = VCCL = VCCD = 5 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Operation control unit						
Lower supply threshold voltage		VCCthl	4.5		4.75	V
Upper supply threshold voltage		VCCthh	5.25		5.6	V
Supply voltage for power supply fail detection		VCCfail	1.5		7	V
Threshold for current limit switch-off		$I_{LDKswoff}$	170		280	mA
Switch-on current limit		$I_{LDKswon}$			120	mA
Threshold for loop error switch-off		I_{PDK} / iref		1.5		–
Slow starter						
Bias voltage, high status	Pin 42	V_{EXTChi}		3.0		V
Saturation voltage, low status	I_{load} = 2 mA Pin 42	V_{EXTClo}	1	1.5		V
Charge current	Pin 42	I_{EXTC}	9	17		µA
Digital inputs SDATA, SENB, SCLK, MCLK, DATAIN1, M3T, LDENB, WGATE, HFE						
L-input voltage		V_{IL}			0.8	V
H-input voltage		V_{IH}	3.5			V
Threshold voltage		V_{th}		2.5		V
L-input current		I_{IL}	–70			µA
H-input current		I_{IH}			70	µA
Open collector outputs PFAIL, LPFAIL						
L-output voltage	I_{OL} = 1 mA	V_{OL}			0.6	V
L-output current		I_{OL}			1	mA
Output leakage current		I_{OH}			10	µA
Open collector output SDATA (acknowledge output)						
L-output voltage	R_L = 2 kΩ	V_{OL}			0.6	V
L-output current		I_{OL}			3	mA
Test outputs TA, TB						
Voltage range		dVO	3		5	V
Source resistance		RO		10		kΩ
Temperature test diode TD1						
Diode voltage	I_d = 100 µA	Vd		750		mV
Temperature dependancy		ΔVd/Δδ		1.5		mV/°C
Bias current		Id			300	µA

AC Characteristics

VCCA = VCCL = VCCD = 5 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Servo amplifier						
Open loop parameters	Without LD, I_{LDK} = 100 mA					
DC gain	$V_{GADJ} = V_{FSC}$ = 2.5 V	gDC		110		dB
Low frequency pole	V_{FSC} = 2.5 V	fpLF		60		kHz
High frequency pole	V_{GADJ} = 2.5 V	fpHF		10		MHz
High frequency gain	V_{GADJ} = 2.5 V, f = 100 MHz	gHF		42		dB
Phase margin	V_{GADJ} = 2.5 V, C_{PDK} = CREF = 10 pF, f = 100 MHz	Δφ		70		°
Gain adjust range	V_{GADJ} = 1.5 V to 2.5 V, see figure 15	Δg		14		dB
Low frequency gain adjust range	V_{FSC} = 1.5 V to 2.5 V, see figure 16	ΔgLF		12		dB
Circuit parameters						
Impedance	Pin 37	r_{CC}		312 ‖ 50		Ω//pF
Series inductance	Pin 37	l_{CC}		6		nH
Input dynamic range	10% compression for max, see figure 17	iref	15		1000	µA
Optical pulse parameters V_{GADJ} and V_{FSC} adjusted for optimal pulse shape						
Rise time	10% → 90%	T_r		5		ns
Fall time	90% → 10%	T_f		5		ns
Settling time to 5%		T_{set}		20		ns
Overshoot		Aos		15		%
HF modulator						
Modulation frequency	f_{MCLK} = 24 MHz	f_{mod}		288		MHz
	f_{MCLK} = 38 MHz	f_{mod}		456		MHz
Output current swing	I_{HFV} = 833 µA	I_{LDKpp}		5		mA
Switch-off attenuation		a_{off}	30			dB
LDENB see figure 3						
Slow starter delay	CEXT = 10 nF	Tpon		2		ms
Switch-off delay	CEXT = 10 nF	Tpof			100	ns
Delay time WGATE		Tdwg	200			ns
WGATE, DATAIN1, MCLK see figure 4						
WGATE set-up time		TsWD	340			ns
DATAIN1 set-up time		TsDM	10			ns
DATAIN1 hold time		ThDM	10			ns
Period of MCLK		Tw	26		42	ns
Duty cycle of MCLK		DCM	45		55	%

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
LDK write pulse widths f_{MCLK} = 24 MHz see figure 5						
Width of first write pulse, Tfd = 4	$T_{DATAIN1}$ > 2 Tw, LPL = low	Twpf	39	41.6	44	ns
Width range of first write pulse, Tfd = 0 to 7	$T_{DATAIN1}$ > 2 Tw, LPL = low	Twpf-min,max	44		65	ns
Width increment of first write pulse	LPL = low	ΔTwpf	3	5.2	7	ns
Width of last write pulse	AOP = LPL = high	Twpl	39	41.6	44	ns
Width of intermediate write pulses	AOP = LPL = high	Twpi	18	20.8	23	ns
Duty cycle of intermediate write pulses	f_{MCLK} = 38 MHz, AOP = LPL = high	DCwp	40		60	%
LDK off pulse widths						
Width, Tcw = 2	AOP = LPL = high, wdata = 0	Top	39	41.6	44	ns
Width range, Tcw = 0 to 6	AOP = LPL = high, wdata = 0	Top-min,max	19		86	ns
Width increment of off pulse		ΔTop	8	10.4	13	ns
Operation control unit see figure 6						
Fail period	f_{MCLK} = 24 MHz	Tfail1		5.3		µs
	f_{MCLK} = 38 MHz	Tfail2		3.4		µs
Master clock fail	LPFAIL = low Pin 28	f_{MCLK}			15	MHz
Serial interface see figure 7						
SCLK pulse cycle	Pin 18	TcySCK	100			ns
SCLK pulse width high	Pin 18	TwhSCK	40			ns
SCLK pulse width low	Pin 18	TwlSCK	40			ns
SENB set up time	Pins 18 and 17	TsSEN	20			ns
SENB hold time	Pins 18 and 17	ThSEN	20			ns
SDATA set up time	Pins 16 and 18	TsSDA	15			ns
SDATA hold time	Pins 16 and 18	ThSDA	15			ns
Acknowledge time margin	Pins 16 and 18	TdACK	0			ns
Acknowledge low level delay	Pins 16 and 18	TdlACK	10		50	ns
Acknowledge high level delay	C_{load} = 20 pF Pins 16 and 17	TdhACK			100	ns

Timing Diagrams

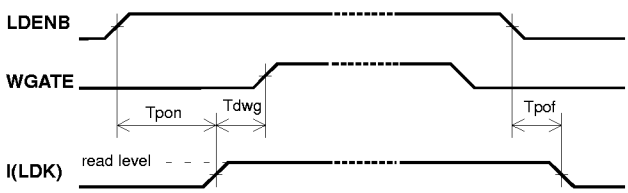


Figure 3. LDENB

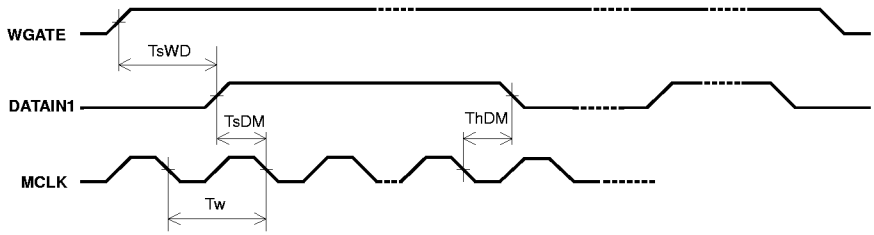


Figure 4. DATAIN1

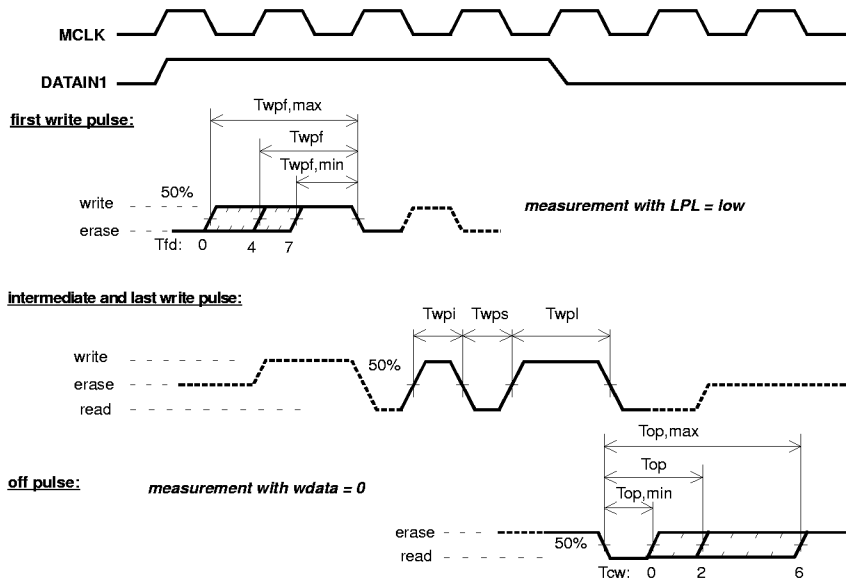


Figure 5. LDK pulses

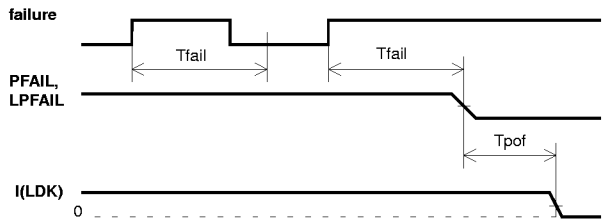


Figure 6. Failures

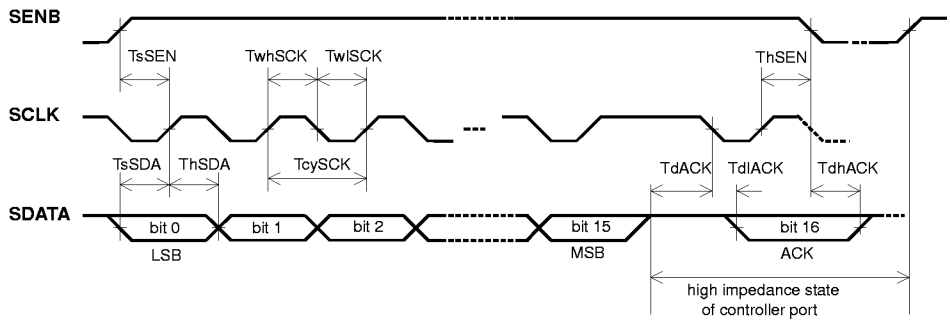


Figure 7. Serial interface

General

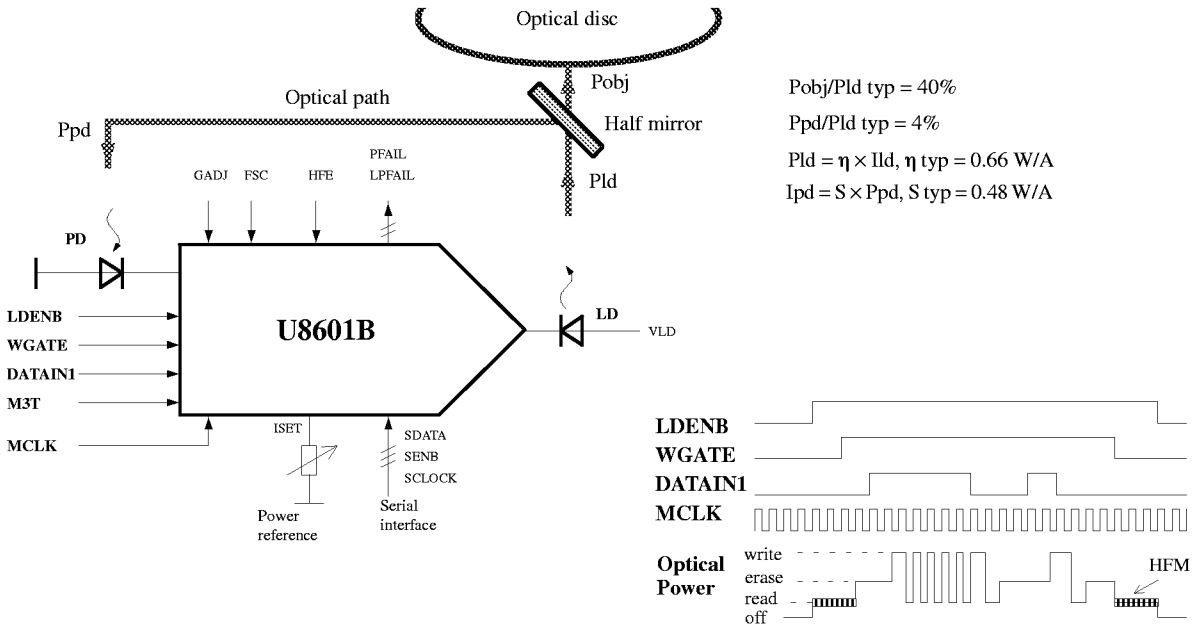
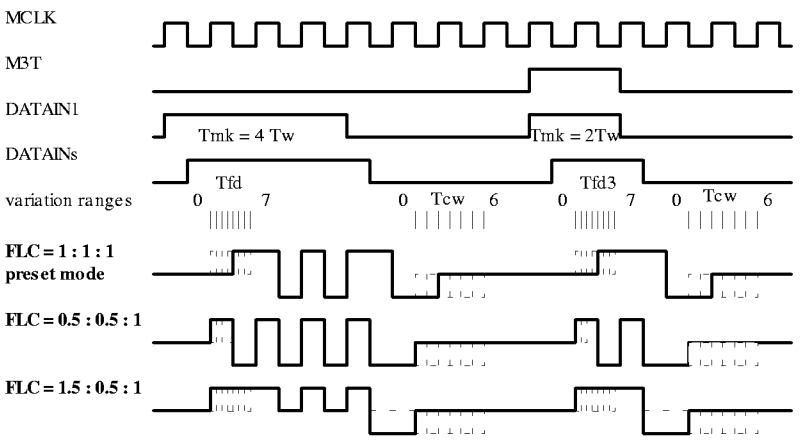


Figure 8. Simplified functional diagram



Parameter settings and M3T input signal:
(Tfd3 is selected by M3T = H)

AOP	LPL	FBL	OPE	M3T	Tfd	Tfd3	Tcw default values
H	H	L	H	L	4	4	2
L	H	H	H	L	0	0	0
L	L	L	H(L)	X	0	0	0

Figure 9. Write schemes

Glossary

MCLK: Master Clock
M3T: writing 3T Mark
DATAIN1: NRZ Data Input
DATAINs: internal synchronized data
FLC: Widths of First–/Last–/Cool–Pulse

AOP: Add One Pulse
LPL: Lower Pulse–chain Level
FBL: First Bottom Level
OPE: Off Pulse Enable

Detailed Description

Servo Amplifier

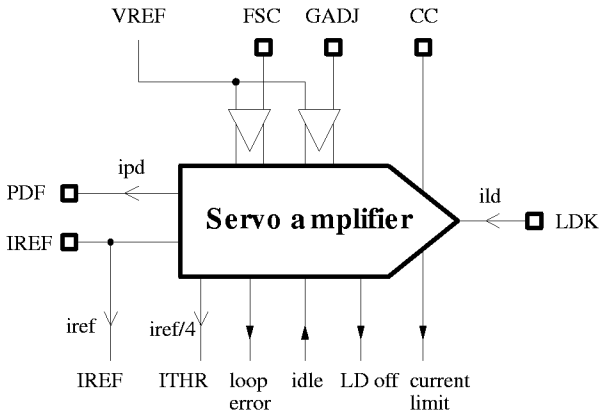


Figure 10. Block diagram

Amplifier

The servo amplifier drives the optical power of the laser diode according to the reference current, iref. The feedback loop is closed through the optical path and the photo diode which monitors the actual laser power.

The comparison of photo current, ipd, and reference current, iref, is performed within a transimpedance input stage, yielding low input impedance and biasing voltage for the operation of the grounded photo diode. For symmetry reasons a capacitor should be connected to the Pin IREF, corresponding to the total capacitance of photo diode and stray capacitance at the Pin PDK. This will improve bandwidth and noise.

A parallel amplifier technique is used to satisfy the needs for high gain and high bandwidth. By means of its high gain path, an open loop DC gain of approximately 110 dB and a first pole frequency of f1 $\approx$ 60 kHz is achieved. The pole frequency of its wideband path is set to f2 $\approx$ 10 MHz. The control input FSC (**F**requency **S**hift **C**ontrol) facilitates the correct adjustment of the frequency response slopes of the two contributing amplifiers versus production tolerances (see section "FSC Adjustment").

The total closed loop gain (amplifier gain + laser efficiency + optical path attenuation + photo diode sensitivity) is controlled at the Pin GADJ (**G**ain **ADJ**ust). Depending on tolerances of the optical parameters, the closed loop gain is adjusted by a control voltage to obtain good loop stability and pulse shape. For a closed loop bandwidth of approximately 100 MHz, the electro/optical attenuation, Δipd/Δild, has to be in the order of 36 to 40 dB.

The Pin CC is a direct connection to the integrated low-pass filter of the wideband amplifier. It can be used for possible manipulations of the frequency response, e.g., reduction of the pole frequency f2.

The output stage is capable of driving up to 180 mA laser current.

Supervision and Switch-off

Two parameters of the servo amplifier are supervised to indicate incorrect functions.

At the input, the photo current, ipd, is compared to the reference current, iref. A loop-error signal is generated if ipd exceeds iref by more than 50%. The variable threshold current for the detector is supplied through the ITHR terminal. At the output stage, a current-limit signal is generated, slightly below limiting condition.

Both error signals are fed into the operation control unit which generates a delayed LD-off signal to shut down the output stage. The idle input is provided to power down the complete servo amplifier.

FSC Adjustment

The function of the FSC input is depicted in the figures 11 and 12. With the control voltage V_{FSC}, the gain of the high gain amplifier is varied, keeping its pole frequency f1 constant. The effect is a shift of the low frequency slope of the frequency response. Concerning the transient response, a left shift of the low frequency slope (dashed line) divides the transient response into two different slopes, depending on the pole frequencies f1 and f2. Settling time is significantly increased. A right shift (dotted line) however causes an overshoot of the step response. Both deviations from the optimum frequency response yield amplitude errors for the short write and off pulses. It is recommended not to exceed V_{FSC} above the optimum value, in order to not decrease loop stability.

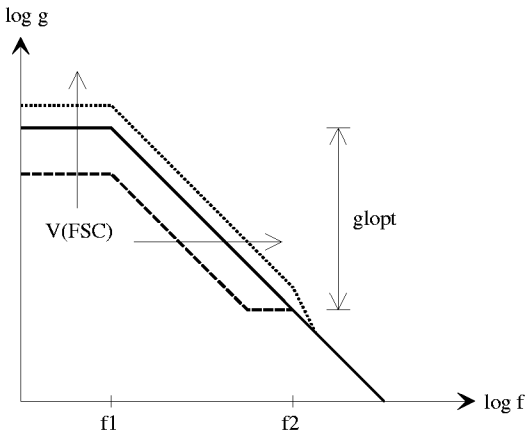


Figure 11. Principle of open loop frequency response

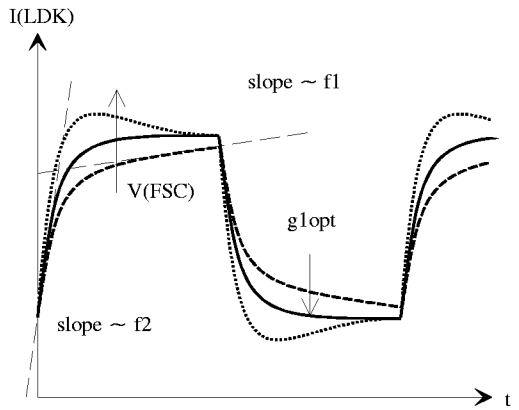


Figure 12. Transient response (closed loop)

Typical Operating Conditions

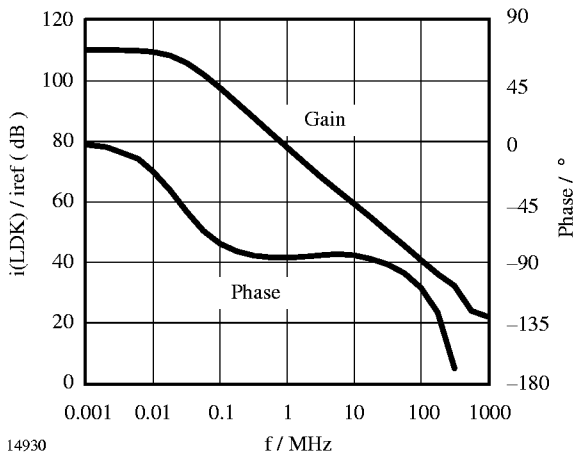


Figure 13. Open loop frequency response
(Simulation: VCC = 5 V, T_{amb} = 25°C,
V_{GADJ} – VREF = V_{FSC} – VREF = 0 V)

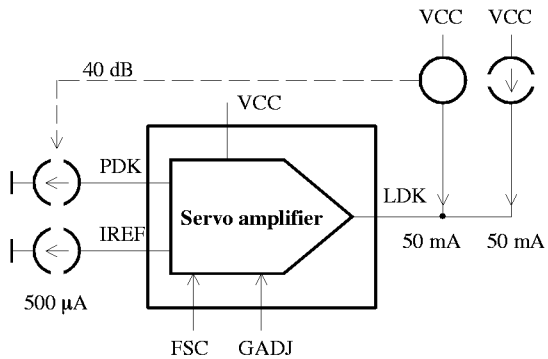


Figure 14. Simulation circuit

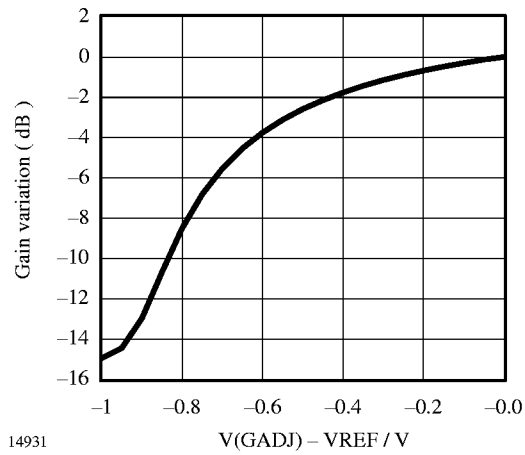


Figure 15. DC gain variation vs. V_{GADJ}, V_{FSC} = 2.5 V, (Simulation: VCC = 5 V, T_{amb} = 25°C)

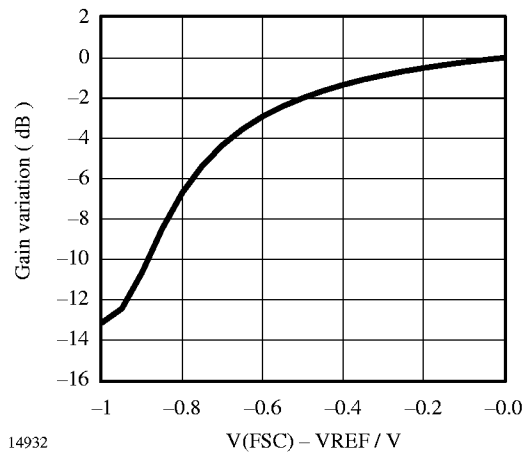


Figure 16. DC gain variation vs. V_{FSC}, V_{GADJ} = 2.5 V (Simulation: VCC = 5 V, T_{amb} = 25°C)

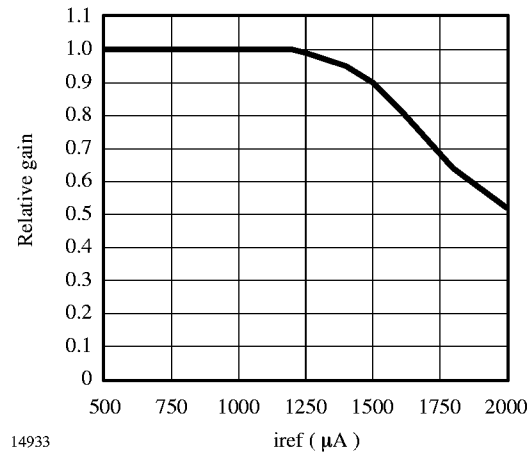


Figure 17. Input compression (gain vs. input current, iref)

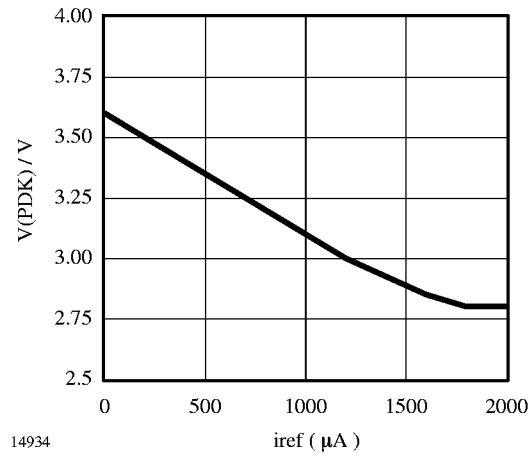


Figure 18. Bias voltage for photo diode vs iref

High Frequency Modulator

A **H**igh **F**requency **M**odulator (HFM) is integrated on the chip to reduce mode hopping noise of the laser during read mode by weak modulation.

The HFM comprises a PLL and a laser driver stage. The VCO frequency is controlled at 12 times the master clock frequency which corresponds to a HFM frequency range of 288 MHz to 456 MHz. The current swing of the laser driver stage is externally adjusted at the Pin HFV (IHFMpp ≈ 6×(VCC – 0.9 V) / RHFV; max. 5 mA), and enabled by the condition: HFE × $\overline{\text{WGATE}}$ × SLOST.

For test reasons, the VCO control signal is monitored to the test output, TA. It is separated for TM = H (test mode, see section "Serial Interface").

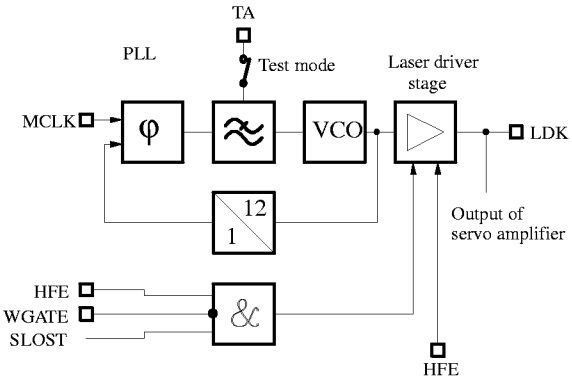


Figure 19. Simplified block diagram of HFM

Power Generators

Read, erase, and write levels are generated by 3 D/A converters with 4-bit resolution each. Their weighting ratio is 1:4:7. According to the optical efficiency, the reference currents are set by the external resistor RSET.

The read current ir is continuously contributing to the total current, tot, whereas erase current, ie, and write current, iw, are switched according the off-pulse and write-pulse signals from the pulse-width generators. Furtheron, an external analog modulation current can be added at the Pin EXTM. The buffer/ monitor block splits the total current into the reference current, iref, for the servo loop, the monitor current at the Pin VMON, and the threshold current ITHR for the servo loop monitor. Their weighting ratio is 4:2:1.

Equations for DA Currents

$$ir = \frac{iset}{4} \times \frac{rdata}{4}$$

$$ie = iset \times \frac{edata}{4}$$

$$iw = \frac{7}{4} iset \times \frac{wdata}{4}$$

Equations for Buffer Monitor

$$itot = ir + ie + iw + iextm$$

$$iref = \frac{4}{7} itot$$

DA Current Examples

RSET = 11.2 kΩ → iset = 2.5 V / 11.2 kΩ = 224 µA

Power Data		DA Output Currents (µA)			Contributions to iref (µA)		
		ir	ie	iw	iref,r	iref,e	iref,w
1	(LSB)	14	56	98	8	32	56
4		56	224	392	32	128	224
9	(preset)	126	504	882	72	288	504
15	(max)	210	840	1470	120	480	840

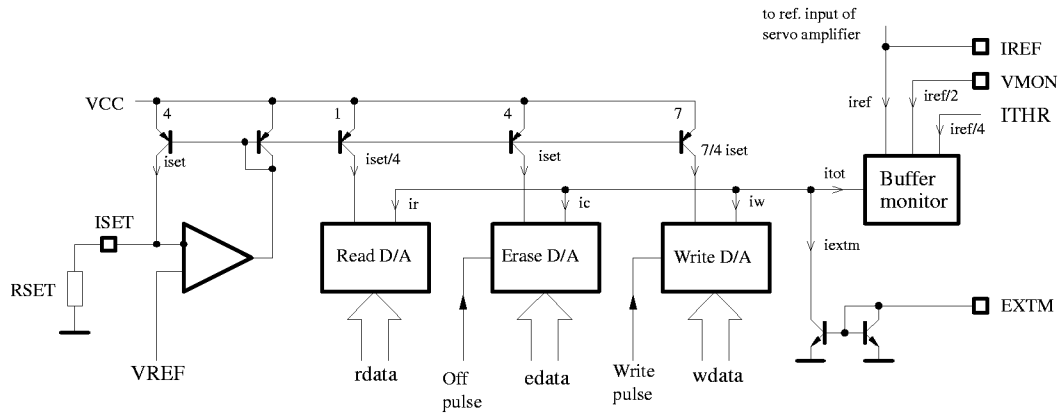


Figure 20. Simplified block diagram of power generator

Pulse Width Generators

This function block generates the signals for the write pulse train and the off pulse, switching the D/A converters for write and erase levels respectively.

General

A mark on the optical disc is generated by a write pulse train during DATAIN1 is high. The duty cycle of the separated pulses corresponds to the one of the master clock MCLK. Due to the thermal interference on the disc, the individual pulses merge to one mark. The mark is delimited by one off pulse, "cooling" down the disc material.

Three principal write pulse schemes, described by FLC (relative widths of **F**irst-/**L**ast-/**C**ool-pulse), can be selected by setting the three parameters FBL (**F**irst **B**ottom **L**evel), LPL (**L**ow **P**ulse-chain **L**evel), and AOP (**A**dd **O**ne **P**ulse), (see figure 9 "Write Schemes"). FLC = 1:1:1 is the default setting. It is also possible to set any other combination.

Table 1.

FLC	FBL	LPL	AOP	Tfd	Tcw
1 : 1 : 1	L	H	H	4	2
0.5 : 0.5 : 1	H	H	L	0	0
1.5 : 0.5 : 1	L	L	L	0	0

An additional feature is implemented to slightly shift the mark boundaries on the optical disc. The width of each first write pulse, and the off pulse width can be varied in fractions of the master clock period, Tw. The according shift parameters, Tfd and Tcw, are stored in two registers. Tfd is assigned to the delayed start of the first write pulse in steps of Tw/8 with a value range of 0 to 7. Tcw is assigned to the lengthening of the off pulse in steps of Tw/4 with a value range of 0 to 6. The default values of Tfd and Tcw are also displayed in the table above.

A special write pulse width parameter, Tfd3, is enabled by the M3T signal. It is provided simultaneously with the short data pulses Tmk = 2Tw.

Circuit Description

The pulse generation circuit comprises two parallel paths for the write pulses and the off pulse respectively. A D-flip-flop for DATAIN1 synchronization, and the Interpolator PLL for pulse width variations are common for both paths.

The write pulse generator is enabled by the synchronized data DATAINs = H. At that time, the interpolator is addressed by the Tfd parameter.

The off-pulse generator is enabled by DATAINs = low and the interpolator is now addressed by the Tcw parameter. With OPE = L, the off pulse is completely suppressed.

Both write pulses and erase level are enabled by the WGATE signal.

The interpolator enables the small pulse widths variations in steps of Tw/8 or Tw/4 respectively by the use of a PLL circuit. Depending on the input data, a shifted master clock is generated. For test reasons, the PLL control signal is monitored to the test output TB. It is separated for TM = H (test mode, see chapter "Serial Interface").

Digital External Modulation (DEM)

The versatility of the U8601B is further increased by the DEM feature. It allows the direct switching of the write and erase levels through the DATAIN1 and the M3T terminals independent from the WGATE state. The DEM mode is activated by a serial command (see chapter "Serial Interface").

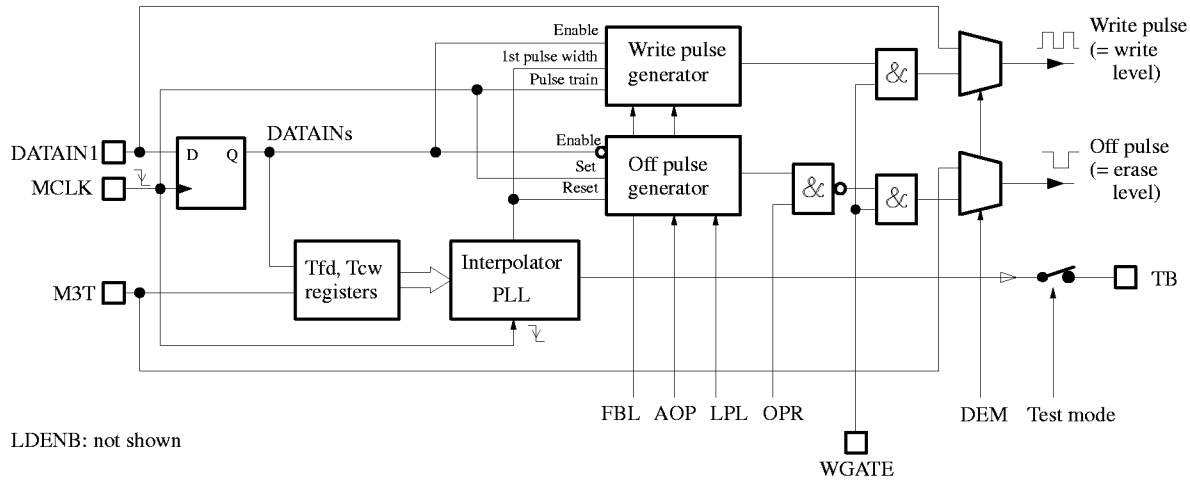


Figure 21. Simplified block diagram of pulse width generators

Operation Control Unit

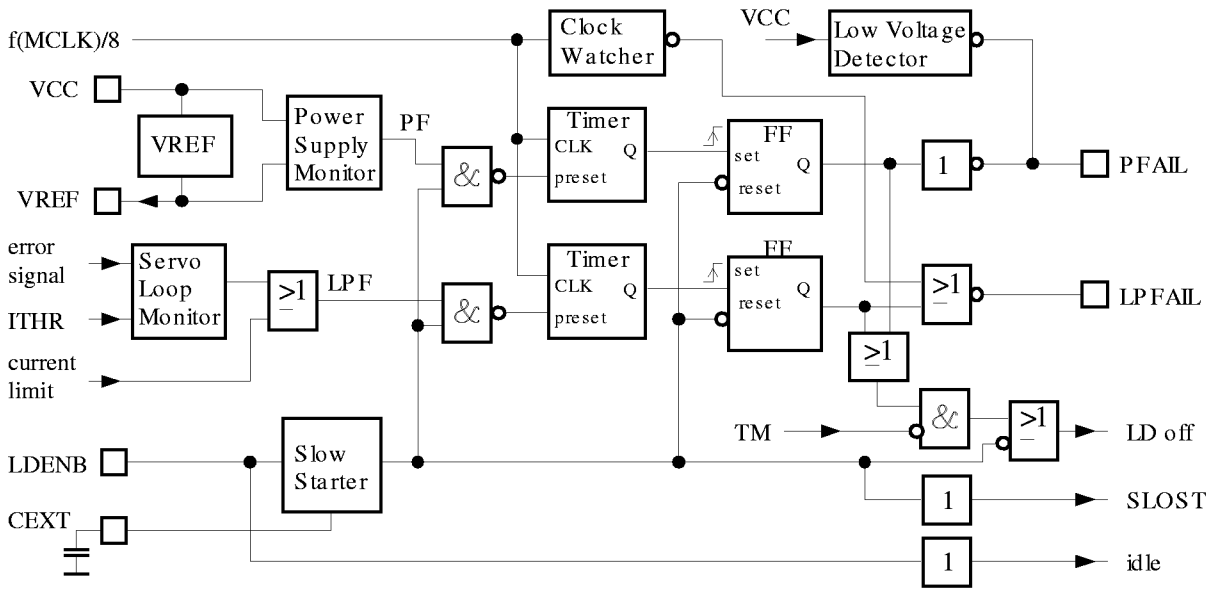


Figure 22. Block diagram of operation control unit

PFAIL signal indicates

- Power supply voltage out of window

LPFAIL signal indicates

- LDK current reaches limiting range
- LDK output transistor saturates
- Photo current exceeds reference current
- No master clock available

Failure Conditions

Power supply monitor:	VCC < 4.5 V to 4.75 V VCC > 5.25 V to 5.6 V
Low voltage detector:	VCC = 1.5 V to 3.5 V
Current limiter:	i_{LDK} > 170 mA to 280 mA
Servo loop monitor:	i_{PDK} > 1.5 × iref
Clock watcher	f_{MCLK} < 8 MHz

Timing Conditions

Timer:	Tfail = 120 × Tw to 132 × Tw Tfail @ f_{MCLK} = 4 µs to 4.4 µs
Slow Starter:	Tpon = 1 ms to 2 ms Tpoff < 2 µs

Idle Mode (LDENB = low)

Slow starter circuitry and the VREF generator remain active in idle mode.

Serial Interface

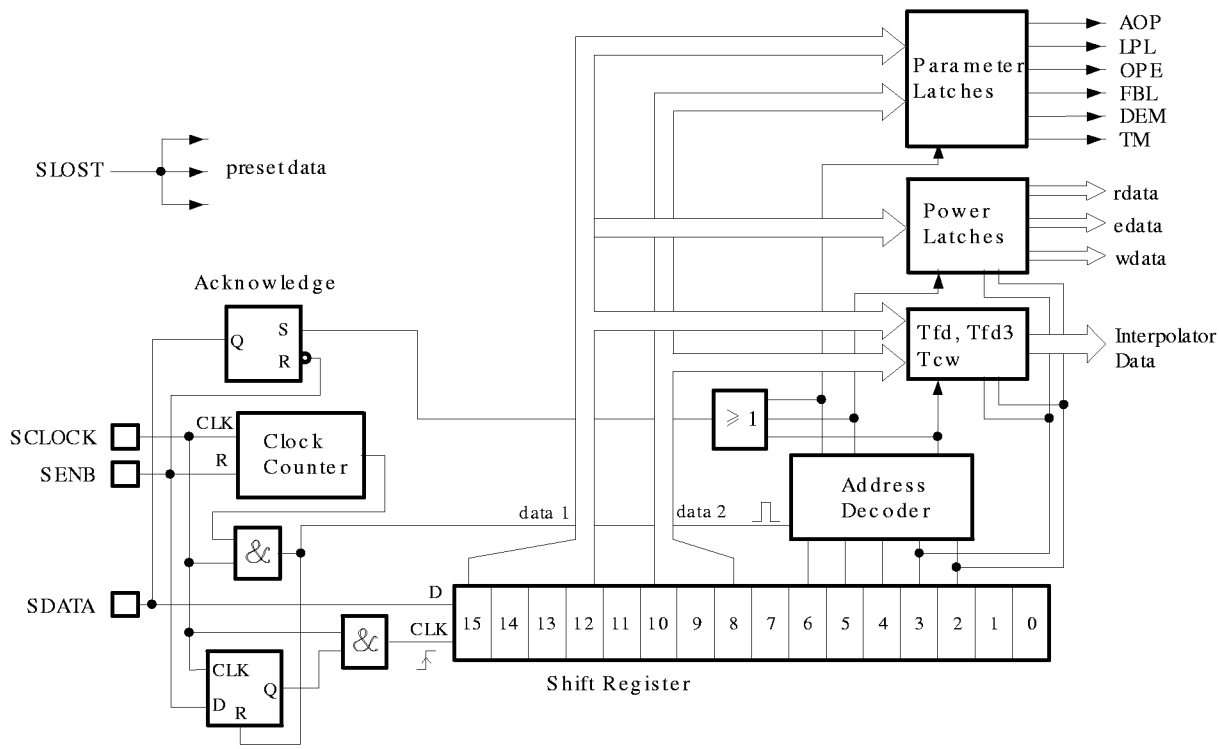


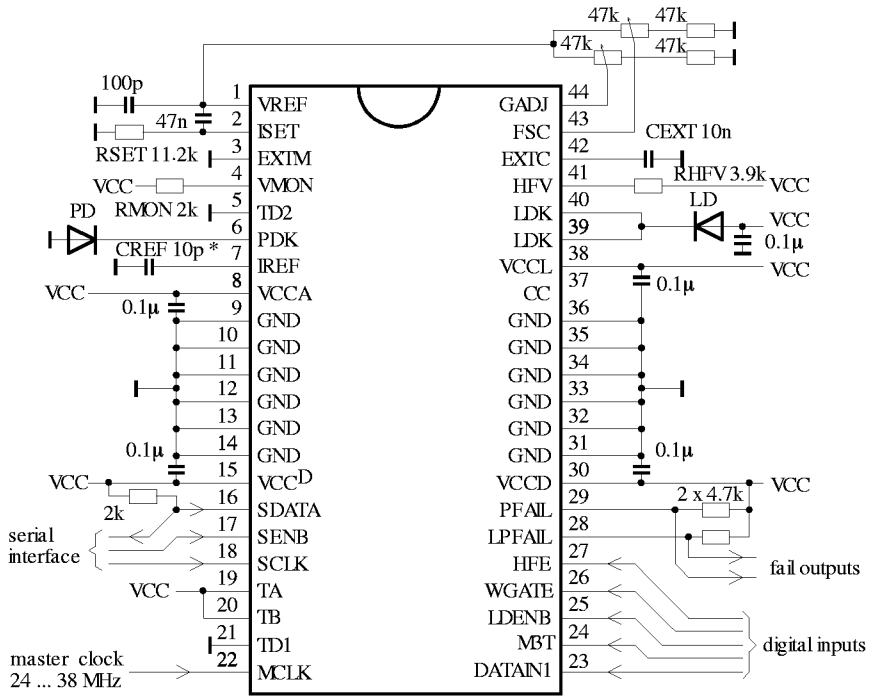
Figure 23. Simplified block diagram of serial interface

Data Assignment Table

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
ACK out	data1				data2				address								data assignment	
				lsb				lsb									data1	data2
L	D	D	D	D	x	x	x	x	x	H	L	L	L	L	x	x	rdata	–
L	D	D	D	D	x	x	x	x	x	H	L	L	L	H	x	x	edata	–
L	D	D	D	D	x	x	x	x	x	H	L	L	H	L	x	x	wdata	–
L	AOP	LPL	OPE	FBL	x	x	DEM	TM	x	H	L	L	H	H	x	x	parameter set	
H	x	x	x	x	x	x	x	x	x	H	L	H	x	x	x	x	not used	
L	x	D	D	D	x	D	D	D	x	H	H	L	L	L	x	x	Tfd	Tcw
L	x	D	D	D	x	x	x	x	x	H	H	L	L	H	x	x	Tfd3	–
H	x	x	x	x	x	x	x	x	x	H	H	L	H	x	x	x	not used	
H	x	x	x	x	x	x	x	x	x	H	H	H	x	x	x	x	not used	
H	x	x	x	x	x	x	x	x	x	L	x	x	x	x	x	x	U8601B not selected	

rdata:	read power data	preset: 9
edata:	erase power data	preset: 9
wdata:	write power data	preset: 9
Tfd:	parameter for start delay of 1st write pulse	preset: 4
Tfd3:	parameter for start delay of 1st write pulse enabled by the M3T flag	preset: 4
Tcw:	parameter for off pulse lengthening	preset: 2

Typical Operating Circuit



*: value of CREF should be approx. corresponding to total capacitance of PD

Figure 24.

Test Circuit (Electrical Feedback)

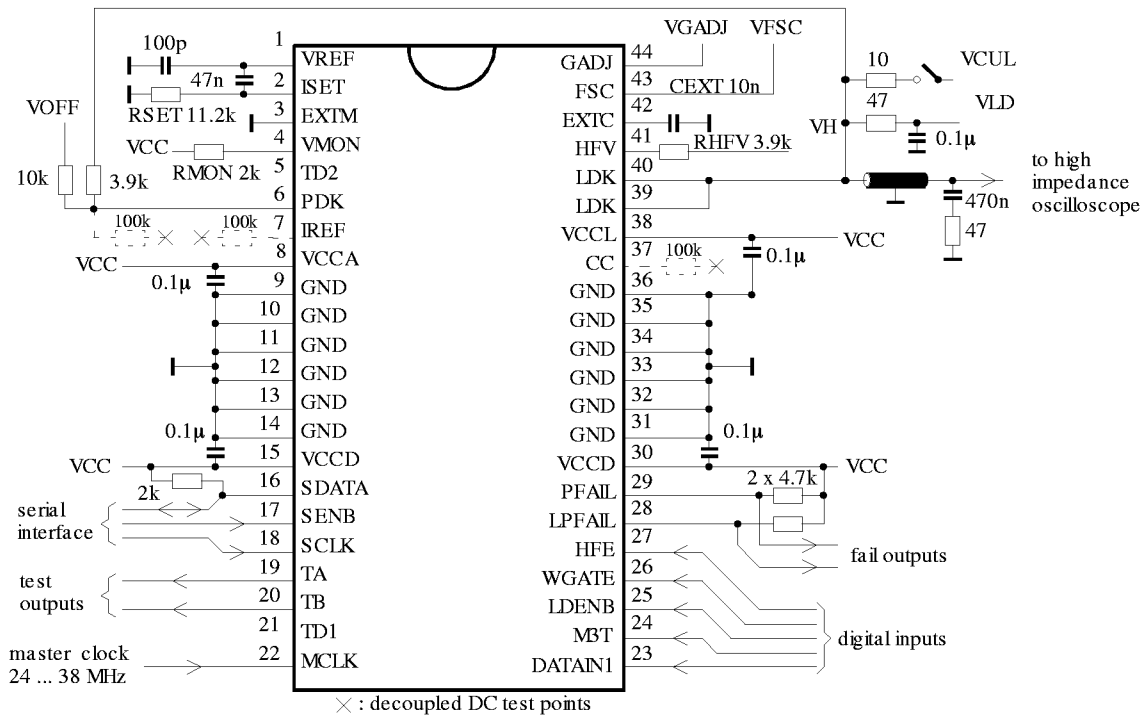
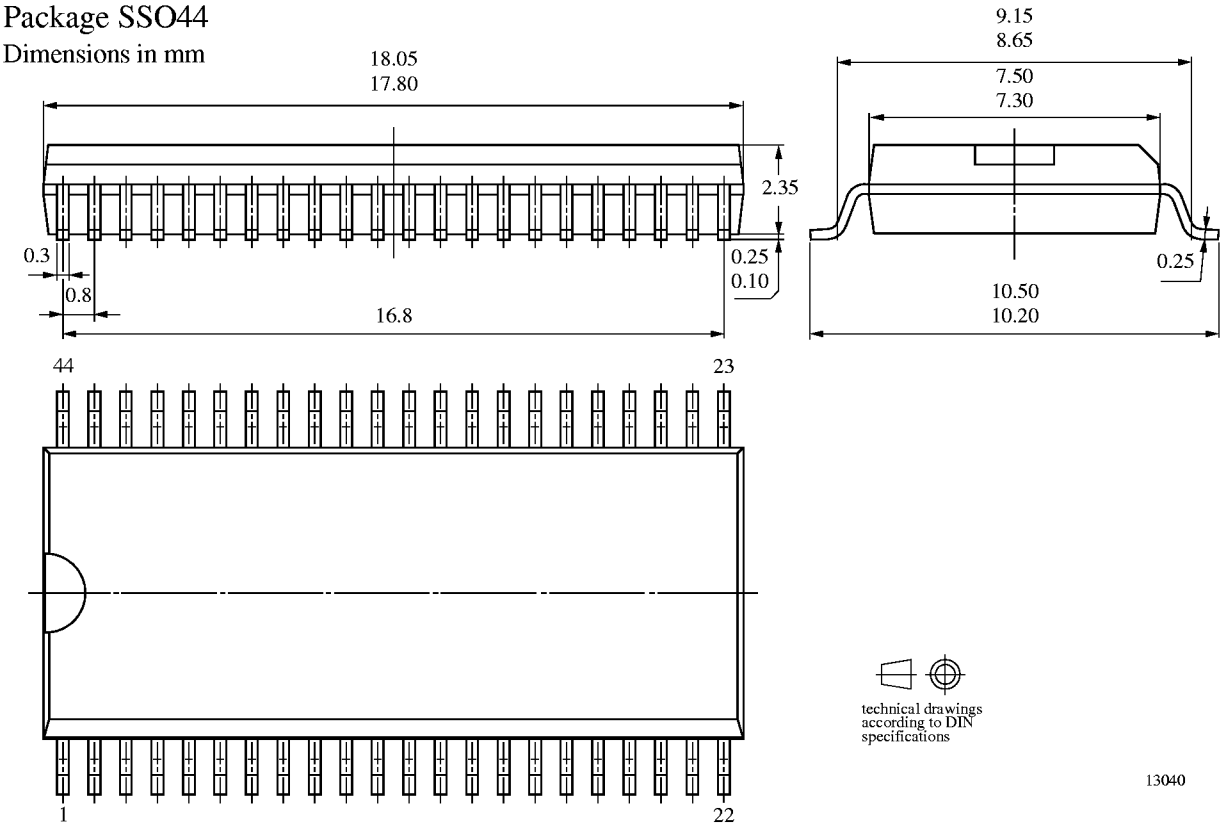


Figure 25.

Package Information

Package SSO44
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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