T3BwP Device
Channelized DS3 Access Solution
TXC-06826

TECHNICAL OVERVIEW

FEATURES

- Complete single-chip channelized DS3 solution
- RISC processor with royalty-free DD-AMPS™ firmware (Drivers, Data link, Alarms, Messaging, Performance/configuration objects, and Signaling)
- Host communication via royalty-free, message-based, POSIX-compatible API
- Integrated 672 x 4,096-channel DS0 cross connect supports grooming, broadcast, off-bus hairpinning, and bonding
- Integrated DS1 cross connect
- 28 DS1 line interfaces or 1 DS3 line interface
- Combination of unframed DS1, transmission DS1, and either MVIP or H.100/H.110 as terminal side interfaces
- Selectable DS3 clear channel functionality
- On-chip maintenance of 15-minute performance objects per IETF RFCs 2495, 2496, and 2494.
- Two DS1 monitor ports for monitoring any DS1 clock and data
- Test Access Port (IEEE 1149.1 boundary scan)
- +3.3 volt input/output leads, +5 volt tolerant
- +3.3 volt and +1.8 volt power supplies
- 456-lead plastic ball grid array package (27 mm x 27 mm)

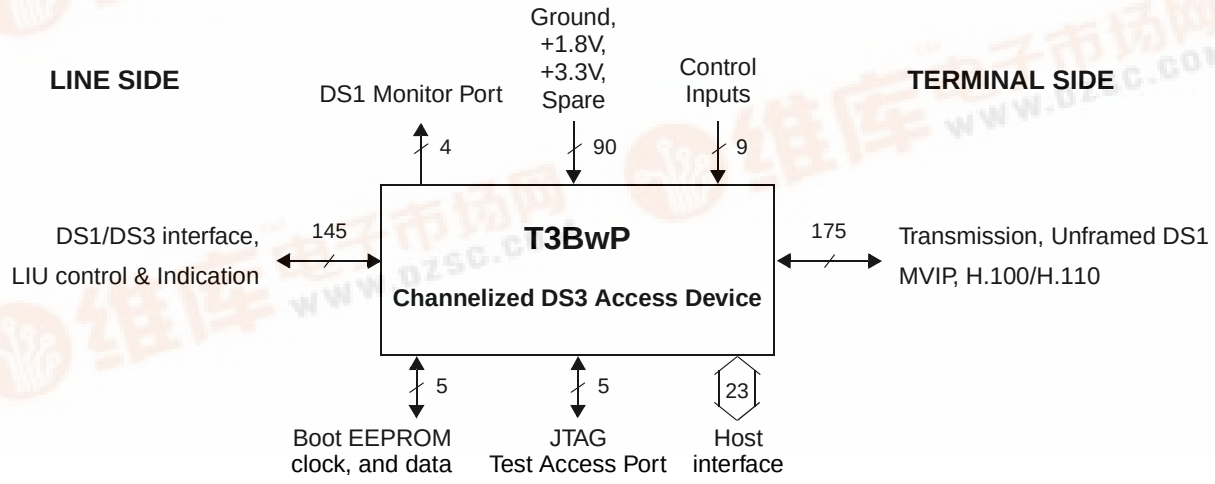
DESCRIPTION

T3BwP™ (TXC-06826) is a RISC processor-based device that supports the requirements of next-generation channelized DS3 access systems. T3BwP integrates an M13 multiplexer, 28 DS1 framers, and a 672 x 4,096-channel DS0 cross connect with an embedded high-performance microprocessor to provide a complete channelized DS3 solution on a single chip. The embedded processor firmware handles device drivers, data links, alarms, messaging, MIB performance objects, and signaling functions and allows communication to an external host via high-level API messages. The firmware is provided by TranSwitch and loaded from an external serial EEPROM at device boot-up.

The T3BwP can be configured to support a variety of modes of operation, which allows for design flexibility. T3BwP supports a combination of unframed DS1, transmission DS1 and H.100/H.110 bus or MVIP interfaces on the terminal side and either DS3 or DS1 on the line side. For TDM applications, all 672 DS0 channels can be switched to any of the 4,096 H.100/H.110 computer telephony (CT) bus channels. The T3BwP can also be enabled to provide DS3 C-bit parity for unchannelized services. The on-chip firmware provides the control and management plane functionality to the host to configure, control and monitor all DS3, DS1, DS0 and digital cross connect functions. The standards-based MIB functionality is provided for network management.

APPLICATIONS

- T-carrier termination equipment: muxes, inverse muxes, cross connects, groomers
- CT (Computer Telephony) network interface boards
- VoP (Voice over Packet/Cell) gateways
- MSADs (Multi-Service Access Devices)
- DSLAMs (Digital Subscriber Loop Access Multiplexers)
- ECUs (Echo Cancellation Units)



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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* Please note that TranSwitch provides documentation for all of its products. Current editions of many documents are available from the Products page of the TranSwitch Web site at www.transwitch.com. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

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OVERVIEW

The T3BwP is a single-chip solution for supporting the requirements of next-generation channelized DS3 access systems. An integrated M13 multiplexer, DS1 framers, DS0 and DS1 cross-connects and a high-performance RISC processor for embedded driver support makes the T3BwP a complete channelized DS3 solution. Communication with the host is accomplished via a high-level message-based API, thereby reducing the software integration effort and providing flexibility to address feature enhancements and standards changes through firmware upgrades.

The flexible T3BwP architecture supports a variety of modes of operation, determined by the upgradeable firmware provided with the device. When used in conjunction with the firmware, T3BwP supports a combination of unframed, transmission DS1 and H.100/H.110 bus or MVIP system interface on the terminal side. The T3BwP line side interface is either fractional DS3, which interfaces directly with a DS3 transmitter/receiver such as the DART (TXC-02030), or DS1 which interfaces directly with a T1 line interface unit for transmission across a cable or an AAL1/2 device such as the COBRA (TXC-05427C).

The integration of the time slot interchange allows for grooming, concentration, switching, and multiplexing making the T3BwP a unique device. The T3BwP can switch any DS1 to any DS1 when configured in unframed, transmission mode. The DS0 cross-connect provides the ability to switch any time slot on any DS1 to any other time slot on any DS1. When configured in MVIP mode, all 672 DS0 channels can be switched to any of the 672 DS0 channels. For TDM applications when in H.100/H.110 mode, all 672 DS0 channels can be switched to any of the 4096 H.100/H.110 computer telephony bus channels. This feature allows for multiple T3BwP devices to be connected to the same H.100/H.110 bus.

FEATURES

The T3BwP device provides the following features:

LINE SIDE DS3 INTERFACE

- M13 block provides all of the functionality found in the TranSwitch M13X device (TXC-03305)
- DART LIU control port
  - Provides control to the TranSwitch DART (TXC-02030) LIU device
- Framing and C-bit support for unchannelized (cell/packet) traffic at 44.210 Mbit/s rate.

28 LINE SIDE DS1 INTERFACES

- Includes Tx and Rx Data (NRZ), Tx and Rx Clock, and Rx BPV.

TERMINAL SIDE INTERFACES AND CROSS CONNECT FUNCTIONALITY

- Integrated DS0 TSI allows for grooming, concentration, multiplexing, internal hairpinning, bonding, broadcast, and switching of any DS0 to any TDM bus (MVIP or H.100/H.110) time slot. A time slot written in frame N is read back out in frame N+1.
- Integrated DS1 cross connect
  - Any line side DS1 may be switched to any terminal side DS1 when configured in unframed mode or transmission mode.
- DS1 terminal port
  - Unframed Mode
  - Transmission Mode:

- Through DS1 cross connect; bypass DS0 TSI
- 1.544 MHz plus 3ms multiframe pulse

- MVIP Mode:
  - Through DS0 TSI
  - 2.048 MHz plus 125 µs frame pulse
- H.100/H.110
  - Through DS0 TSI
  - 8.192 MHz plus 125 µs frame pulse

- Terminal ports can be configured to operate in unframed DS1, transmission DS1, and either H.100/H.110 or MVIP TDM bus modes
- H.100/H.110 operation as bus slave
  - Edge error and frame error detection
  - Bus clock source selection, monitoring, and automatic switching
  - Hardware and software support for hot-swap per PICMG 2.1 R1.0

ON-CHIP RISC PROCESSOR AND FIRMWARE

- RISC processor-based SoC with embedded DD-AMPS (Drivers, Data link, Alarms, Messaging, Performance/configuration objects, and Signaling) firmware
- On-chip maintenance of 15-minute performance objects per IETF RFCs 2495, 2496, and 2494
- Firmware and default configuration loaded via serial EEPROM interface

HOST SOFTWARE

- High-level message-based host API
- Support for standard MIBs
- Source code and portation guide provided by TranSwitch upon request.

GENERAL

- Boundary scan
- +3.3 volt input/output circuit power supply, +1.8V core power supply
- +3.3 volt input/output leads, +5 volt tolerant
- Maximum power dissipation of 1.7 Watt
- 456-lead PBGA (27 mm x 27 mm) package

Maintenance:

- DS3 local loopback and remote line loopback via the TranSwitch DART device
- DS1 remote line and payload loopback and DS1 local loopback
- NxDS0 channel loopback, NxDS0 local loopback
- NxDS0 remote loopback: detect loop-up (Fractional DS1 (2^7 - 1)) / loop-down (Fractional DS1 (2^7 - 1) inverted) sequences; setup/remove NxDS0 channel loopback according to loop-up/loop-down sequences; initiate loop-up/loop-down sequence
- Pseudo-Random Binary Sequence (PRBS) generator and analyzer
  - Two sets of PRBS generators and analyzers for DS1 line: QRSS (2^{20} - 1); 2^{15} - 1

- Two sets of PRBS generators and analyzers for either NxDS0 or DS3: 2^{23} - 1; QRSS (2^{20} - 1); 2^{15} - 1; 2^{11} - 1; 32-bit code word
- Indicator for lock, out of lock,
- OOL counter

The following features are independently selectable for each of the 28 DS1 framers:

Framing Modes:

- D4 SF (Superframe Format)
  - Programmable for Fs, Ft or both frame bits
- ESF (Extended Superframe Format) - FPS bits with or without a valid CRC-6
  - HDLC On-board Controller; 4 kbit/s Data Link
- Unframed (bypass)
- Automatic
  - Framer searches alternatively for SF or ESF; state of search status in automatic and manual modes
- Programmable out of frame control: 2 out of 4, 5, or 6 frame bits

Line Code:

- NRZ: Clock polarity for clock in/out selection; data inversion and clock edge options

Signaling:

- A, AB, 9-state AB signaling for ANSI T.403 ROB applications (SF)
- A, AB, ABCD (ESF)
- Signaling enable/disable on per DS0 basis
- Signaling freeze on per line basis (separate for Tx and Rx directions)
- Signaling freeze on LOS
- Per-DS0 enable with microprocessor read and substitution in both receive and transmit directions for call control and trunk conditioning
- Signaling de-bouncing: Four consecutive signaling states must be equal before a state-change message is sent to the host

Clock Management:

- Use any of three reference clocks: BITS, Local Stratum, or any of twenty-eight recovered DS1 clocks
- Terminal side and line side clocks for receive and transmit are independent

Alarms and Errors:

- Detect and force “yellow” and “blue” (AIS) alarms. Detect RAI-CI and AIS-CI signature.
- Detect Out-Of-Frame, Loss-Of-Signal, Severely-Errored-Frame, Change-Of-Frame-Alignment, Transmit Slips, and Receive Slips
- Detect, count, and force CRC errors (ESF only), frame bit errors, and line code errors (bipolar violations, with or without excessive zeros)
- Detect and force frame slips

Slip Buffer and DS0 Control:

- Separate Tx and RX frame slip buffers, with independent bypass
- Per-DS0 enable (independent receive and transmit) with microprocessor read and substitution in both receive and transmit directions
- Per-DS0 inversion in transmit and receive directions (after slip buffers) in Transmission, H.100/H.110, and MVIP Modes

Performance and Fault Monitoring:

- Framer-based per-DS1 performance monitoring in Rx direction (Transmission, MVIP, and H.100/H.110 Modes)
- Facility Data Link (FDL) HDLC controller
- Shadow registers for all alarms and counters
- Automatic generation and transmission of FDL performance report message for NE and FE maintenance of performance objects per RFC 2495

The following features are selectable for the M13 mux:

DS3 Framing Functions:

- Framing on 4 F-bits in M Subframe
- Framing on 3 M-bits in M Frame
- X-bit read access (Far end SEF/AIS)
- X-bit programmable value (Far end SEF/AIS)
- P-bit parity generating, monitoring, and counting (16-bit)
- C-bit parity or M13 mode selection
- C-bit parity Unchannelized (44.210 Mbit/s clear channel)
- FEAC channel (C3): read access of FEAC word, write access to set loopbacks; FEAC word detection of codes; loopbacks and alarms RAI indication (DS3 and DS1 alarms)
- C-bit access:
    - C1 identification
    - C-bit parity (C7-9) generation, checking, and counting
    - C-bit Path Maintenance Data Link (PMDL) HDLC controller (C13 -15)
    - FEBE generation (on M, F or C parity error), detection, and counting

DS2 Framing Functions:

- Frame alignment on F-bits
- Multiframe alignment on M-bits
- X-bit access

Multiplexing/Demultiplexing Functions:

- 4 DS1s into a DS2 using stuff bit control (DS2 C-bits)
- 7 DS2s into a DS3 using stuff bit controls (DS3 C-bits) or C-bit parity mode
- DS3 into 7 DS2s using stuff bit controls (majority vote DS3 C-bits) or C-bit parity mode
- DS2 into 4 DS1s using stuff bit controls (majority vote DS2 C-bits)

Alarms and Errors:

- Detect and force: DS3 AIS (optional unframed 1010 or 11110), DS3 IDLE (framed 1100), DS3 FEAC alarms (all codes in C-bit parity mode), DS3 RAI, P-bit parity errors, C-bit parity errors, FEBE, and DS2 RAI
- Detect: DS3 Out Of Frame, Loss Of Signal, Severely Errored Frame, and DS2 OOF

Performance and Fault Monitoring:

- Maintenance Data Link HDLC controller
- P-bit and C-bit parity error counter
- Frame bit errors
- Maintenance of performance objects per RFC 2496

MICROPROCESSOR INTERFACE

- 8-bit Motorola or Intel Address/Data buses access mode
- 16-bit Multiplexed Address/Data bus access mode

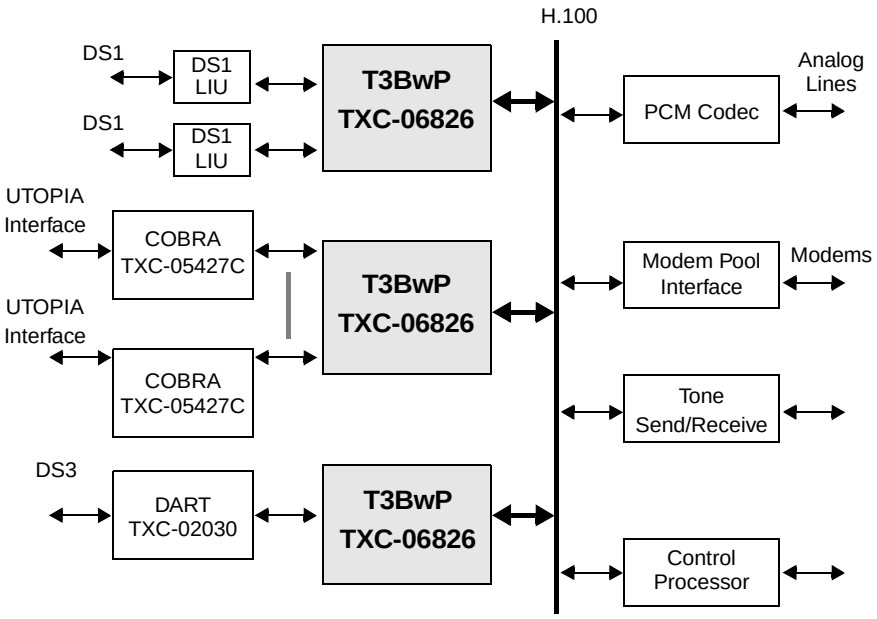
OTHER

- Two DS1 monitor ports
- Ability to tristate all outputs for in-circuit testing
- IEEE 1149.1 boundary scan

APPLICATION EXAMPLES

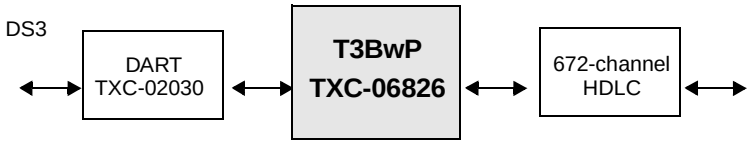
A typical telephony application using the T3BwP is shown in Figure 1.

Figure 1. Telephony Application Using the T3BwP TXC-06826



A DS3 Remote Access Concentrator (RAC) can be implemented using a three-chip solution in conjunction with the T3BwP, as shown in Figure 2.

Figure 2. DS3 RAC Using the T3BwP TXC-06826



INTER-OPERABILITY

T3BwP works directly with the following TranSwitch devices:

- TXC-02030, DART VLSI Device (Advanced E3/DS3 Receiver/Transmitter
- TXC-03103, QTIF-*PLUS* VLSI Device (Quad T1 Framer-*Plus*)
- TXC-03305, M13X VLSI Device (DS3/DS1 Mux/Demux with Enhanced Features)
- TXC-03452B, L3M VLSI Device (Level 3 Mapper)
- TXC-03453, TL3M VLSI Device (Triple Level 3 Mapper)
- TXC-04222, TEMx28 VLSI Device (21/28 Channel Dual Bus High Density Mapper)
- TXC-05150, CDB VLSI Device Cell Delineation Block (CDB)
- TXC-05427C, COBRA VLSI Device (Constant Bit Rate ATM Adaption Layer 1)
- TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator)
- TXC-06103, PHAST-3N VLSI Device (SONET STM-1, STS-3, or STS-3c Overhead Terminator)

DEVICE FUNCTIONAL DESCRIPTION

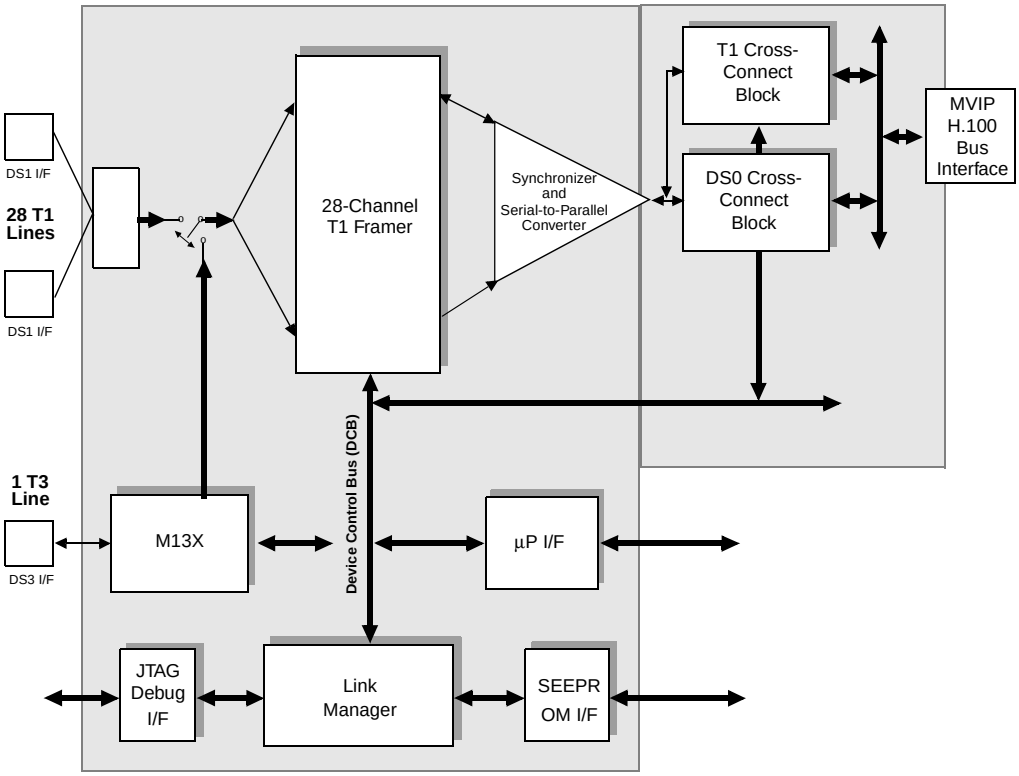
The T3BwP is a complete system-on-chip device that integrates both hardware and software functions. The hardware blocks provide user plane functionality and the resident firmware/software provides parts of the control and management planes. Support for an external management plane is provided via a message interface. The next two sections provide an overview of the hardware and software architectures.

HARDWARE ARCHITECTURE OVERVIEW

The T3BwP provides a DS1 to DS3 multiplexer with a DS3 framer including full C bit functionality (FEAC channel, maintenance data link, parity, etc.), 28 DS1 framers (bypass or SF or ESF framing support including facility data link) with slip buffers and signaling insertion/extraction, a DS1 cross-connect to configure the device for a variety of applications, a full function of DS0 Time Slot Interchange (TSI), and an on-board processor supporting device handling and protocol operations. External interfaces include a serial EEPROM interface for device initial bootup, a local microprocessor bus (8051-like) used to control external devices, two monitor ports to monitor any two DS1s, a control port to control DART, 28 system side framer access ports (supporting MVIP, H.100/H.110 and regular transmission modes), 28 DS1 line-side framer access ports or one DS3 line-side framer access port. For channelized DS3 applications, the DS1 framer line ports are multiplexed/demultiplexed to/from the DS3 line port; the system side DS1 ports may individually be used for direct multiplex access. The DS1 to DS3 multiplexer may be bypassed for direct T1 line access.

The DS1 framer functions are similar to the TranSwitch QT1F-*Plus* device (TXC-03103). Automated features such as Performance Report Message generation and Auto SF/ESF, and software load reduction features such as Trunk Conditioning, deep FDL slip buffers, one second shadow registers and interrupt on signaling change of state are accomplished by the core processor. Framing is provided to and from the T1 line ports or the DS1 to DS3 multiplexer/demultiplexer. Alarm detection/generation, signaling access/insertion/extraction, slip buffering, facility data link (FDL) support and diagnostic support using loopbacks/PRBS generator/analyzer, etc. are provided. The system side supports MVIP/ H.100/ H.110 and transmission modes with clock, frame, data and signaling leads; (common clock and frame signals are provided in MVIP and H.100/H.110 modes). Nx64k DS0 support is provided, in bulk for an entire DS1. For direct T1 line access, a rail interface is not provided (DS1 line port will only operate in NRZ mode). A local microprocessor bus (8051-like) is provided to control external devices such as quad LIUs. The control of the DART is fully supported when a DS3 interface is used in place of the DS1 interfaces. Figure 3 provides a block diagram for the T3BwP device. The main blocks shown are: M13X, QT1F-*Plus*, Serial-to-Parallel converter, DS1/DS0 cross-connect, and high performance processor. In terms of interfaces: 1 DS3, 28 DS1, System Interface (H.100/MVIP), Microprocessor, Serial EEPROM, and JTAG (Test Access Port) are supported.

Figure 3. T3BwP TXC-06826 Block Diagram



The DS3 framer and multiplexer functions are similar to the TranSwitch M13X device (TXC-03305). The DS3 framer provides framing (M frame and M sub-frame) with AIS and LOS detection in addition to DS3 loopbacks and access to the C bits with processing of the FEAC channel (C3), the maintenance data link (full duplex HDLC controller over C13, C14 and C15) and FEBE (C10, C11 and C12). In addition, DS3 X bit access, loss of signal, loss of frame, AIS, idle, C bit parity (C7, C8 and C9) and P bit parity are detected and generated. This block can operate in the M13 mode as well where the 21 C bits are used for stuff control of the 7 DS2s. DS2 framing (7 instances) is provided either all at a fixed rate (C bit parity mode at 6306.2723 kb/s) or M13 mode. Each DS2 framer and multiplexer handles four DS1 signals. DS1 loss of signal is provided as well as DS1 loop backs under control of the FEAC channel, the DS2 stuff control bits (C bits) or register control. The DS1 signals are multiplexed directly from the DS1 framer blocks. The DS1 signals are demultiplexed and fed to the DS1 framer blocks via a dejitter buffer or with demultiplexing jitter, depending on application.

The Link Manager processor performs control and management functions which are grouped as follows:

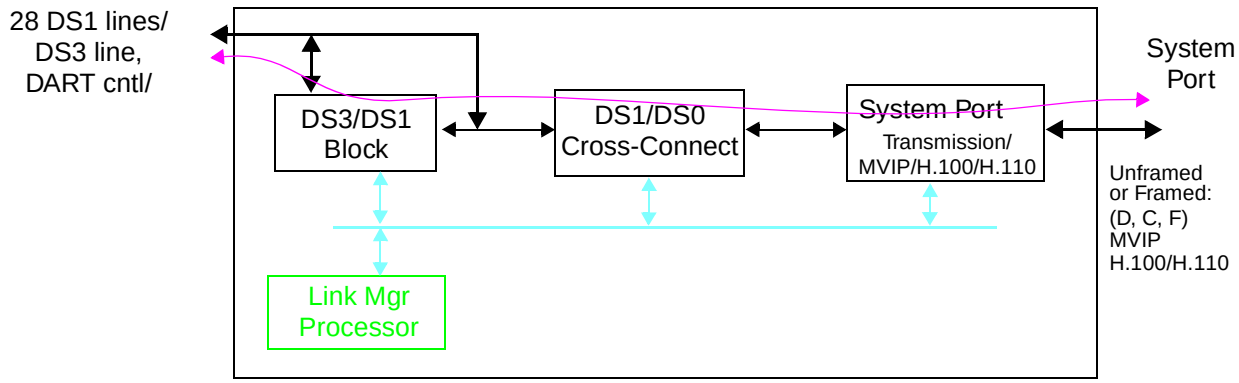
1. Interface with the host using priority-based message queues
2. Device initialization, configuration and control
3. Alarm detection and propagation, as applicable
4. Far end alarm generation (through FEAC channel /X-bits, FDL/ payload bit)
5. Performance monitoring of near end and far end at DS1 and DS3 rates
6. Performance reporting to near and far end (e.g., DS1 PRMs in ESF mode), DS3 FEBE in C-bit parity mode)
7. Execution of maintenance and diagnostic requests from host or far end (e.g., loopbacks)

The device also provides a DS1 monitor function that can be used to monitor any two of the 28 DS1s (either Tx or Rx) via two monitor ports when operating in DS3 mode. Two DS1 reference clock outputs are provided to support a common reference clock source. IEEE 1149.1 Boundary Scan is sorted for BYPASS, IDCODE, EXTEST and SAMPLE/PRELOAD.

Traffic Flow

On the line side, the T3BwP provides the interface to one DS3 line or twenty-eight DS1 lines. The T3BwP contains 28 DS1 framers, a DS3 framer, and a variety of configurable multiplexer functions. On the system side, each DS1 system port can be configured to operate in different modes of unframed, transmission, and either MVIP or H.100/H.110 modes. Figure 4 shows the TDM traffic flow through the T3BwP device.

Figure 4. T3BwP TDM Traffic Path



FIRMWARE/SOFTWARE ARCHITECTURE OVERVIEW

Figure 5 shows the connectivity model for the T3BwP device. The device contains a high performance processor that is responsible for interacting, controlling, and initializing the “cores” inside the T3BwP. The microprocessor controls the following core blocks:

1. M13X block: this block provides the means to multiplex 28 DS1 channels into a DS3 channel and demultiplex DS3 data into its 28 DS1 channels. The block is managed with the appropriate device driver that runs in the on-chip processor LMPro.
2. Quad Framer block: this block provides the framing for up to 28 DS1 lines. Similarly as in the DS3 case, the on-chip processor LMPro runs the device driver that controls the DS1 links.
3. Cross connect block: two levels of cross connect are available. The first is a DS1 cross connect which can connect any input DS1 to any output DS1. The second is a DS0 cross connect that can connect any DS0 to any DS0.

In addition to running device drivers to control the "cores", the microprocessor is responsible for managing the interface layer between the device drivers and the external message interface. This message interface provides the connectivity from specific user function calls (via the mailbox) to the T3BwP device and the device register manipulation and interaction with the host (via the mailbox). The modules provided are:

1. Facility Manager: this module performs the function of generating and processing messages to and from the host and invoking the associated driver modules and routines.

2. Platform Module: this module absorbs all the hardware interface details along with any OS specific details.

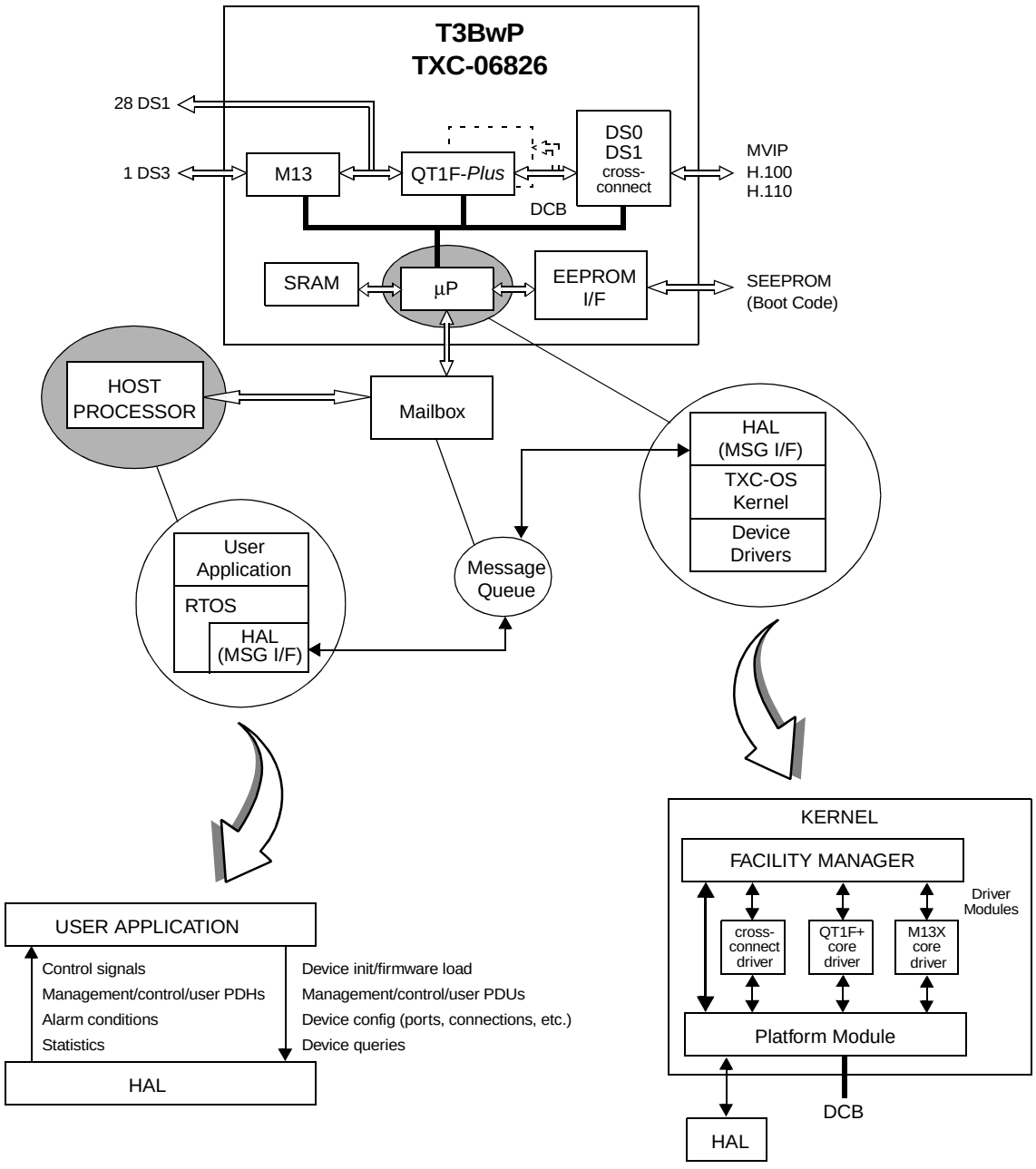
As referred to previously, the mechanism for message passing is provided by a shared media device. The interface is a set of FIFOs that can be accessed by both the host processor and T3BwP's on-chip processor.

Provided with the T3BwP device is the "device driver library" that provides the hardware abstraction layer between the host application software and the T3BwP device. The definition of the hardware abstraction layer (message-based API interface) is provided in the API Firmware Reference Guide for T3BwP.

DEVICE CONFIGURATION

The mechanism to load code into the instruction RAM for the on-chip processor requires the storage of the code into non-volatile external memory. The external memory is accessed serially and the code is loaded into the processor instruction RAM. The external EEPROM will hold an image for the entire instruction RAM.

Figure 5. Software and Hardware Interaction for T3BwP



SELECTED PARAMETER VALUES

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Core Supply Voltage, +1.8V nominal	V_{DD-INT}	-0.3	2.1	V	Notes 1, 4
I/O Supply Voltage, +3.3V nominal	V_{DD-IO}	-0.3	3.9		Notes 1, 4
DC input voltage	V_{IN}	-0.5	5.5	V	Notes 1, 4
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min linear airflow. Note 1
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative humidity, during assembly	RH	30	60	%	Note 2
Relative humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3
Latch-up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.
4. Device core is 1.8V only. All input signal leads accept 5V signals.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient			20	° C/W	0 ft/min linear airflow

POWER REQUIREMENTS

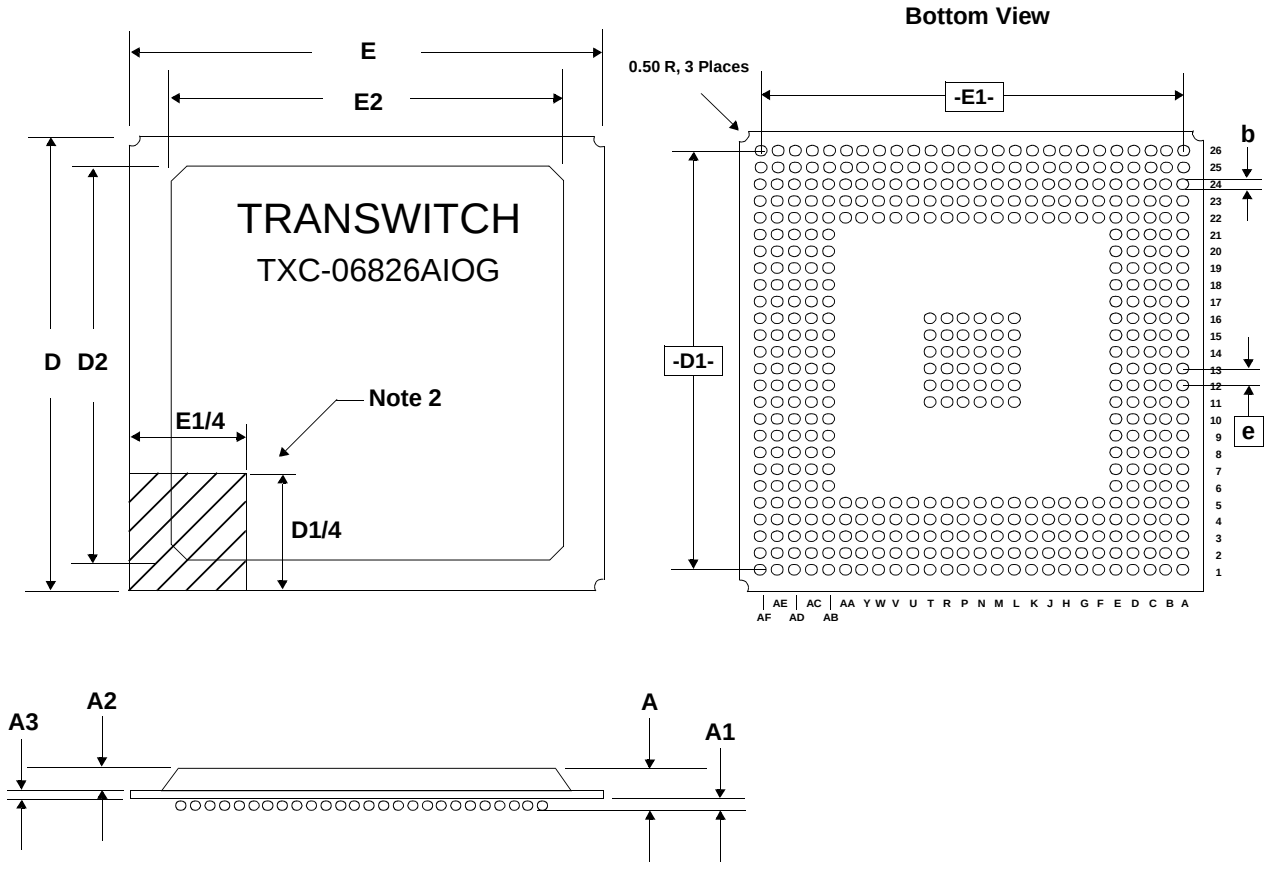
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD-IO}	3.15	3.3	3.45	V	
I_{DD-IO}		210	350	mA	See Notes 1 and 2
P_{DD-IO}		0.7	1.2	W	See Notes 1 and 2
V_{DD-INT}	1.71	1.8	1.89	V	
I_{DD-INT}		170	280	mA	See Notes 1 and 2
P_{DD-INT}		0.3	0.5	W	See Notes 1 and 2
$P_{DD-TOTAL}$		1.0	1.7	W	

Notes:

1. Typical values are based on measurements made with nominal voltages at 25° C.
2. All I_{DD} and P_{DD} values are dependent upon V_{DD}.

PACKAGE INFORMATION

The T3BwP device is packaged in a 456-lead plastic ball grid array package suitable for surface mounting.



Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.

Dimension (Note 1)	Min	Max
A (Nom)	2.23	
A1	0.40	0.60
A2 (Nom)	1.12	1.22
A3 (Nom)	0.56	
b (Ref.)	0.63	
D	27.00	
D1 (Nom)	25.00	
D2	23.95	24.70
E	27.00	
E1 (Nom)	25.00	
E2	23.95	24.70
e (Ref.)	1.00	

Figure 6. T3BwP TXC-06826 456-Lead Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number: TXC-06826AIOG 456-Lead Plastic Ball Grid Array Package

RELATED PRODUCTS

TXC-02030, DART VLSI Device (Advanced E3/DS3 Receiver/Transmitter). DART performs the transmit and receive line interface functions required for transmission of E3 (34.368 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-03103, QT1F-*Plus* VLSI Device (Quad T1 Framer-*Plus*). A 4-channel framer for voice and data applications. This device handles all logical interfacing functionality to a T1 line. This device requires a 5.0 volt supply. The new TXC-03103C device provides the same functionality but can operate either from a 5 volt supply or from a 3.3 volt supply at lower power dissipation.

TXC-03305, M13X VLSI Device (DS3/DS1 Mux/Demux with Enhanced Features). This single-chip device provides the functions needed to multiplex and demultiplex 28 independent DS1 signals to and from a DS3 signal with either an M13 or C-bit frame format. It includes some enhanced features relative to the M13E TXC-03303 device.

TXC-03452B, L3M VLSI Device (Level 3 Mapper). The L3M maps a DS3 line signal into a STM-1 TUG-3 or STS-3/STS-1 SPE or STS-1 SPE SDH/SONET Signal.

TXC-03453, TL3M VLSI Device (Triple Level 3 Mapper). Maps three 44.736 Mbit/s DS3 to an STM-1, TUG-3 or STS-3 STS-1 SPE SDH/SONET signal. An 34.368 Mbit/s E3 signal is mapped in to an STM-1 TUG-3. The TL3M's SDH/SONET interface format is COMBUS, byte wide parallel. The TL3M supports drop bus and add bus SDH/SONET timing modes. Drop bus timing provides timing signals for the add side while timing for both busses is independent for the add bus timing mode.

TXC-04222, TEMx28 VLSI Device (21/28 Channel Dual Bus High Density Mapper). An add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Up to 28 E1, DS1, or VT/TU payloads are mapped to and from VT1.5/TU-11s and VT2/TU-12s carried in an STM-1 VC-4 or STS-3 format.

TXC-05150, CDB VLSI Device Cell Delineation Block (CDB). This device provides cell delineation for ATM cells carried in a physical line at rates of 1.544 Mbit/s to 155.52 Mbit/s.

TXC-05427C, COBRA VLSI Device (Constant Bit Rate ATM Adaptation Layer 1). Provides ATM AAL1 Structured and Unstructured service for four DS1, E1 or n x 64k constant bit rate interfaces.

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device provides SONET STS-1 overhead termination with section, line and path overhead processing.

TXC-06103, PHAST-3N VLSI Device (SONET STM-1, STS-3 or STS-3c Overhead Terminator). This PHAST-3N VLSI device provides a Telecom Bus interface for downstream devices. It operates from a power supply of 3.3 volts.

REFERENCE DOCUMENTS

- ANSI T1.102 -1995, Digital Hierarchy - Electrical Interfaces.
- ANSI T1.107 -1995, Digital Hierarchy - Format Specifications.
- ANSI T1.231 -1997, Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring
- ANSI T1.403 -CORE 1998, Network and Customer Installation Interfaces - DS1 Electrical Interface
- ANSI T1.404 -1994, Network-to-Customer Installation- DS3 Metallic Interface Specification.
- AT&T PUB 62411, Accunet T1.5 Service Description and Interface Specification.
- AT&T PUB 54016, Requirements for Interfacing Digital Terminal Equipment To Services Employing the Extended Superframe Format, Sept. 1989.
- GR-499-CORE, Transport Systems Generic Requirements (TSGR): Common Requirements, (Issue 1, Dec. 1995)
- IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture, May 1990.
- MVIP, H-MVIP Multi-Vendor Integration Protocol. Working Document, April 1995.
- Enterprise Computer Telephony Forum, H.100 Rev. 1.0 Hardware Compatibility Spec. CT Bus
- ITU-T G.711 Pulse Code Modulation (PCM) of Voice Frequencies, 1972
- ITU-T O.151 Error Performance Measuring Equipment Operating at the Primary Rate and Above. 10/92

- NOTES -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