PHAST-3P Device
STM-1/STS-3c SDH/SONET Overhead Terminator with CDB/PPP UTOPIA Interface
TXC-06203

TECHNICAL OVERVIEW

FEATURES

- ATM cells over SDH/SONET
  - ATM cell delineation
  - Single-bit error correction and multiple-bit error detection
  - ATM Scrambler/descrambler option ($x^{43}+1$)
  - Idle cell discard/Cell filtering (GFC, PTI and CLP fields)
  - Four-cell receive and transmit FIFOs
  - Rate adaptation using idle cells
  - HEC generator with optional COSET addition
- PPP (IP packets) over SDH/SONET
  - Octet stuffing/destuffing
  - PPP Scrambler/descrambler option ($x^{43}+1$)
  - Data inversion option, Invalid frame detection
  - Short frame and programmable long frame detection
  - CRC-16 or CRC-32 detection/generation/pass-through option
  - 256-byte receive and transmit FIFOs
- Bit-serial P-ECL SDH/SONET line interface
- Byte-parallel SDH/SONET line interface
- Section, line and path overhead byte processing
- Receive pointer tracking and false pointer detection
- RAM access to section, line and path overhead bytes
- Section, line and path overhead byte insertion sources:
  - RAM, interfaces, ring (mate device) or receive side
- Supports 1+1 or 1:N APS applications
- Interfaces:
  - TOH bytes with programmable byte marker pulse
  - K1/K2 APS bytes
  - Section data communications (D1-D3) bytes
  - Line data communications (D4-D12) bytes
  - POH bytes (VC-4 or each STS-1)
  - Alarm Indication Port (AIP) for line/path ring operation
- Terminal side 8-bit or 16-bit UTOPIA level 2 interface (with additional signals for PPP)
  - Single-PHY or Multi-PHY
- Intel-compatible or Motorola-compatible microprocessor interface
- Boundary scan and line loopback
- Single +3.3 volt, ±5% power supply; 5 volt input signal tolerance
- 256-lead plastic ball grid array package
- Device driver:
  - Insulates application from register access details
  - Driver APIs configure and manage the PHAST-3P device
  - Default configurations are provided within the driver
  - One command configures all the control registers
  - Driver can download the firmware code into PHAST-3P
  - Similar architecture to other TXC drivers, such as the ML3M

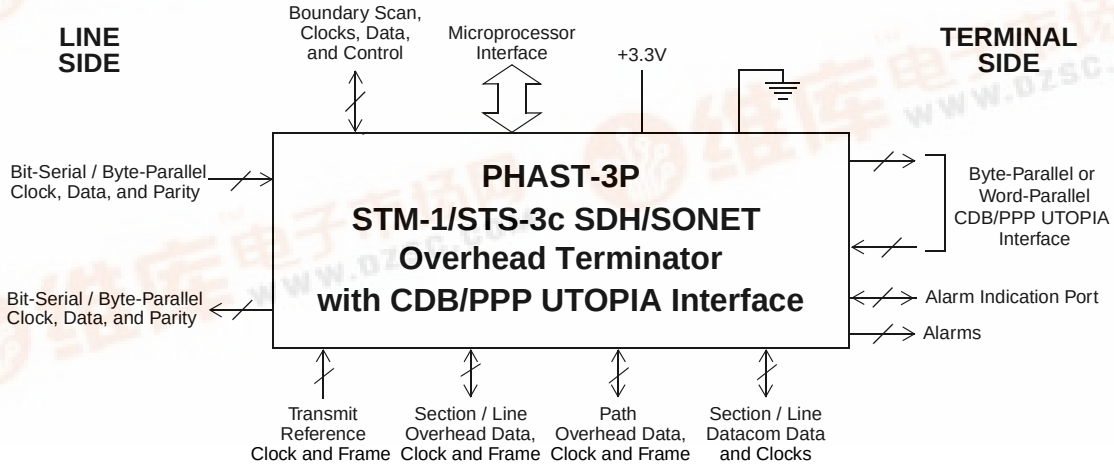
DESCRIPTION

The TranSwitch PHAST-3P (TXC-06203) is an STM-1/STS-3c section, line and path overhead termination device that performs ATM and PPP PHY-layer processing. It provides either a SDH/SONET pseudo-ECL bit-serial interface or a byte-wide parallel interface on the line side. The serial interface provides 155 MHz clock recovery and clock synthesis, and the section and line overhead bytes in the data are processed. The PHAST-3P performs pointer tracking and POH byte processing. TOH (RSOH and MSOH) and POH bytes are provided in RAM for microprocessor access or via TOH and POH interfaces. The POH bytes can be inserted from RAM, the serial POH interface, or a mate PHAST-3P device for line and path ring applications. The terminal interface is UTOPIA level 2 for ATM cells or level 2P for packets. UTOPIA bus width can be 8-bit or 16-bit, Single-PHY and Multi-PHY operation are supported.

For testing, the PHAST-3P provides boundary scan, B2 and B3 BER measurements, programmable BIP error mask generation, and line loopback. The device provides either Intel or Motorola microprocessor access. Performance counters can be configured to be saturating or roll-over. The interrupts, with mask bits, can be programmed for positive, negative, or positive/negative alarm transitions or positive levels. A software polling register is also provided. A fully functional Device Driver is available through TranSwitch Applications Engineering.

APPLICATIONS

- Add/drop multiplexers
- Data communications systems
- ATM switches
- Routers
- Communications gateways



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* Please note that TranSwitch provides documentation for all of its products. Most product documentation is available from the TranSwitch Internet Web site at www.transwitch.com. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product

LIST OF FIGURES

OVERVIEW

The PHAST-3P provides section, line, and path overhead byte termination for an SDH STM-1 AU-4 or SONET STS-3c format, which is carrying either ATM cells (CDB operation) or IP packets (PPP operation). Upstream access to the PHAST-3P is provided by either a bit-serial 155.52 MHz pseudo-ECL interface or a 19.44 MHz byte-parallel interface. The serial interface is equipped with an optional 155.52 MHz Clock Recovery block. The frame pulse for the receive parallel interface is optional. In addition, an external fail signal input lead is provided on the receive side for an upstream loss of signal and/or loss of frame indication. Two external scan and drive leads are also provided. These leads are used to input up two external alarms and for the control of external circuitry by the microprocessor.

The PHAST-3P provides TOH byte processing including descrambling/scrambling, B1 parity checking, a single-bit or a 16-byte trail trace J0 comparison, S1 byte change in synchronization recovery and detection, and line AIS or line RDI detection and recovery, as well as a B2 BER measurement. The TOH bytes are written into RAM locations for microprocessor read access. In addition, the TOH bytes are provided at a TOH interface for access by external circuitry. This interface has a programmable marker pulse which will identify the location of a selected byte (e.g., F1). Separate interfaces are provided for accessing and inserting the APS bytes (K1 and K2), the order wire bytes (E1 and E2 separately), and the section (D1 through D3) and line (D4 through D12) data communication bytes.

The PHAST-3P provides pointer tracking for the STM-1 AU-4 and STS-3c formats. The pointer tracking state machine has been implemented based on the requirements found in ETSI and ANSI documents. In addition, the value of the size bits, including an option for bypassing the use of the size bits, is programmable. A false concatenation detector is also provided (STM-1 versus STS-3 format). Beside AIS, LOP, and NDF detectors, counters are provided for pointer increments and decrements.

The POH bytes are written into RAM locations for microprocessor read access. In addition, the POH bytes are provided at a POH interface for external access. POH byte processing includes J1 16-byte trail trace message processing (or storage of 64-byte messages in RAM synchronous to the CR/LF characters), B3 parity check (with a BER measurement), C2 mismatch and unequipped processing, and G1 processing (REI counter, old and new RDI).

The PHAST-3P provides two types of payload mappings: CDB over SDH/SONET and PPP over SDH/SONET. In the receive direction, the CDB function includes a CDB delineation function along with an optional scrambler. Other features include cell filtering with individual header fields which are maskable and idle cell discard. The receive FIFO is four cells deep with auto and manual reset capability. A Single-PHY or Multi-PHY UTOPIA interface is provided for the receive and transmit directions. The Single-PHY interface supports both octet and cell handshake. The interface can be programmed to be either 8 bits wide or 16 bits wide. A 16-bit bus is recommended for Multi-PHY operation. Odd or even parity generation and checking for data only is also provided. In the transmit direction, the depth of the transmit FIFO can be programmed. Other features in the transmit direction include an idle cell generator with programmable header fields and payload.

For PPP over SDH/SONET mappings, the PHAST-3P provides optional data stream inversion, transparent operation, and an HDLC controller. The HDLC controller provides octet stuffing/destuffing, CRC-16 or CRC-32 generation and checking, CRC pass-through, long and short frame checking, invalid frame generation and checking, and flag fill character generation. The receive and transmit FIFOs are 256 bytes deep, with auto or manual resets on alarm conditions. In addition, depth indication is provided. The interface is a modified Single-PHY or Multi-PHY interface. An option is provided to control the number of bytes transferred. The PHAST-3P also provides an optional scrambler/descrambler prior to the SDH/SONET mapping.

The POH bytes can be inserted into the SPE from a POH interface, from RAM locations that contain microprocessor-written values, or from the local receive side (e.g., line RDI) of the PHAST-3P. The TOH bytes can be inserted into the STM-1/STS-3c format from TOH interfaces, RAM locations that contain microprocessor-written values, or the local receive side (e.g., line RDI).

The PHAST-3P memory map is 8-bit register-based and will function with either Intel or Motorola split bus microprocessors. In addition to a software polling register, latched and unlatched alarm positions are provided. The latched alarm positions can be programmed to occur on positive, negative, or positive and negative alarm transitions, or the positive level of an alarm. Activation of the hardware interrupt by alarms is optional, with individual interrupt mask bits provided for the latched alarms. Performance counters can be programmed globally to be either saturating (stopping at their maximum count), or roll-over. An optional interrupt is provided to indicate when the maximum count is reached in the saturating mode.

The PHAST-3P is equipped with two internal processors, one for the receive side and the other for the transmit side. The purpose of the internal processors is to perform many of the TOH (RSOH and MSOH)/POH processes. For example, controlling the alarms that will generate path RDI, and implementing the J1 trail trace message comparisons.

PHAST-3P testing features include line loopback. In addition, a BIP-n error mask capability with programmable length is also provided. Other test features include boundary scan capability and the ability to force all output leads to the high impedance (High-Z) state.

The PHAST-3P software driver has the same architecture of the other TranSwitch device drivers such as the ML3M software, and is meant to be easily integrated with them. The application software calls the driver functions to configure, control and manage the PHAST-3P device. The device driver insulates the application from the internal details of the device register usage and provides a higher level of abstraction. Particularly powerful are the default configurations provided within the driver that allow one single command to bring the device to operational mode. The device driver will also take care of downloading the Firmware code into PHAST-3P.

FEATURES

The following is a list of features supported by the PHAST-3P:

General Features

- Line Side Interfaces:
  - Pseudo-ECL serial interface
    - Clock recovery and synthesis with bypass options
    - Transmit clock and data out, receive data in, with optional clock in
    - Loss of Clock (LOC) detection (Stuck high or low)
    - ETSI or ANSI Loss Of Signal (LOS) detection
    - Receive 8 kHz clock output reference
    - Receive 19.44 MHz clock output reference
  - Byte-parallel interface
    - Data byte, clock, parity, and optional frame pulse
    - Programmable parity: even or odd, and data-only or data and framing
    - Loss of Clock detection
    - Receive 8 kHz clock reference
    - Receive 19.44 MHz clock output reference
- Receive and Transmit
  - External scan and drive leads (two each)
  - External line fail input lead
- Transport Overhead Byte Processing
  - Out Of Frame (OOF) and Loss Of Frame (LOF) detection
  - Descrambling option
  - J0 (C1) byte trail trace
    - Single-byte comparison - ANSI
    - 16-byte message comparison - ETSI
    - Disable option
  - B2 parity check
    - BER Measurement (10^{-3} to 10^{-7} with burst error protection)
    - 16-bit performance counter with bit or block count option
  - Line REI
    - 16-bit performance counter with bit or block count option
  - K1 and K2 Bytes
    - APS byte failure alarm detection
    - Change in APS byte status
    - Line RDI (FERF) detection
    - Line AIS detection
    - Debounced K1 and K2 bytes
  - S1 byte
    - Change in value indication (for bits 5, 6, and 7)
  - All TOH bytes are written in RAM for microprocessor access
- Receive TOH Interfaces
  - TOH interface plus programmable byte marker

- Markers for J0, D1-D3, D4-D12, E1, E2, K1/K2, and F1 bytes
- APS Interface (K1 and K2 bytes)
- E1 order wire Interface
- E2 order wire Interface
- Section data communication interface (D1 - D3 bytes)
- Line data communication interface (D4 - D12 bytes)

- Receive Pointer Tracking
  - ETSI compliant
  - Size bit check (00, 10, 01, 11, or bypassed)
  - False concatenation check
  - AIS-LOP transition bypass option
  - LOP, AIS and new NDF alarms
  - Increment and decrement counters (8-bit counters)
- Receive Path Overhead Byte Processing (STM-1/STS-3c)
  - Receive POH interface
  - All POH bytes written in RAM for microprocessor access
  - J1 Byte
    - 16-byte trail trace message comparison
    - 64-byte RAM storage with CR/LF alignment
    - Disable detection
  - B3 BIP check
    - 16-bit performance counters with bit/block count option (B3 errors)
    - B3 BER measurement (10^{-3} to 10^{-7} with burst error protection)
  - C2 byte
    - Mismatch Detection
    - Unequipped Detection
  - G1 byte
    - REI, bit or block count option
    - Single-bit or three-bit RDI detection
  - H4 byte
    - Not processed
  - K3 byte
    - Debounced value provided
  - N1 byte
    - Not processed
- Path AIS Generator
  - Enable feature bit
    - Microprocessor control
- Transmit POH Byte Insertion Source
  - RAM locations
  - POH Interface
  - Local receive side (e.g., RDI and REI)
- Transmit POH Byte Internal Processing
  - J1 byte

- 16-byte or 64-byte option via RAM
- POH interface
- B3 parity calculation
  - Programmable error mask
- C2 byte
  - Transmit selected value (e.g., microprocessor or POH interface)
- G1 byte
  - REI
  - RDI, single-bit or three-bit RDI with microprocessor control
  - Bit 8 control
  - RAM or POH interface option
  - Test mode
- H4 byte
  - RAM value or POH interface
- F2, F3 and K3 bytes
  - RAM or POH interface
- N1 (Z5) byte
  - RAM or POH interface

- Transmit Timing
  - Fixed to 522 decimal value
- Transmit Pointer Generation
  - Size bit value is programmable
  - ss bits in Y byte are programmable
- Unequipped Status Generation
  - VC-4 with supervisory option
- Transmit TOH Byte Insertion Sources
  - Programmable selection, RAM or interfaces
  - Transmit TOH interfaces
    - TOH interface plus programmable byte marker
    - Markers for J0, D1-D3, D4-D12, E1, E2, K1/K2, and F1 bytes
    - APS interface (K1 and K2 bytes)
    - E1 order wire interface
    - E2 order wire interface
    - Section data communication interface (D1 - D3 bytes)
    - Transmit line AIS
- Testing
  - Boundary scan
  - BIP error masks with programmable errors
  - Line loopback
  - High-Z all output leads (except the P-ECL output leads)
- Microprocessor
  - Split bus, Intel or Motorola interface
  - Interrupt is edge and level programmable for activation by alarm bits
  - Global polling register
- Performance counters are optionally roll-over or saturating (with interrupt)

CDB Features

- Receive CDB Features
  - CDB delineation
    - LCD, uncorrectable HEC error, correctable HEC error
    - Single-bit error correction or multiple-bit error detection in SYNC state
      - Cell acceptance: 1, 2, 4, or 8 cells
    - Performance counters
      - Receive cell count (16-bit counter)
      - Correctable HEC error count (8-bit counter)
      - Uncorrectable HEC error count (8-bit counter)
        - with optional cell pass-through
    - Descrambling option
    - Idle cell discard (GTC, PTI, CLP fields equal to 0000 0001)
    - Cell filtering
      - GTC, PTI and CLP fields
      - Individual mask bits
      - Cell discard
  - HUNT state on SDH/SONET alarms
    - Alarm option
    - Enable control bits for individual alarms
    - Microprocessor control
  - Receive FIFO
    - Four cells (53 bytes each)
    - Overflow alarm indication
    - Microprocessor reset and auto reset
- Receive Terminal Side UTOPIA Interface
  - Single-PHY (cell or octet) or Multi-PHY
    - Parity generation, even or odd over data
    - 8-bit bus with 16-bit bus option
- Transmit Terminal Side UTOPIA Interface
  - Single-PHY (cell or octet) or Multi-PHY
    - Parity check, odd or even
- Transmit CDB Features
  - Transmit FIFO
    - Four cells with programmable depth (2, 3, or 4 cells)
    - FIFO overflow alarm
    - Depth alarm (first cell read, reset on two empty cells)
    - Microprocessor reset and auto reset
  - Idle or unassigned cell generator
    - Microprocessor-written values for GFC, PTI and CLP fields
  - Scrambler option ($x^{43}+1$)
  - HEC generator
    - with optional COSET polynomial addition
  - Test option: invert cell bits.

PPP Features

- Receive PPP Features
  - Data inversion option
  - Descrambler ($x^{43}+1$) option
  - Invalid frame detection
  - Octet destuffing
    - 7D Hex octet removed, next octet exclusive-or gated with 20 Hex
  - Check packet for short frame length
    - CRC-16 (less than 32 bits between flags)
    - CRC-32 (less than 48 bits between flags)
  - Long frame length
    - Programmable between 4 bytes and 8192 bytes
    - No size option
  - CRC-16 or CRC-32 FCS check
    - Pass-through FIFO option
  - Transparent mode (bypass HDLC controller)
  - Receive FIFO
    - Four blocks, each 48 octets or sixteen blocks, each 16 octets
    - FIFO overflow alarm
    - Depth alarm
    - Microprocessor reset and auto reset
  - Performance measurements
    - Choice of CRC errors, long or short frames detected, invalid frames received, total number of frames
- Receive Terminal Side Modified UTOPIA Interface
  - Single-PHY or Multi-PHY
    - Parity generation, even or odd over data
    - 16-octet or 48-octet block data option for Multi-PHY
    - 8-bit bus with 16-bit bus option
      - CRC and abort indications
    - Force output bus signals to High-Z state
- Transmit Terminal Side Modified UTOPIA Interface
  - Single-PHY or Multi-PHY
    - Parity check, odd or even
    - 16-octet or 48-octet block transfer for Multi-PHY
- Transmit PPP Features
  - Transmit FIFO
    - Four blocks (48 octets per block) or sixteen blocks (16 octets per block)
    - FIFO overflow alarm
    - Depth alarm (first cell read, reset on two empty cells)
    - Microprocessor reset and auto reset
  - Flags fill character generation
  - Octet stuffing
    - Flag sequence

    - Control escape
- CRC generation
    - CRC-16
    - CRC-32
    - Pass-through CRC mode
- Invalid frame generation
- Transparent operation
- Data inversion option
- Scrambler ($x^{43}+1$) option

APPLICATION EXAMPLE

The application of the PHAST-3P in a dual unidirectional ring architecture is illustrated in Figure 1 below for both IP/PPP and ATM/CDB switching network interfaces.

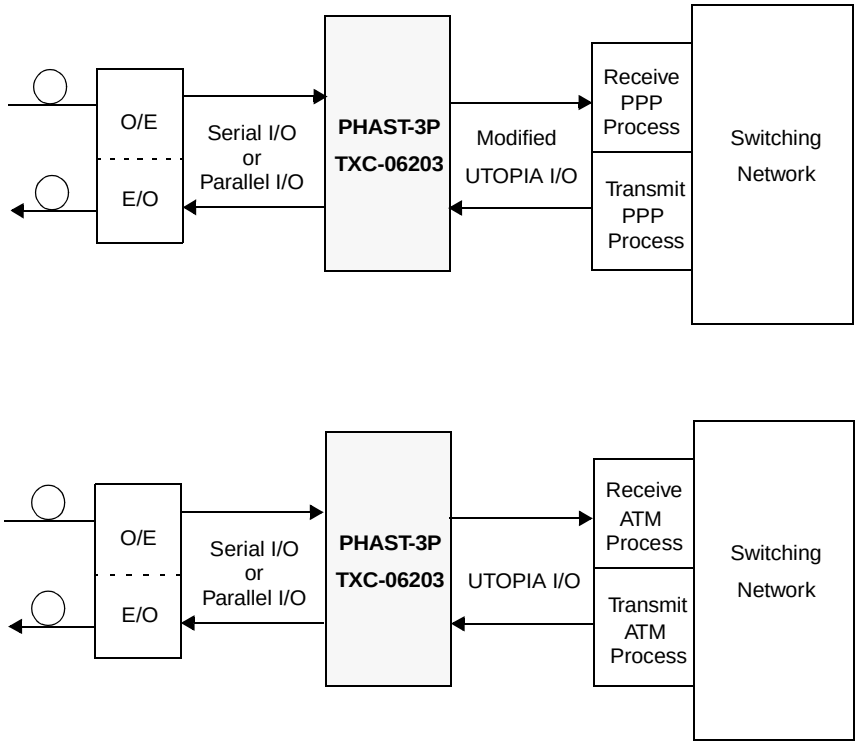


Figure 1. PHAST-3P in Dual Unidirectional Ring Architecture

FUNCTIONAL DESCRIPTION

The functional block diagram for the CDB configuration of the UTOPIA interface is shown in Figure 2 below.

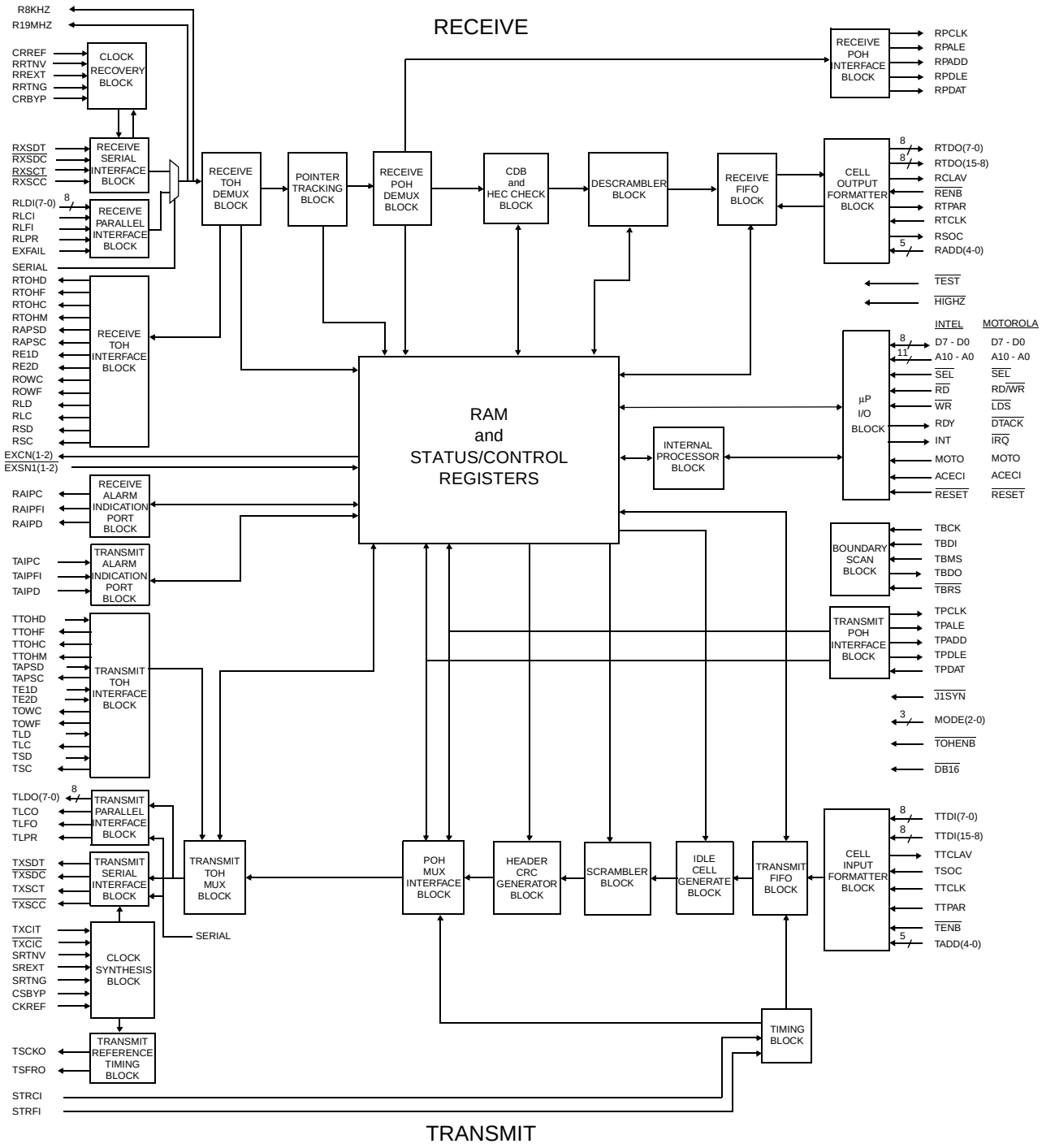


Figure 2. PHAST-3P with CDB UTOPIA Interface Block Diagram

The functional block diagram for the PPP configuration of the UTOPIA interface is shown in Figure 3 below.

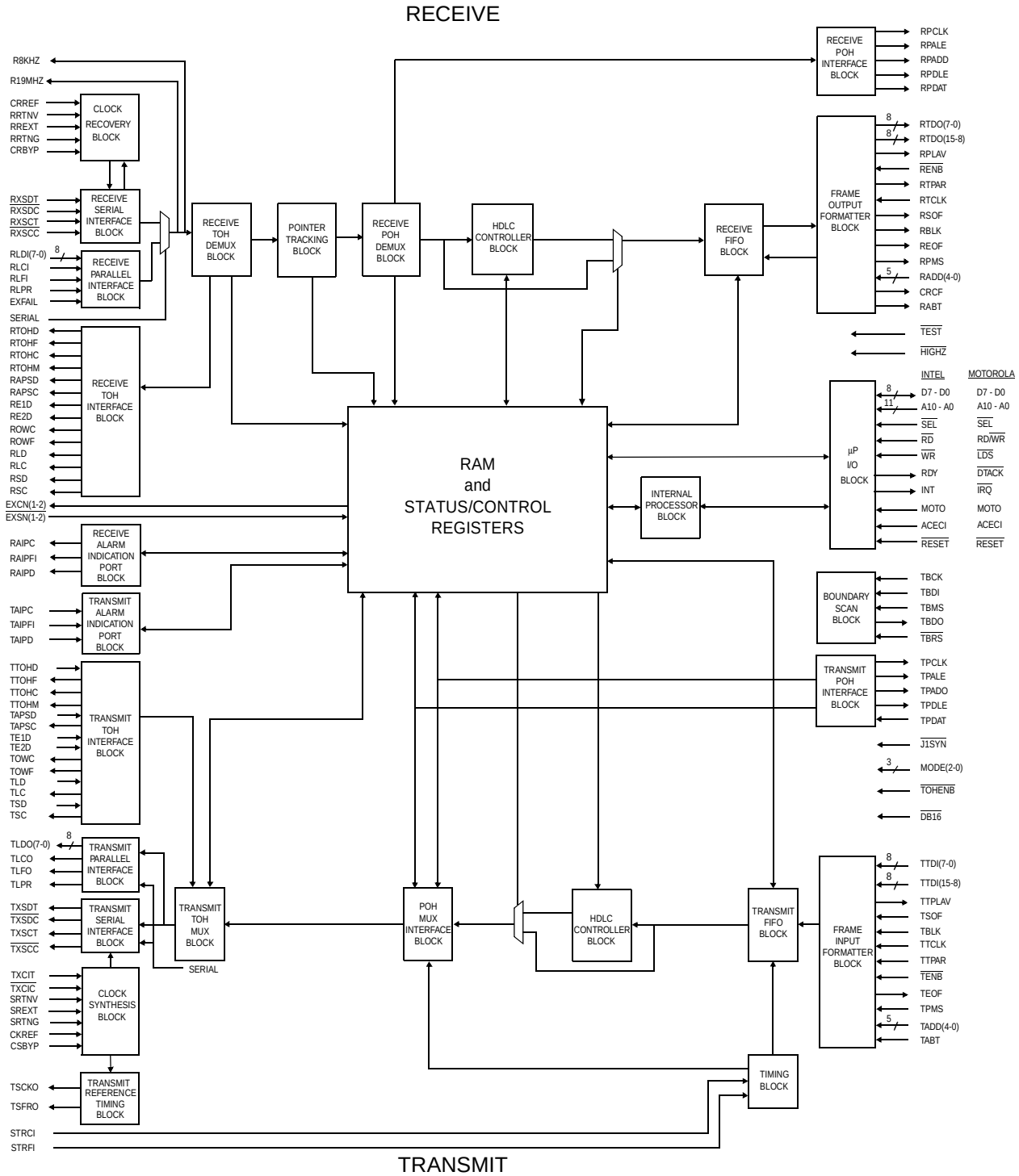


Figure 3. PHAST-3P with PPP UTOPIA Interface Block Diagram

The PHAST-3P provides two selectable line side SONET/SDH interfaces: a bit-serial pseudo-ECL interface and a byte-wide parallel interface. The selection is common for both the receive and transmit sides. The selection of the interface is determined by the state placed on signal lead SERIAL. A high selects the line interface to be serial, while a low selects the interface to be parallel.

The clock recovery circuit for the serial interface is enabled by placing a low on the CRBYP lead. When the clock recovery circuit is enabled, the pseudo-ECL interface consists of the following input signals: true and complement receive data (RXSDT and RXSDC). A 19.44 MHz clock is recovered from the RXSDT and RXSDC signal leads. When the clock recovery circuit is bypassed by placing a high on the CRBYP lead, the pseudo-ECL interface must consists of the following input signals: true and complement receive clocks (RXSCT and RXSCC) and receive data (RXSDT and RXSDC).

The incoming serial interface signal is monitored for loss of signal in the clock recovery mode, or when the external clock input is provided. There are two requirements regarding loss of signal detection, one specified in ANSI documents and the other specified in ETSI/ITU documents. The PHAST-3P meets both loss of signal requirements.

The byte-parallel interface consists of the following input signal leads: receive byte data RLDI(7-0), receive clock RLCI, optional frame pulse RLFI, and receive parity signal RLPR. Bit 7 is defined as the MSB and the first bit received in the SDH/SONET bytes. When the optional frame pulse RLFI is not provided an internal circuit establishes the SDH/SONET byte frame boundaries for the parallel data. The incoming parallel interface clock is also monitored for a loss of clock. The loss of clock detection is a sanity check for stuck high or stuck low conditions. Parity is calculated and compared against the state of the RLPR input lead. When a parity error is detected an alarm (and possible interrupt) will occur. No other actions are taken, and the PHAST-3P will continue to operate. The parity check is programmable for odd/even parity as well as parity over data only or over both data and framing. The parallel interface data is also monitored for a stuck high or low condition over a frame period when the scrambler is enabled.

An 8 kHz clock reference signal is derived from either the serial or parallel clock interface signals. In addition, a 19.44 MHz clock reference signal is also provided. The reference clocks are derived from either the 155.52 MHz input clock when the clock recovery block is disabled, from the clock recovery block when enabled, or from the SONET/SDH line input clock (RLCI) when the parallel interface is enabled.

An external SDH/SONET line failure indication input (EXFAIL) is also provided. This input signal lead is enabled when the byte-parallel interface is enabled. This input may be used to indicate, for an example, a loss of frame alignment from upstream circuitry when the PHAST-3P is configured in a higher order SDH/SONET system. The PHAST-3P also provides two external scan leads (EXSN1 and EXSN2) for both the serial and parallel interfaces. These signal leads may be used to notify the microprocessor from an external line interface circuit.

The Receive TOH Demultiplexer block interfaces the line and section overhead bytes to the Receive TOH Interface block and writes the TOH bytes into designated RAM locations for microprocessor read access. The processing performed by this block includes optional descrambling, performing a single-byte comparison (ANSI), or a 16-byte trail trace comparison (ETSI) for the J0 (C1) byte. The PHAST-3P does not perform a CRC-7 calculation of the ETSI trail trace message written by the microprocessor. This block also performs a B1 parity check, B2 parity check with a programmable B2 BER measurement, line REI count, APS byte processing consisting of inconsistent APS byte, change in APS byte status, line RDI (FERF) detection, and line AIS detection. The incoming K1 and K2 bytes are debounced for microprocessor read access. Bits 5, 6, 7 and 8 in the S1 byte (synchronization status message byte) are checked for a change in status indication.

TOH bytes, including the unused bytes, are written into RAM locations for microprocessor read access, in addition to being provided at the TOH interface. The TOH interface consists of the following signal leads: receive TOH byte data RTOHD, receive TOH clock RTOHC, receive TOH frame pulse RTOHF, and receive TOH byte marker indicator RTOHM. The TOH byte marker indicator RTOHM indicates the location of one of the following TOH bytes: J0 byte, section data communication bytes (D1 - D3), line data communication bytes (D4 -D12), E1 order wire byte, E2 order wire byte, K1 and K2 bytes indication, or F1 byte.

The K1 and K2 bytes, E1 order wire byte, E2 order wire byte, section data communication bytes (D1 - D3) and line data communication bytes (D4 - D12) are also provided as separate TOH byte interfaces. The K1 and K2 byte interface consists of the following signal leads: receive K1 and K2 byte output data RAPSD, receive output clock RAPSC, and output frame pulse RAPSF. The order wire interface consists of the following leads: receive E1 byte output data RE1D, receive E2 byte output data RE2D, receive output clock ROWC, and output frame pulse ROWF. The section data communication bytes (D1 - D3) interface consists of the following leads: receive data output RSD, and receive clock output RSC. The line data communication bytes (D4 - D12) interface consists of the following leads: receive data output RLD, and receive clock output RLC.

The H1 and H2 bytes in the STM-1/STS-3c format are used determine the starting location of the J1 byte and the remaining payload bytes in the VC-4/SPE format. The H1/H2 bytes are checked for Loss Of Pointer (LOP), path AIS, new pointer value, pointer decrements and increments, and a false concatenation (STS-3 format). The pointer tracking state machine is designed according to the state machine specified in ETSI and ANSI documents. The pointer tracking state machine SS-bits can be disabled as part of pointer tracking or their value can be programmed by the microprocessor.

The nine POH bytes in the STM-1 VC-4 and STS-3c SPE are provided at a POH interface for external access. All POH bytes are also written into RAM locations for microprocessor read access in addition to being provided at the POH interface. The POH interface leads consist of: clock RPCLK, address latch enable lead RPALE, address lead RPADD, data latch enable lead RPDLE, and a data lead RPDAT.

Receive POH byte processing consists of optional J1 byte processing (16-byte trail trace comparison against a microprocessor value or 64-byte LF/CR alignment), B3 byte parity calculation with programmed BER measurement, C2 byte mismatch alarm (when compared against a microprocessor-written value) or unequipped status, G1 byte REI count, RDI (single-bit or three-bit), and a K3 byte debounced. Three-bit RDI is defined for ANSI applications, while single-bit RDI is recommended for ITU applications. The PHAST-3P does not perform a CRC-7 calculation of the J1 byte ETS trail trace message written by the microprocessor. The K3 byte is also monitored for change in a new value after three frames. The received H4, Z4 and N1 bytes will be written into the designated memory locations, and provided at the POH interface only.

Receive CDB Processing

The ATM cells are carried in the STM-1 VC-4 or STS-3c SPE by aligning the byte structure of every cell with the byte structure of the payload. The entire payload will be filled with cells, yielding a transfer capacity for the cells of 149.760 Mbit/s. Because the payload does not contain an integer multiple of the 53 byte ATM cells, some cells will cross the VC-4/SPE boundary.

The CDB block performs cell delineation. Cell delineation is defined as the process of finding the boundaries of the ATM cells using the Header Error Check (HEC) field defined in the five-byte header field. The HEC check is a CRC-8 calculation over the first four bytes of the ATM cell header using the generating polynomial is $x^8 + x^2 + x + 1$. The PHAST-3P will perform single-bit error correction and multiple-bit error detection. An option is provided to either drop a cell or pass it along to the FIFO. The PHAST-3P will count correctable HEC errors (8 bits), uncorrectable HEC errors (8 bits), and receive cells (16 bits). The number of cells received and written to the receive FIFO is counted. Cells that are filtered due to HEC errors or idle/unassigned cell matches will not be counted.

A descrambling option is provided. When enabled, descrambling will be performed over the 48-byte payload. The self-synchronizing scrambler uses the polynomial $x^{43} + 1$, as defined in the ITU I.432 document.

A match header register, match header mask register, and match header register enable bit are provided. Individual masks are provided for the GFC, PTI and CLP fields. This extends the cell filtering capability beyond the 00 00 00 01 header of a standard idle cell.

The receive FIFO will accommodate up to four cells, where each cell is equal to 53 bytes. A FIFO overflow status indication is provided. The receive FIFO will automatically reset upon an overflow condition. In addition, an alarm indication is provided when the fourth cell is being written. This status alarm is reset automatically when two empty cell segments become available within the FIFO. The receive FIFO may also be reset by the microprocessor.

The receive terminal-side UTOPIA bus interface supports either a Single-PHY (cell or octet) or a Multi-PHY UTOPIA interface. The UTOPIA bus interface consists of the following leads: data byte output RTDO(7-0) or data word output RTDO(15-0), input clock RTCLK, cell available output RCLAV, input enable RENB, output start of cell RSOC, output parity RTPAR, and Input Address RADD(4-0) for the Multi-PHY interface when it is selected. Parity RTPAR is calculated as either even or odd over the data bus only. The data bus is configured for 16 bits when a low is placed on the DB16 lead. A 16-bit bus is recommended for Multi-PHY operation.

Receive PPP Processing

The PHAST-3P supports the Point to Point Protocol (PPP) specified in the RFC documents for SDH/SONET application using octet stuffing/destuffing. The data bus interface for SONET PPP applications can be either 16 or 8 bits wide. The data bus is configured for 16 bits when a low is placed on the DB16 lead.

The HDLC controller performs layer 2 processing. The HDLC controller performs: descrambling, data inversion, flag (7E Hex) detection to determine the start of the packet, octet de-stuffing, a check for minimum and maximum frame length, detects an invalid frame character (i.e., abort), performs a CRC-16 or CRC-32 calculation, provides a CRC-16 or CRC-32 pass-through mode, inter-frame flag discard, and detects the closing flag. The use of a descrambler has been defined in the ANSI standards body. The descrambler, using a $x^{43}+1$ polynomial, is provided as an option. The HDLC controller can also be bypassed for transparent operation.

The receive FIFO will accommodate up to four blocks of data, with each block consisting of 48 bytes of data or sixteen blocks of data, with each block consisting of 16 bytes of data. A FIFO overflow status indication is provided, along with a status indication when the fourth block segment is being written to. The alarm is reset automatically when two empty blocks become available within the FIFO.

The receive FIFO may also be reset by the microprocessor. Please note that flags filler characters will not be written into the receive FIFO by the receive HDLC controller. The PHAST-3P will measure the following performance parameters associated with the incoming packets: number of frames, number of CRC errors, number of short frames, number of long frames, number of invalid frames received, and number of all error conditions. The time of the measurement may be controlled by the microprocessor, and one parameter at a time or all parameters may be measured during a microprocessor-determined period.

The terminal-side PPP modified UTOPIA bus interface consists of the following signaling leads: output data byte RTDO(7-0) or data word RTDO(15-0), input clock RTCLK, output packet available RPLAV, input enable RENB, output start of frame RSOF, output 16-byte or 48-byte block transfer RBLK, output parity lead RTPAR, output end of frame REOF, output most significant byte RPMS when the data bus is configured for 16-bits, input address RADD(4-0) for Multi-PHY operation, output CRC fail indication CRCF, and output frame abort RABT.

Transmit CDB Processing

The transmit terminal-side UTOPIA bus interface will support either a Single-PHY (cell or octet) or a Multi-PHY UTOPIA interface. The Multi-PHY level 2 UTOPIA interface is specified in ATM Forum documents. The UTOPIA interface consists of the following signal leads: input data TTDI(7-0) or TTDI(15-8), input clock TTCLK, output cell available TCLAV, input enable TENB, input start of cell TSOC, input parity lead TTPAR, and input address TADD(4-0) when the data bus is configured for Multi-PHY operation. The bus width is programmable as 8 bits or 16 bits. A 16-bit bus is recommended for Multi-PHY operation. The data bus is configured for 16 bits when a low is placed on the DB16 lead. The DB16 lead is common with the receive side. The interface will support an even or odd parity check over data only. When a parity error is detected, no action is taken other than an alarm notification.

The PHAST-3P can be programmed to control the depth of the FIFO from two cells (106 bytes) to four cells (212 bytes). This allows the user to minimize cell latency when required. The transmit FIFO is also monitored for an overflow condition. The transmit FIFO will be automatically reset upon occurrence of an overflow state. In addition, the FIFO may be reset by the microprocessor. An alarm indication is provided when the first cell segment is being read from a full buffer. The alarm is reset automatically when two empty cells become available within the FIFO. The number of cells read from the FIFO is counted in a 16-bit performance counter. Idle or unassigned cells will not be counted.

The PHAST-3P will generate and send idle or microprocessor-written unassigned cells when no outstanding ATM cells are detected in the transmit FIFO. The idle pattern specified in the ITU I.432 document is transmitted. This cell is defined as having a header equal to 0000000152 (with COSET added), followed by 48 bytes of 6A Hex. An option is provided in which the microprocessor can write the value of the GFC, PTI and CLP fields within the header, and the value of all 48 payload bytes.

The scrambler is provided as an option. When enabled, scrambling is performed over the 48-byte payload only, using the polynomial $x^{43} + 1$. The self-synchronizing scrambler is defined in the ITU I.432 document.

The HEC generator performs a CRC-8 calculation using the generating polynomial $x^8 + x^2 + x + 1$. An option is provided which enables the addition of the COSET polynomial $x^6 + x^4 + x^2 + 1$ to the calculated HEC byte before transmission. In addition, the HEC generation on the transmit cell can be disabled. When disabled, the transmit HEC byte in the header byte from the transmit FIFO is transmitted. A test option enables the inversion of the HEC byte prior to insertion into the transmitted cell.

Within the STM-1/STS-3c frame, the payload location is fixed to a pointer offset of 522. The timing is derived from the external clock STRCI and frame pulse STRFI. Signal STRFI is an active high, one clock cycle-wide frame pulse, clocked in rising edges of the reference clock STRCI. This reference can be provided by connecting TSCKO to STRCI, and TSFRO to STRFI.

Transmit PPP Processing

The modified UTOPIA interface for the PPP over SDH/SONET feature is based on the UTOPIA Interface standard. The modified UTOPIA bus interface consists of following signaling leads: input data TTDI(7-0) or data TTDI(15-0), input clock TTCLK, output packet available TPLAV, input enable $\overline{\text{TENB}}$, input start of frame TSOF, input 16-byte or 48-byte block transfer TBLK, input parity lead TTPAR, input end of frame TEOF, input address TADD(4-0) when the Multi-PHY interface is selected, and an output transmit abort TABT. An even or odd parity check is performed on data only. Other than an alarm indication, no action is taken for a parity error.

The transmit FIFO will accommodate up to four blocks of data, with each block consisting of 48 bytes of data or up to sixteen blocks of data, with each block consisting of 16 bytes of data when the Single-PHY or Multi-PHY modified UTOPIA interface is selected. A 16-bit bus is recommended for Multi-PHY operation. A FIFO overflow status indication is provided. The transmit FIFO is automatically reset when an overflow condition occurs. The frame is terminated by transmitting an invalid frame indication, and an overflow indication is provided for the downstream circuitry with an active high on the TABT lead. The transmit FIFO may also be reset by the microprocessor. In addition, an alarm status indication is provided when the first block segment is being read from a full buffer. The alarm is reset when two empty blocks become available within the FIFO.

The HDLC controller performs the following functions: flag generation, generating inter-fill characters of flags (7E Hex - 0111 1110) between the opening and closing flags of a frame, octet stuffing, CRC-16 or CRC-32, invalid frame generation, CRC pass-through, data inversion, transparent operation, and SDH/SONET scrambling.

An option is provided for a scrambler prior to inserting the data into the SDH/SONET payload. The scrambler uses a $x^{43}+1$ generating polynomial.

Within the STM-1/STS-3c frame, the payload location is fixed to a pointer offset of 522. The timing is derived from the external clock STRCI and frame pulse STRFI. Signal STRFI is an active high, one clock cycle-wide frame pulse, clocked in rising edges of the reference clock STRCI. This reference can be provided by connecting TSCKO to STRCI, and TSFRO to STRFI.

Transmit SDH/SONET Processing

The PHAST-3P inserts the POH bytes from either RAM locations or a POH interface. The insertion of POH bytes has individual programmable control bits for maximum system flexibility.

The transmit POH interface consists of the following signals: output clock TPCLK, output address latch enable lead TPALE, output address TPADD, output data latch enable lead TPDLE and input data lead TPDAT.

The transmitted J1 byte message size can be programmed to be either 16 or 64 bytes in length. The PHAST-3P does not calculate the CRC-7 for the 16-byte trail trace message. The G1 byte REI value is inserted from errors derived from the receive side, the POH interface port, or from a transmit RAM location. To prevent missed counts from being transmitted due to phase differences between the receive and transmit side clocks, a synchronization circuit is provided on the transmit side. The capability to generate single-bit or three-bit RDI is also provided. To prevent a transient RDI state from being transmitted, RDI will be transmitted for at least 20 frames when an alarm occurs. The B3 parity generator has an error mask in which the bits in error and the number of frames transmitted in error can be programmed by the microprocessor.

The PHAST-3P can generate an unequipped status channel, or a supervisory unequipped channel, path AIS, and line AIS.

The Transport Overhead bytes (TOH bytes), including the unused bytes, and the B1 and B2 bytes (which may be used as error masks) may be provided at the transmit TOH interface for insertion into the transmit bit stream when selected. The TOH interface consists of: input data lead TTOHD, output frame pulse lead TTOHF, output programmable byte indication lead TTOHM, and an output clock lead TTOHC. The TOH byte indicator TTOHM indicates the location of one of the following programmable TOH bytes: J0 byte, section data communication bytes (D1 - D3), line data communication bytes (D4 - D12), E1 order wire byte, E2 order wire byte, K1 and K2 bytes, or F1 byte.

The K1 and K2 bytes, the E1 order wire byte, the E2 order wire byte, the section data communication bytes (D1-D3) and the line data communication bytes (D4-D12) also have separate interface access in addition to memory map RAM locations. The K1 and K2 byte interface consists of the following signal leads: transmit K1 and K2 byte input data TAPSD, transmit output clock TAPSC and output frame pulse TAPSF. The order wire interface consists of the following leads: transmit E1 byte input data TE1D, transmit E2 byte input data TE2D, transmit output clock TOWC and an output frame pulse TOWF. The section data communication bytes (D1 - D3) interface consists of the following leads: transmit section data communication byte input data TSD and transmit section data communication byte output clock TSC. The line data communication bytes (D4 - D12) interface consists of the following leads: transmit line data communication byte input data TLD, and transmit line data communication byte output clock TLC.

Depending upon the option selected, TOH bytes may be transmitted from RAM locations, or from the various TOH interfaces. In addition, it is possible to force a B1 error condition in which each column (bit position) from a RAM location or from the TOH interface is exclusive-or gated with the calculated B1 value, thus causing the transmitted B1 bit position to be transmitted inverted. Under microprocessor control up to 8 error indications (which correspond to each of the eight columns) may be transmitted. The B2 byte calculation is performed internally. In addition, an internal or external error mask may be used to transmit individual bit errors. The number of frames in which the errors are to be transmitted is programmable. Line RDI (FERF) can also be generated as a result of TOH alarms or under microprocessor control. Line RDI state is transmitted for at least 20 frames when activated.

The SDH/SONET scrambler selection is optional. The scrambler is the same as the descrambler with the generating polynomial $x^7 + x^6 + 1$, and it is reset to 1111111 on the most significant bit (MSB) of the byte following the C1 byte.

The SDH/SONET line interface can be configured to be either a 155.52 Mbit/s bit-serial interface or a byte-parallel interface. The serial interface is selected by placing a high on the SERIAL lead. An optional Clock Synthesis block is provided for the serial interface. The Clock Synthesis block is enabled by placing a low on the CSBYP lead. The serial interface consists of a pseudo-ECL differential transmit clock output TXSCT and TXSCC and differential transmit data output signals TXSDT and TXSDC. The Clock Synthesis block uses a 19.44 MHz clock from the CKREF lead to derive the 155.52 MHz clock.

The Clock Synthesis block is bypassed by placing a high on the CSBYP lead. When the Clock Synthesis block is bypassed, the serial interface consists of a pseudo-ECL differential transmit clock input TXCIT and its complement TXCIC, pseudo-ECL differential transmit clock output TXSCT and its complement TXSCC, and pseudo-ECL differential transmit data output TXSDT and its complement TXSDC.

The byte-parallel interface is selected by placing a low on the SERIAL lead. The byte-parallel interface consists of the 19.44 MHz transmit clock output signal TLCO, transmit data output byte signal TLDO(7-0), and an active high, one clock cycle-wide frame pulse TLFO. Bit 7 is defined as the MSB and the first bit transmitted in the SDH/SONET bytes. Options are provided to calculate even or odd parity and parity over data only or parity over data plus framing signal.

The PHAST-3P provides two drive leads, EXCN1 and EXCN2, whose output states are controlled by the microprocessor. This feature is available for both line interface options.

All of the control registers, performance counters, status and alarm indications, and RAMs are accessed through the PHAST-3P microprocessor bus interface. The PHAST-3P supports both an Intel and a Motorola microprocessor bus interface. The selection of the microprocessor buses is controlled by the MOTO control lead. When the MOTO lead is high, the Motorola bus is selected, and when low, the Intel bus is selected.

The Intel microprocessor bus interface consists of a eight bidirectional data bus leads (D7 - D0), eleven address leads (A10 - A0), a select lead $\overline{SEL}$, read lead $\overline{RD}$, write lead $\overline{WR}$, an interrupt request lead INT, and ready lead RDY. Leads D0 and A0 are defined as the least significant bits of the data and address buses.

The Motorola microprocessor bus interface consists of eight bidirectional data bus leads (D7 - D0), eleven address leads (A10 - A0), a select lead $\overline{SEL}$, a read RD / write $\overline{WR}$ lead, an interrupt request lead $\overline{IRQ}$, an active low LDS ($\overline{LDS}$) signal for 68302 operation, and a data transfer acknowledgment lead $\overline{DTACK}$. Leads D0 and A0 are defined as the least significant bits of the data and address buses. The $\overline{LDS}$ signal uses the same lead as the Intel $\overline{WR}$ signal.

It is recommended that RDY/$\overline{DTACK}$ lead be used with the corresponding microprocessor timing diagram, as the RDY/$\overline{DTACK}$ pulse width may be extended considerably.

An external clock (ACECI), asynchronous with respect to the other clocks connected to the PHAST-3P, is used for the two internal ACE processors and for internal RAM arbitration (i.e., internal read/write operations versus microprocessor read/write operations). This clock should be operated at a frequency of 48 MHz +/- 2% and a duty cycle of (50 +/- 10)%.

The alarm reporting structure consists of unlatched and latched (event) alarm bit positions. The unlatched alarm bit positions will reflect the current status of a detection circuit (e.g., C2 mismatch detection). A latched alarm (event bit) is capable of latching on either a positive level, positive transition, negative transition, or positive/negative transition of the unlatched alarm. A latched bit position, and the other latched bit positions in that register location, are cleared on a microprocessor read cycle.

The latched (event) bits cause a hardware interrupt when enabled. The PHAST-3P provides both a hardware indication (INT/$\overline{IRQ}$ output lead) and software polling register. The software polling register points to registers within the memory map that caused the interrupt to occur.

All counters are capable of counting events as either bits or blocks, unless otherwise specified. All 16-bit performance counters have a special 16-bit read operation which will allow uninterrupted access, without the danger of one byte changing while the other byte is read. Counts that occur during the read cycle are held, and the counter is updated afterwards. All the performance counters can be configured to be either saturating or non-saturating. When the performance counters are configured to be saturating, the counters will stop at their maximum count. A saturating counter is reset on a microprocessor read cycle. When the counters are configured to be non-saturating, roll over (starting with 0) occurs after the maximum count is reached. In this mode, the counters do not clear on a microprocessor read cycle, but continue to count. All the performance counters can be reset simultaneously by writing to a reset control bit.

The PHAST-3P supports the following boundary scan test instructions specified in the IEEE 1149.1 document: EXTEST, SAMPLE, and BYPASS. The boundary scan test bus interface has four input signals: a test clock TBCK, test mode select TBMS, test data input TBDI and test reset $\overline{TBRS}$. Test data TBDO is an output signal.

A lead designated as $\overline{HIGHZ}$ is provided for customer testing. An active low placed on this lead forces all output leads, except TBDO and the P-ECL leads, to the high impedance state for board testing.

Please note that the PHAST-3P has separate 3.3 volt power and ground leads for the (analog) clock recovery and clock synthesis blocks, in addition to the power and ground leads provided for the other blocks. It is recommended that separate planes and bypass networks be used for connecting the VDD and AVDD power leads on the PHAST-3P to +3.3 volts. Furthermore, each power supply lead should have a 0.1 microfarad capacitor to its corresponding ground.

SELECTED PARAMETER VALUES

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	3.9	V	Note 1
DC input voltage	V_{IN}	-0.5	5.5	V	Notes 1, 3
Storage temperature range	T_S	-40	150	^oC	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	Absolute value 2000		V	Note 4
Latch up	LU				Meets JEDEC Standard 78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Input signal leads can accept 5 volt signals from the outputs of 5 volt devices.
4. Absolute value tested per MIL-STD-883D, Method 3015.7.

THERMAL CHARACTERISTICS

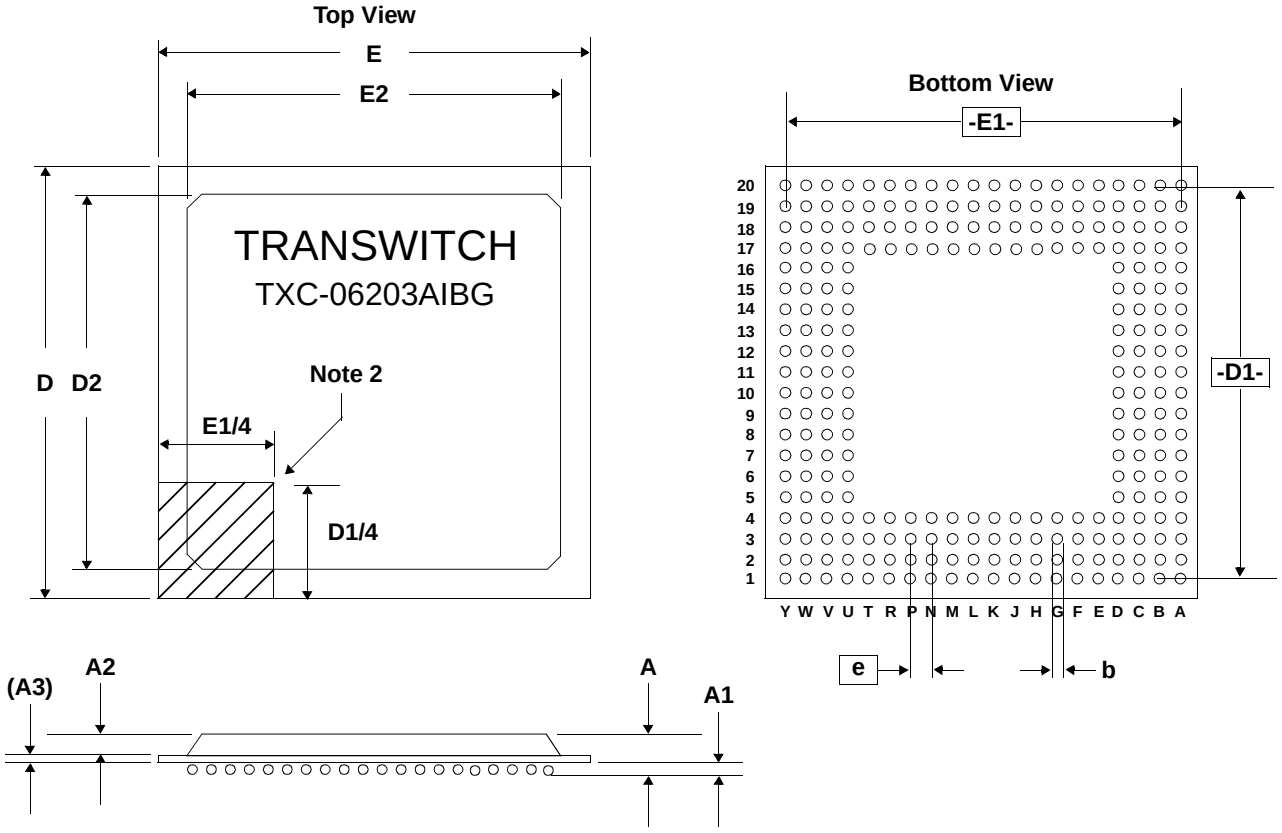
Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: junction to ambient			25	$^oC/W$	0 ft/min linear airflow.

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	3.15	3.30	3.45	V	
I_{DD}		440	490	mA	CDB, RTCLK and TTCLK= 40 MHz, ACECI = 48 MHz, Clock recovery and clock synthesis both enabled; Maximum power is at minimum operating temperature.
Power Dissipation, P_{DD}		1.4	1.7	W	

PACKAGE INFORMATION

The PHAST-3P device is packaged in a 256-lead plastic ball grid array package suitable for surface mounting, as illustrated in Figure 4.



Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 20 x 20, JEDEC code MO-151-BAL-2.

Dimension (Note 1)	Min	Max
A	1.92	2.32
A1	0.50	0.70
A2	1.12	1.22
A3 (Ref.)	0.36	
b	0.50	0.90
D	27.00	
D1 (BSC)	24.13	
D2	23.50	24.70
E	27.00	
E1 (BSC)	24.13	
E2	23.50	24.70
e (BSC)	1.27	

Figure 4. PHAST-3P TXC-06203 256-Lead Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number: TXC-06203AIBG 256-Lead Plastic Ball Grid Array Package

RELATED PRODUCTS

XC-05150, CDB VLSI Device (Cell Delineation Block). Provides cell delineation for ATM cells carried in a physical line at rates of 1.544 to 155 Mbit/s.

TXC-05501, SARA-S VLSI Device (ATM/SMDS Segmentation Controller). Simultaneously segments up to 8000 packets into ATM/SMDS cells.

TXC-05601, SARA-R VLSI Device (ATM/SMDS Reassembly Controller). Simultaneously reassembles ATM/SMDS cells back into up to 8000 packets.

TXC-05802B, CUBIT-*Pro* VLSI Device (*CellBus*® Bus Switch). A single-chip solution for implementing cost effective ATM access systems. It is based on the *CellBus*® bus architecture.

TXC-05804, CUBIT-3 VLSI Device (Multi-PHY *CellBus*® Access Device). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus*® bus architecture.

TXC-05810, ASPEN VLSI Device (*CellBus*® Access Processor). A revolutionary, RISC-based processor designed to support the requirements of next generation multi-service access systems. ASPEN supports *CellBus*® bus operation in both cell and packet modes via two independent *CellBus*® bus ports.

TXC-06212, PHAST-12E VLSI Device (Programmable, High Performance ATM/PPP/TDM SONET/SDH Terminator for Level 12 with Enhanced Features). The PHAST-12E is a highly integrated SONET/SDH terminator device designed for ATM cell, frame, higher order multiplexing, and transmission applications. A single PHAST-12E device can terminate four individual STS-3c or STM-1 lines or a single STS-12/12c or STM-4/4c line.

- NOTES -

- NOTES -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