XBERT Device
Bit Error Rate Generator Receiver
TXC-06125

DATA SHEET

FEATURES

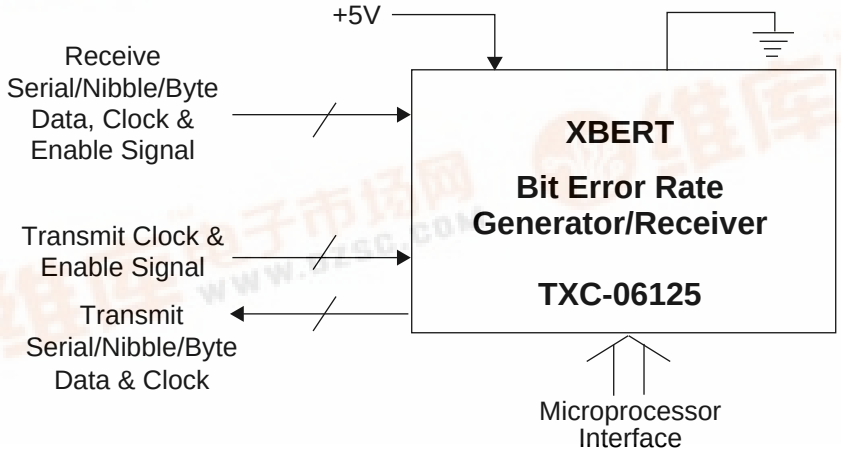
- Bit-serial, nibble-parallel, and byte-parallel interface capability, selectable via control bits
- Transmit and receive clock rate: 100 Hz to 78 MHz for serial, nibble, byte I/O (all telecom rates up to OC-12/STM-4)
- Test patterns at up to 622 Mbit/s using byte-parallel interface and some external circuitry
- 2^{15} - 1, 2^{20} - 1, 2^{20} - 1 QRSS and 2^{23} - 1 pseudo-random generators and detectors
- Fixed word test generator and detector
  - All ones
  - All zeros
  - Alternate 1/0 pattern
  - Alternate 11/00 pattern
- Microprocessor-programmable test word generator and detector (1 to 4 bytes)
- Error generators (single, or 10^{-3} and 10^{-6} BER)
- Bit error counter and clock counter (24 bits each)
- 44-pin plastic leaded chip carrier

DESCRIPTION

The Bit Error Rate Generator/Receiver (XBERT) VLSI device is a microprocessor-programmable multi-rate test pattern generator and receiver on a single chip. It is used for testing the performance of digital communication circuits and communication links. It provides a bit-serial, nibble-parallel or byte-parallel interface, and is capable of operating in a burst data mode by using external signals to enable/disable the transmit and receive clocks. The XBERT generates and analyzes pseudo-random patterns, fixed words, or programmable words. Four pseudo-random test patterns are provided: 2^{15} - 1, 2^{20} - 1, 2^{20} - 1 with zero suppression (Quasi-Random Signal Source, not available in byte-parallel mode), and 2^{23} - 1. The fixed word mode generates and analyzes all zeros, all ones, alternate one/zero pattern or a double alternate one/zero (1100) pattern. The programmable mode allows a choice of one to four bytes written by the microprocessor.

APPLICATIONS

- Transmission and switching systems
- Data communications
- Test equipment
- Remote testing and fault isolation
- Embedded test for proprietary framing algorithms
- Embedded test for secure lines



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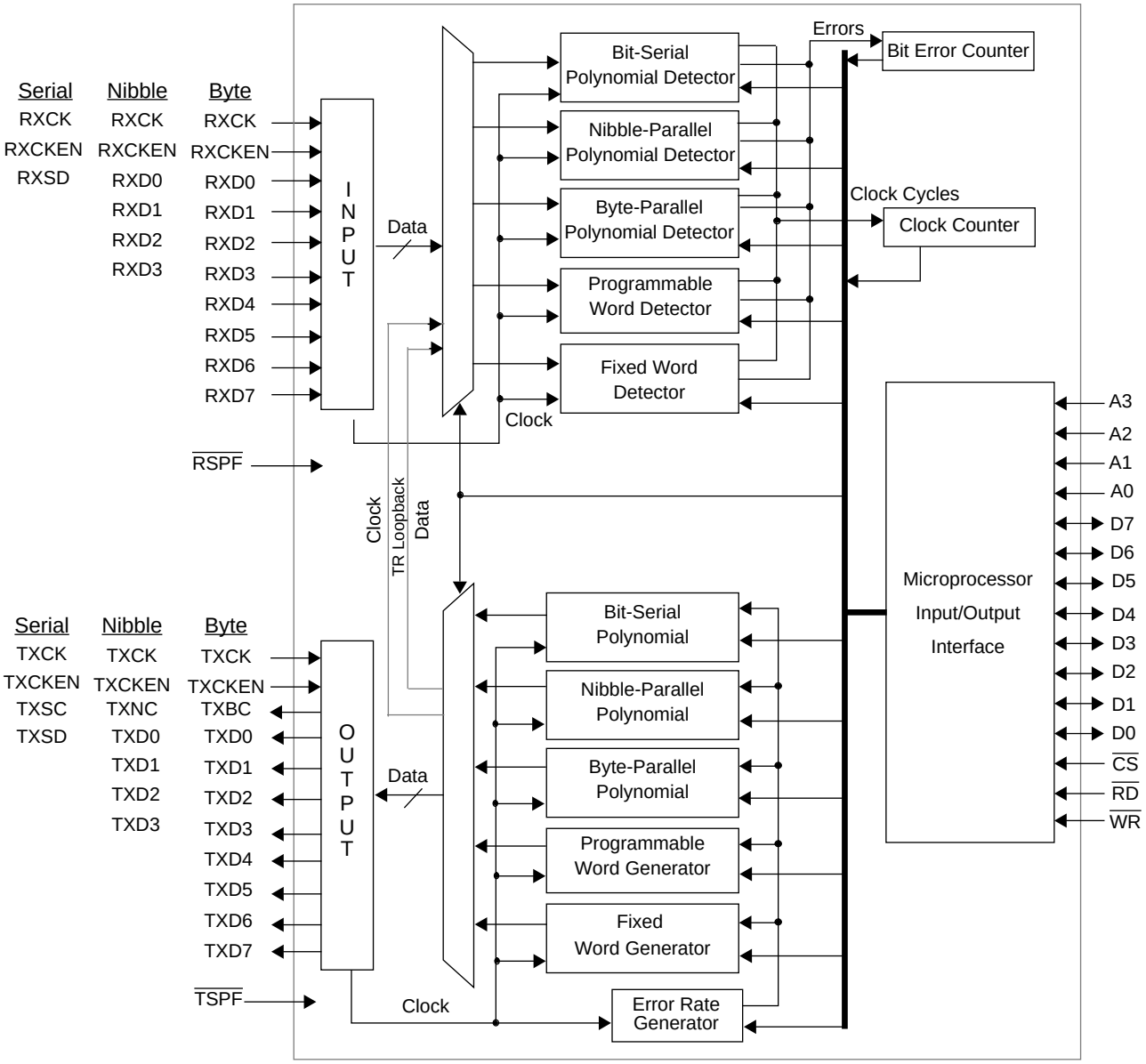


Figure 1. XBERT TXC-06125 Block Diagram

BLOCK DIAGRAM DESCRIPTION

Figure 1 is a simplified block diagram of the XBERT. The Input Block accepts bit-serial (RXSD), nibble-parallel (RXD3-RXD0) or byte-parallel (RXD7-RXD0) data, one of which is selected by writing control bits in the memory map. Incoming data is clocked into the XBERT on positive transitions of the clock signal (RXCK). An input for a receive enable signal (RXCKEN) is provided. A low on this signal lead disables the input clock from clocking in data and permits operation in burst mode.

The test pattern, which is common to both the receiver and transmitter, is selected by writing control bits in the memory map. Each of the test pattern detectors is equipped with a pattern generator and comparator. The comparison between the incoming data and the pattern generator is enabled after frame alignment takes place, or when the receive start of the pseudo-random feature ($\overline{\text{RSPF}}$) is used.

For a 1100 test pattern, a simplified view of the frame alignment (after two consecutive pattern matches), error detection, and loss of frame alignment (after three consecutive pattern match failures) is shown below:

	start	"in frame" detected						LOF detected	
Count good/bad patterns	1	2				1	2	3	
Received signal	1100110011001100. . . .					1100100011101101 1100			
Local generated signal	1100110011001100. . . .					1100110011001100			
Detected errors	0000000000000000. . . .					0000100001000 01			

Running counts of the numbers of bit errors and clock cycles are maintained in two 24-bit counters. Bit error rate performance is determined by having the microprocessor read the counters on a scheduled basis and compute the ratio as an error rate, making due allowance for bit/clock ratios of 4 in nibble-parallel operation and 8 in byte-parallel operation. The clock counter operates regardless of frame alignment status. Both counters should be read together, and at intervals of less than the roll-over interval of the clock counter (about 16 million clock cycles). When XBERT is "in frame", errors are detected one event later. No bit errors are detected after a loss of frame condition occurs.

The transmit clock signal (TXCK) provides the time base for transmitter operation. An input transmit enable signal (TXCKEN) is provided. A low disables the input clock (TXCK) from clocking out data and permits operation in burst mode. This feature is provided for applications where a gapped clock signal is required to prevent the transmitter from clocking out test pattern data.

The interface selection is common to both the receiver and transmitter. The transmit clock signal (TXCK) is used to derive the TXSC, TXNC and the TXBC clock signals. Bit-serial, nibble-parallel and byte-parallel data are clocked out of the XBERT on the falling edges of TXSC, TXNC and TXBC respectively.

For framer applications, a transmit start of pseudo-random pattern framing pulse ($\overline{\text{TSPF}}$) is used to preset the transmit pseudo-random generators' shift registers to ones. This feature permits the XBERT to start the pseudo-random pattern immediately with a fixed relationship to the start of a frame.

For framer applications, a receive start of pseudo-random pattern framing pulse ($\overline{\text{RSPF}}$) disables the frame alignment circuits in the pseudo-random pattern detectors and presets the pseudo-random generators' shift registers to ones, which will result in an immediate "in frame" condition. Used in conjunction with the transmit start of pseudo-random pattern pulse, this feature permits the XBERT to start a search immediately for bit errors in the receive data. A software reset is required to enable the frame alignment circuitry in the pseudo-random detectors for normal operation.

The microprocessor interface consists of four address bits (A3-A0), eight bidirectional data bus bits (D7-D0), chip select ($\overline{\text{CS}}$), and the read ($\overline{\text{RD}}$) and write ($\overline{\text{WR}}$) signal inputs. A Transmit-to-Receive (TR) loopback feature is provided for self-testing the XBERT device.

PIN DIAGRAM

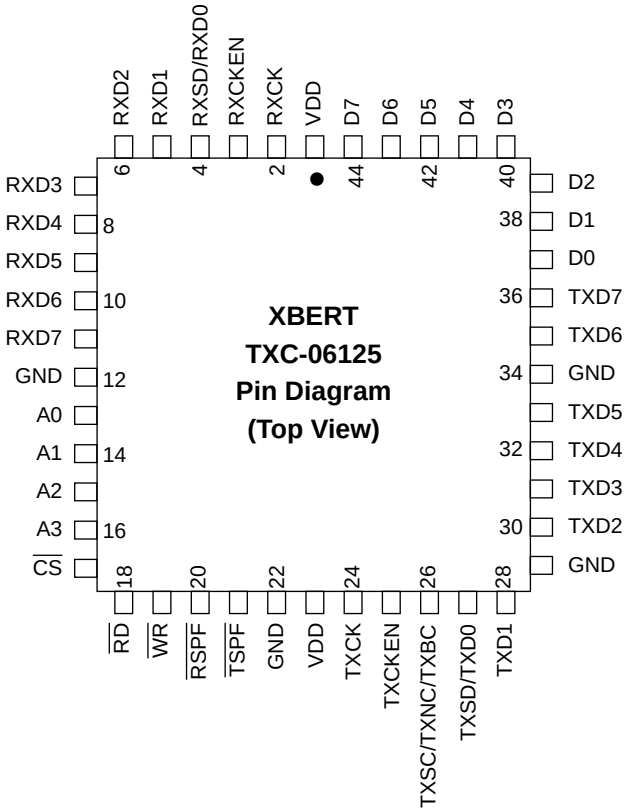


Figure 2. XBERT TXC-06125 Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	1, 23	P		**V_{DD}:** +5 volt supply, ±5%
GND	12, 22 29, 34	P		**Ground:** Zero volt reference level.

*Note: I = Input; O = Output; P = Power

RECEIVE INTERFACE

Symbol	Pin No.	I/O/P	Type*	Name/Function
RXCK	2	I	TTLp	**Receive Clock:** Bit-serial, nibble-parallel, and byte-parallel receive data is clocked into the XBERT on the rising edge of this clock. This clock is used as the time base for all receive functions. It may be gapped to accommodate overhead bit times. Loss of this clock causes the XBERT receiver to become inoperative. See Note 1.
RXCKEN	3	I	TTLp	**Receive Clock Enable:** A high enables the receive clock for clocking data into the XBERT. A low disables the clock from clocking in receive bit-serial, nibble-parallel, or byte-parallel data. See Note 1.
RXSD/RXD0	4	I	TTLp	**Receive Bit-Serial Data/Receive Nibble- or Byte-Parallel Data, Bit 0:** This is the input pin for receive bit-serial data. It is also used as the least significant bit (bit 0) input pin for receive nibble- or byte-parallel data.
RXD1	5	I	TTLp	**Receive Nibble- or Byte-Parallel Data, Bit 1.**
RXD2	6	I	TTLp	**Receive Nibble- or Byte-Parallel Data, Bit 2.**
RXD3	7	I	TTLp	**Receive Nibble- or Byte-Parallel Data, Bit 3:** This is the input pin for the most significant bit (bit 3) for the receive nibble-parallel interface.
RXD4	8	I	TTLp	**Receive Byte-Parallel Data, Bit 4.**
RXD5	9	I	TTLp	**Receive Byte-Parallel Data, Bit 5.**
RXD6	10	I	TTLp	**Receive Byte-Parallel Data, Bit 6**.
RXD7	11	I	TTLp	**Receive Byte-Parallel Data, Bit 7:** This is the input pin for the most significant bit (bit 7) for the receive byte-parallel interface.
$\overline{\text{RSPF}}$	20	I	TTLp	**Receive Start of Pseudo-random Pattern Framing:** An active low enables the PRBS detector to search for an all ones pattern, defining the start of PRBS pattern detection. The first receive pulse sequence (all ones) disables the loss of frame alignment circuit and enables the bit error counter and clock cycle counter. RXCKEN must be enabled before $\overline{\text{RSPF}}$ is clocked in. Once enabled, this feature can only be disabled by a reset. This pin is inoperative for fixed or programmable word patterns.

* See Input, Output and I/O Parameters section for Type definitions.

Note 1: Use of a gapped Receive Clock input (RXCK) or the Receive Clock Enable (RXCKEN) input to disable clocking in of Receive Data for defined time intervals is subject to restrictions. Please contact TranSwitch Applications Engineering for additional technical information relevant to applications employing these capabilities.

TRANSMIT INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
TXCK	24	I	TTLp	**Transmit Clock:** An input clock used as the time base for generating the test patterns and for sourcing bit-serial, nibble-parallel, and byte-parallel transmit data out of the XBERT. This clock may be gapped to accommodate overhead bit times, as required. Loss of this clock causes the XBERT transmitter to become inoperative.
TXCKEN	25	I	TTLp	**Transmit Clock Enable:** A high enables the transmit clock (TXCK) for clocking data out of the XBERT. A low disables the clock from clocking out transmit bit-serial, nibble-parallel, or byte-parallel data.
TXSC/ TXNC/ TXBC	26	O	TTL8mA	**Transmit Serial/Nibble/Byte Clock:** This clock is derived from the transmit clock signal (TXCK), and is used for clocking out data from the XBERT. Data is clocked out of the XBERT on the falling edge of this clock. This clock will have gapped periods corresponding to the times when the transmit enable signal (TXCKEN) is low.
TXSD/TXD0	27	O	TTL8mA	**Transmit Bit-Serial Data/Transmit Nibble- or Byte-Parallel Data, Bit 0:** This is the output pin for transmit bit-serial data. It is also used as the least significant bit (bit 0) output pin for transmit nibble- or byte-parallel data. This bit is the least significant bit and the last bit clocked out for transmit nibble- or byte-parallel data.
TXD1	28	O	TTL8mA	**Transmit Nibble- or Byte-Parallel Data, Bit 1.**
TXD2	30	O	TTL8mA	**Transmit Nibble- or Byte-Parallel Data, Bit 2.**
TXD3	31	O	TTL8mA	**Transmit Nibble- or Byte-Parallel Data, Bit 3:** This is the output pin for the most significant bit (bit 3) for the transmit nibble-parallel interface.
TXD4	32	O	TTL8mA	**Transmit Byte-Parallel Data, Bit 4.**
TXD5	33	O	TTL8mA	**Transmit Byte-Parallel Data, Bit 5.**
TXD6	35	O	TTL8mA	**Transmit Byte-Parallel Data, Bit 6.**
TXD7	36	O	TTL8mA	**Transmit Byte-Parallel Data, Bit 7.** This is the output pin for the most significant bit (bit 7) for the transmit byte-parallel interface.
$\overline{\text{TSPF}}$	21	I	TTLp	**Transmit Start of Pseudo-random Pattern Framing:** An active low pulse causes the XBERT to reset to the beginning of the PRBS pattern. The starting pulse sequence is an all ones pattern, which defines the start of the transmitted PRBS test pattern. If the transmit clock enable signal (TXCKEN) is high when $\overline{\text{TSPF}}$ is clocked in on the positive edge of the clock, the generator transmits the start of the pseudo-random test pattern one and one half clock cycles later (on a negative clock transition). This pin is inoperative for fixed or programmable word patterns.

MICROPROCESSOR INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
D(7-0)	44-37	I/O	TTL8mA	**Data Bus:** Used for programming and reading the registers which reside in the XBERT. The most significant bit is D7. High is logic 1.
$\overline{CS}$	17	I	TTLp	**Chip Select:** A low enables data transfers between the microprocessor and the XBERT memory map during a read/write bus cycle.
$\overline{RD}$	18	I	TTLp	**Read Data:** An active low signal generated by the microprocessor for reading the registers which reside in the memory map. The XBERT memory I/O is selected by placing a low on the chip select lead.
$\overline{WR}$	19	I	TTLp	**Write Data:** An active low signal generated by the microprocessor for writing to the registers which reside in the memory map. The XBERT memory I/O is selected by placing a low on the chip select lead.
A(3-0)	16-13	I	TTLp	**Address Lines:** The four address lines are used to select an XBERT register location. A7 is the most significant bit. High is logic 1.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min*	Max*	Unit
Supply voltage	V_{DD}	-0.3	7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		**	mW
Ambient operating temperature	T_A	**	**	^oC
Operating junction temperature	T_J		125	^oC
Storage temperature range	T_S	-55	125	^oC

*Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

**The minimum and maximum allowable ambient operating temperatures, and the maximum power dissipation, will be dependent on the total thermal analysis.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient			68	$^oC/W$	0 ft/min linear airflow
Thermal resistance - junction to case			13.4	$^oC/W$	0 ft/min linear airflow

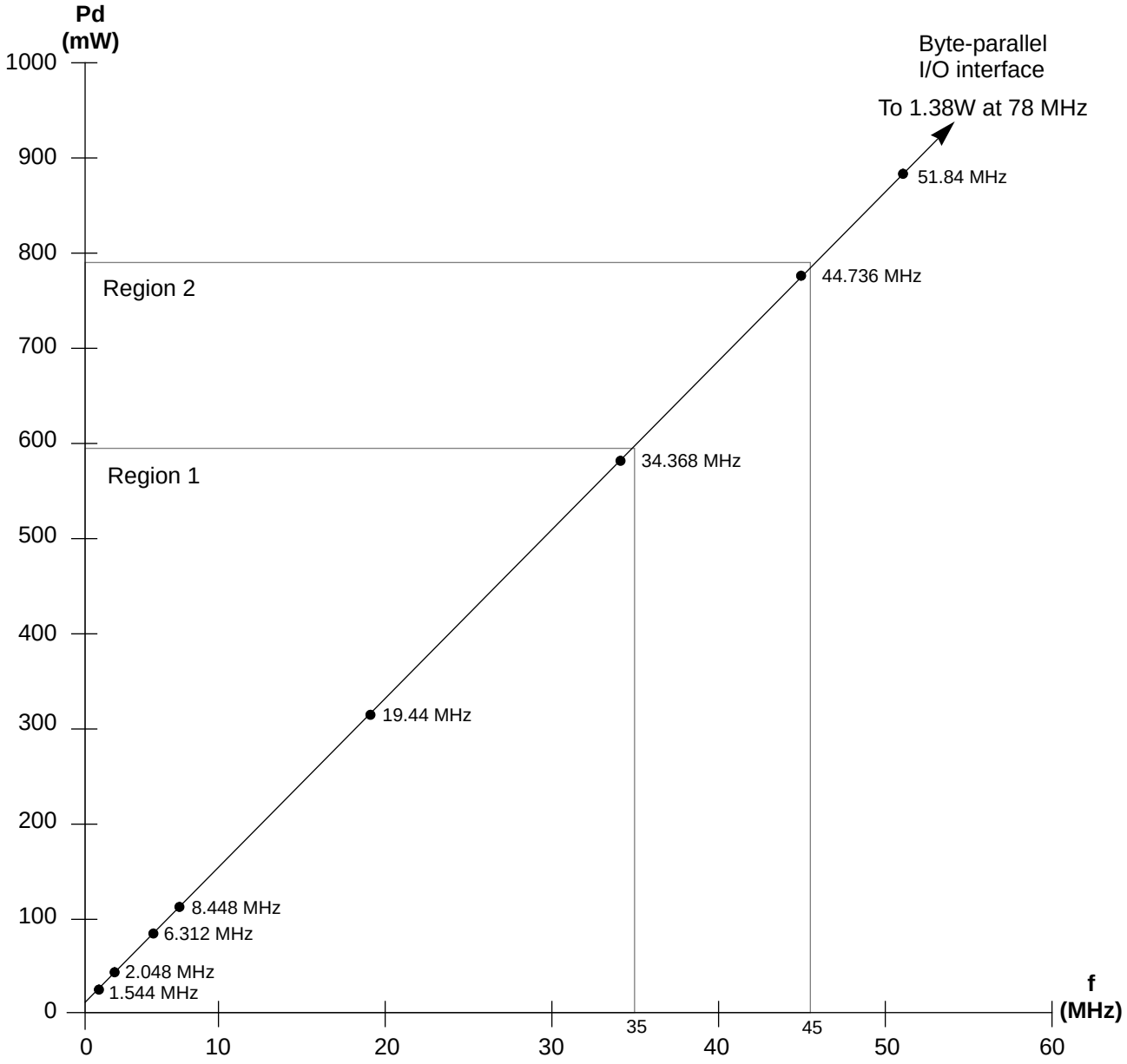
POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}			*	mA	
P_{DD}			*	mW	Inputs switching

*Power dissipation is application specific and depends on the operating frequency, as shown in Figure 3.

Figure 3. Power Dissipation As A Function of Frequency

For operation of the XBERT device in still air without a heat sink, the safe operating regions are defined by the equation: $T_{JMAX} = T_A + [(68°C/W) \times (Pd)] = 125°C$



Region 1 = XBERT may be used in a maximum ambient temperature of $T_A = 85^oC$ for TXCK and RXCK clock frequencies ≤ 35 MHz. This yields a maximum bit rate of 8 x 35 = 280 Mbit/sec.

Region 2 = XBERT may be used in a maximum ambient temperature of $T_A = 70^oC$ for TXCK and RXCK clock frequencies 35 MHz ≤ f ≤ 45 MHz. This yields a maximum bit rate of 8 x 45 = 360 Mbit/sec.

Note: Combinations of frequency and ambient temperature beyond the safe operating regions require additional heat dissipation methods (the maximum power is 1.38 watts at 622/8 = 78 MHz). A TranSwitch Application Note entitled “Designing with TranSwitch XBERT Devices for Byte Interface at the OC-12 Rate”, document number TXC-06125-AN1, provides guidance on circuit and heat sink requirements for operation of XBERT at 622 Mbit/s.

INPUT, OUTPUT AND I/O PARAMETERS

INPUT PARAMETERS FOR TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		-70.0		µA	$V_{DD} = 5.25$
Input capacitance		3.8		pF	

Note: Input has a 72k (nominal) internal pullup resistor.

OUTPUT PARAMETERS FOR TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	3.7			V	$V_{DD} = 4.75$; $I_{OH} = -8.0$
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}	1.0	2.7	5.7	ns	$C_{LOAD} = 15$ pF
t_{FALL}	2.7	6.1	11.7	ns	$C_{LOAD} = 15$ pF

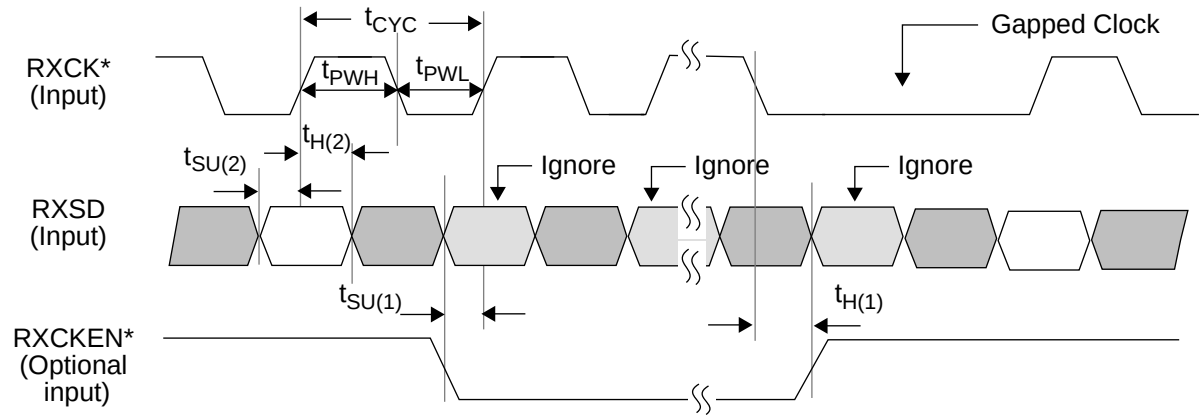
INPUT/OUTPUT PARAMETERS FOR TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		-70.0		µA	$V_{DD} = 5.25$
Input capacitance		7.1		pF	
V_{OH}	3.7			V	$V_{DD} = 4.75$; $I_{OH} = -8.0$
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}	1.1	3.3	7.3	ns	$C_{LOAD} = 15$ pF
t_{FALL}	3.1	8.0	16.0	ns	$C_{LOAD} = 15$ pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the XBERT are illustrated in Figures 4 through 11, with values of the timing intervals tabulated below each diagram. All output times are measured with a maximum 75 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals.

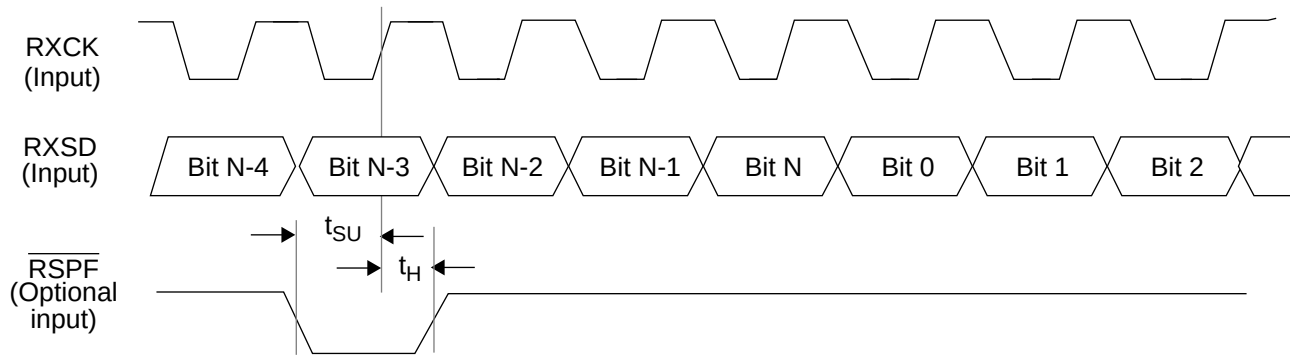
Figure 4. Receive Serial Interface Timing



* See Note in Pin Descriptions section.

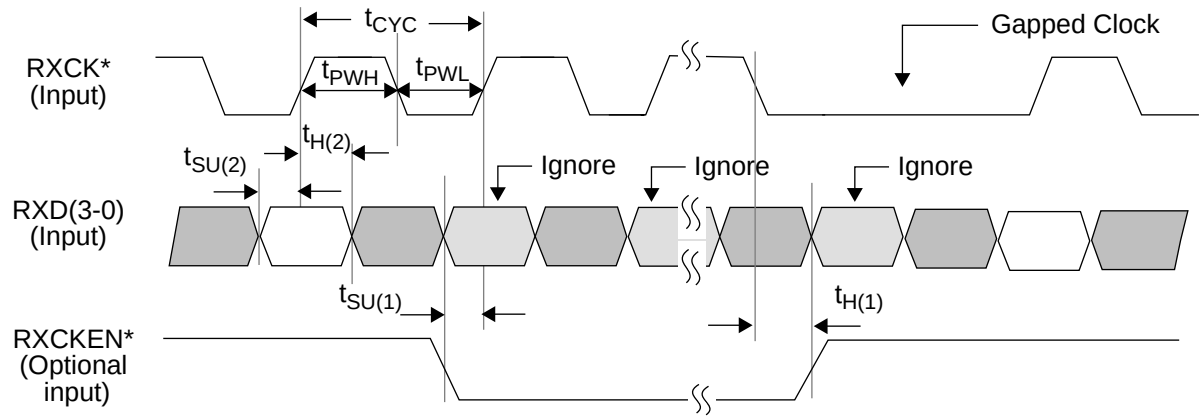
Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	t_{CYC}	12.8			ns
RXCK high time	t_{PWH}	5.4	1/2 t_{CYC}		ns
RXCK low time	t_{PWL}	5.4	1/2 t_{CYC}		ns
RXCKEN set-up time before RXCK↑	$t_{SU(1)}$	2.5			ns
RXCKEN hold time after RXCK↓	$t_{H(1)}$	2.5			ns
RXSD set-up time before RXCK↑	$t_{SU(2)}$	3.0			ns
RXSD hold time after RXCK↑	$t_{H(2)}$	3.0			ns

Note: RXCK may be gapped or stretched without the use of the RXCKEN input to accommodate overhead bit times. The set-up and hold times specified for RXCKEN must be met to ensure correct operation.



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RSPF}}$ set-up time before RXCK↑	t_{SU}	2.5			ns
$\overline{\text{RSPF}}$ hold time after RXCK↑	t_H	2.5			ns

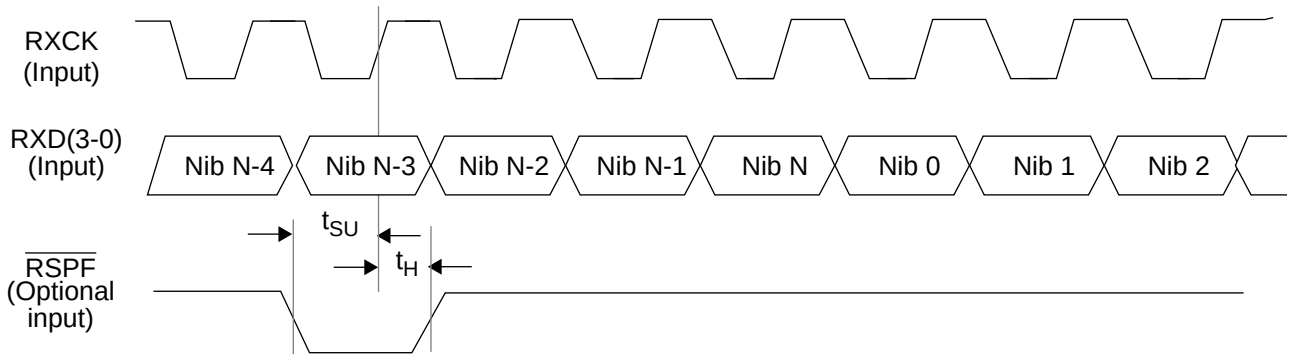
Figure 5. Receive Nibble Interface Timing



* See Note in Pin Descriptions section.

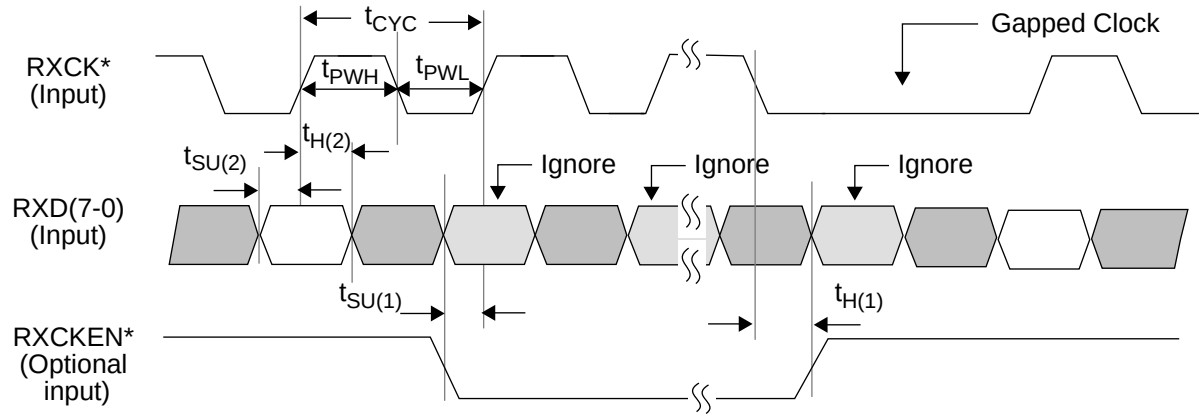
Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	t_{CYC}	12.8			ns
RXCK high time	t_{PWH}	5.4	1/2 t_{CYC}		ns
RXCK low time	t_{PWL}	5.4	1/2 t_{CYC}		ns
RXCKEN set-up time before RXCK↑	$t_{SU(1)}$	2.5			ns
RXCKEN hold time after RXCK↓	$t_{H(1)}$	2.5			ns
RXD(3-0) set-up time before RXCK↑	$t_{SU(2)}$	3.0			ns
RXD(3-0) hold time after RXCK↑	$t_{H(2)}$	3.0			ns

Note: RXCK may be gapped or stretched without the use of the RXCKEN input to accommodate overhead bit times. The set-up and hold times specified for RXCKEN must be met to ensure correct operation.



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RSPF}}$ set-up time before RXCK↑	t_{SU}	2.5			ns
$\overline{\text{RSPF}}$ hold time after RXCK↑	t_H	2.5			ns

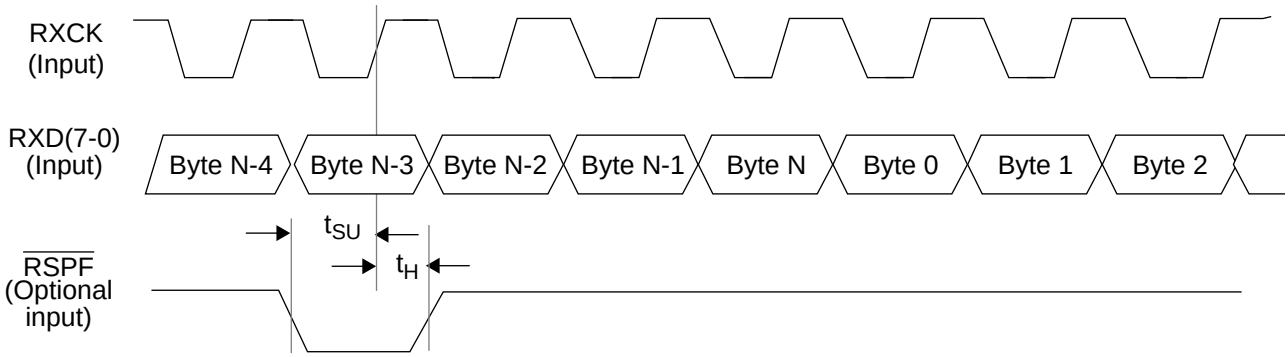
Figure 6. Receive Byte Interface Timing



* See Note in Pin Descriptions section.

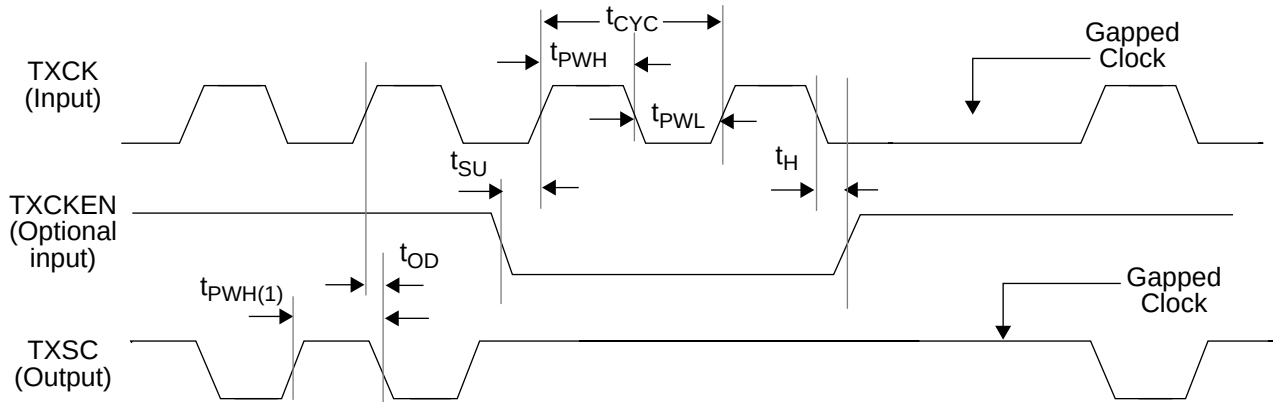
Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	t_{CYC}	12.8			ns
RXCK high time	t_{PWH}	5.4	1/2 t_{CYC}		ns
RXCK low time	t_{PWL}	5.4	1/2 t_{CYC}		ns
RXCKEN set-up time before RXCK↑	$t_{SU(1)}$	2.5			ns
RXCKEN hold time after RXCK↓	$t_{H(1)}$	2.5			ns
RXD(7-0) set-up time before RXCK↑	$t_{SU(2)}$	3.0			ns
RXD(7-0) hold time after RXCK↑	$t_{H(2)}$	3.0			ns

Note: RXCK may be gapped or stretched without the use of the RXCKEN input to accommodate overhead bit times. The set-up and hold times specified for RXCKEN must be met to ensure correct operation.



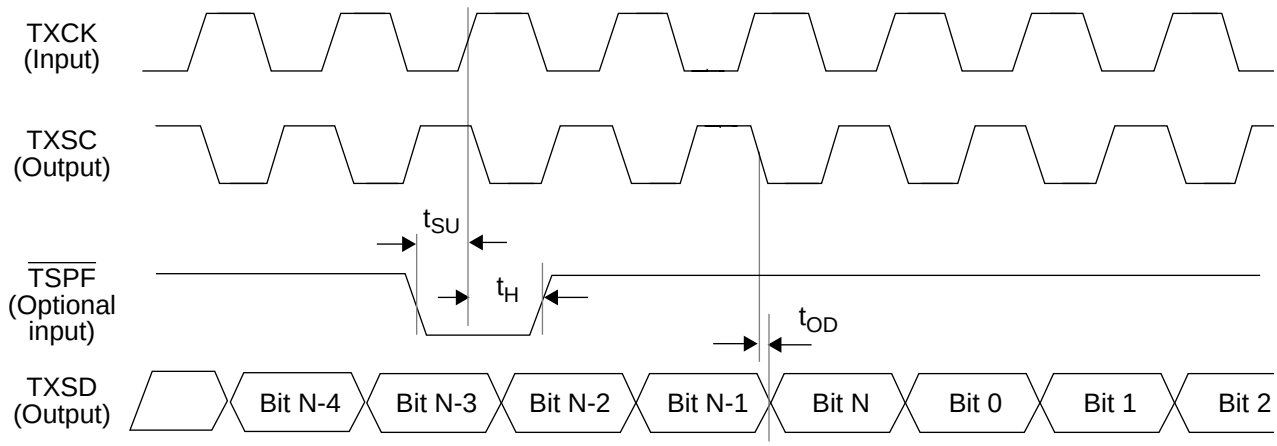
Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RSPF}}$ set-up time before RXCK↑	t_{SU}	2.5			ns
$\overline{\text{RSPF}}$ hold time after RXCK↑	t_H	2.5			ns

Figure 7. Transmit Serial Interface Timing



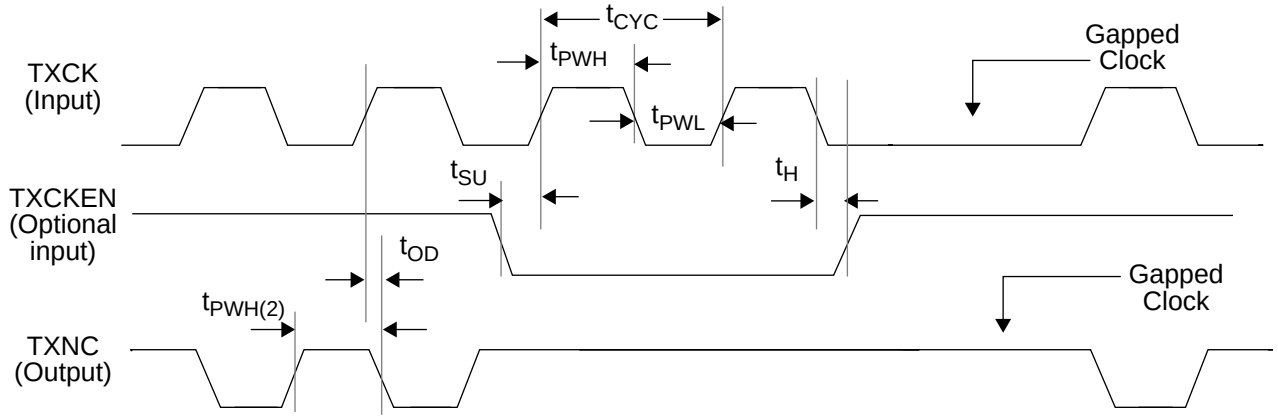
Parameter	Symbol	Min	Typ	Max	Unit
TXCK clock period	t_{CYC}	12.8			ns
TXCK high time	t_{PWH}	5.4	1/2 t_{CYC}		ns
TXCK low time	t_{PWL}	5.4	1/2 t_{CYC}		ns
TXCKEN set-up time before TXCK↑	t_{SU}	2.5			ns
TXCKEN hold time after TXCK↓	t_H	2.5			ns
TXSC output delay after TXCK↑	t_{OD}			5.0	ns
TXSC high time	$t_{PWH(1)}$	5.4			ns

Note: The clock (TXCK) may be gapped or stretched without the use of TXCKEN to accommodate overhead bit times. The set-up and hold times specified for TXCKEN must be met to ensure correct operation.



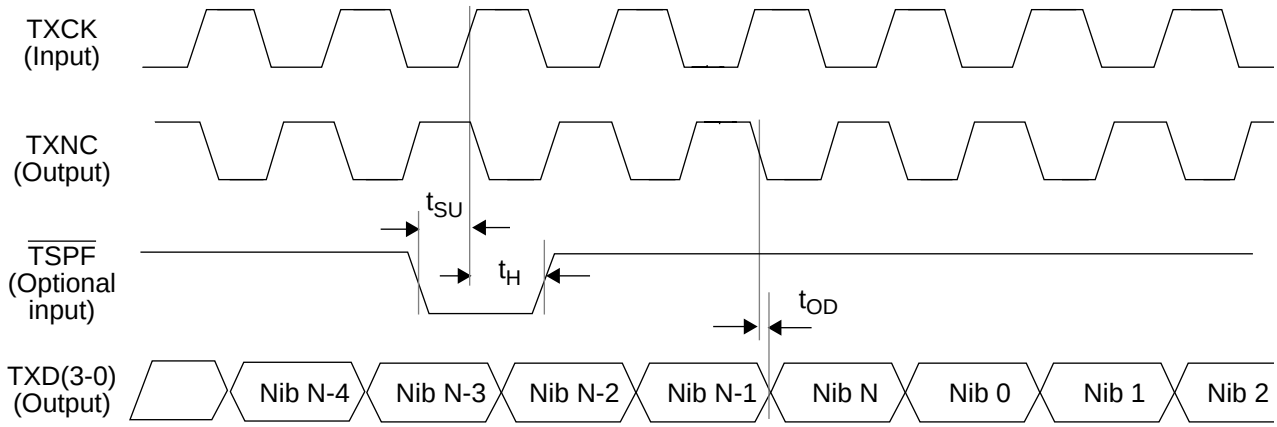
Parameter	Symbol	Min	Typ	Max	Unit
TXSD output delay after TXSC↓	t_{OD}			5.0	ns
$\overline{\text{TSPF}}$ set-up time before TXCK↑	t_{SU}	2.5			ns
$\overline{\text{TSPF}}$ hold time after TXCK↑	t_H	2.5			ns

Figure 8. Transmit Nibble Interface Timing



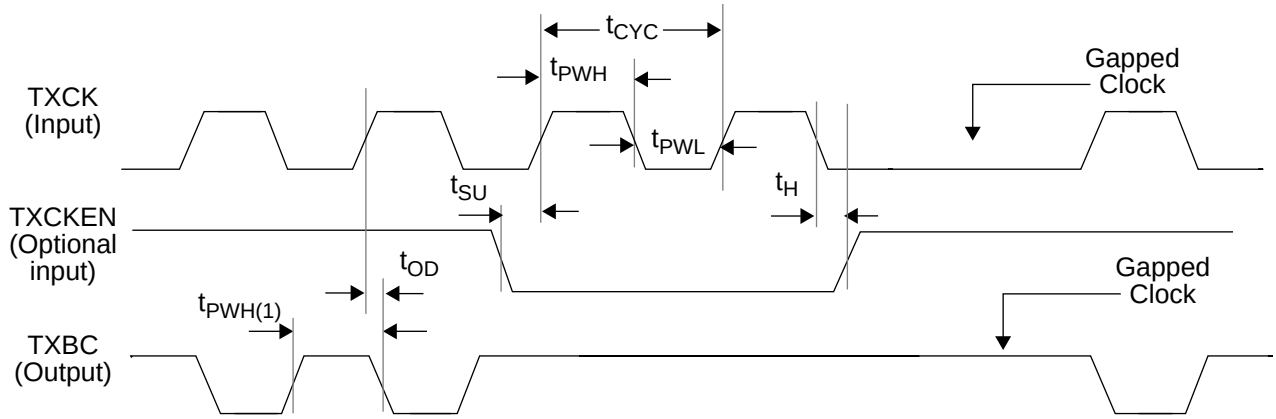
Parameter	Symbol	Min	Typ	Max	Unit
TXCK clock period	t_{CYC}	12.8			ns
TXCK high time	t_{PWH}	5.4	1/2 t_{CYC}		ns
TXCK low time	t_{PWL}	5.4	1/2 t_{CYC}		ns
TXCKEN set-up time before TXCK↑	t_{SU}	2.5			ns
TXCKEN hold time after TXCK↓	t_H	2.5			ns
TXNC output delay after TXCK↑	t_{OD}			5.0	ns
TXNC high time	$t_{PWH(1)}$	5.4			ns

Note: The clock (TXCK) may be gapped or stretched without the use of TXCKEN to accommodate overhead bit times. The set-up and hold times specified for TXCKEN must be met to ensure correct operation.



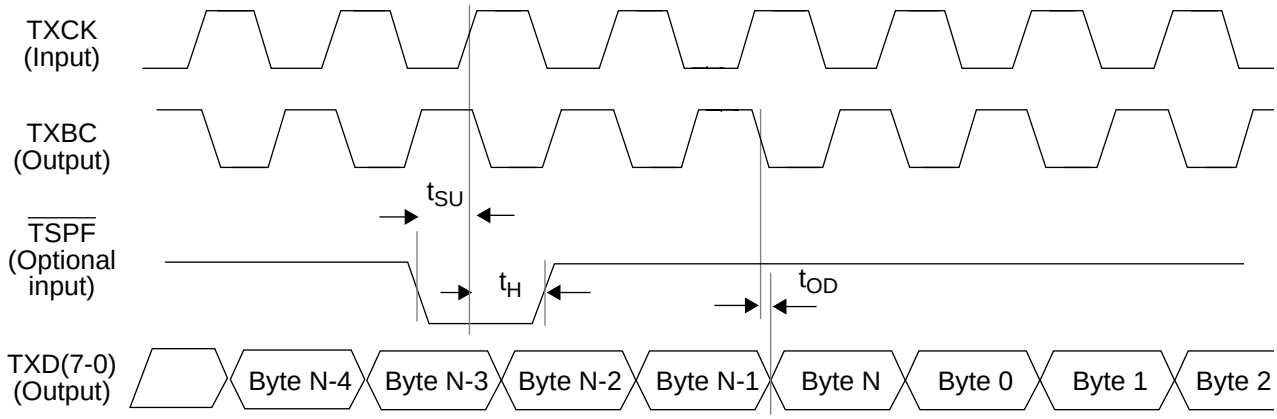
Parameter	Symbol	Min	Typ	Max	Unit
TXD output delay after TXNC↓	t_{OD}			5.0	ns
$\overline{\text{TSPF}}$ set-up time before TXCK↑	t_{SU}	2.5			ns
$\overline{\text{TSPF}}$ hold time after TXCK↑	t_H	2.5			ns

Figure 9. Transmit Byte Interface Timing



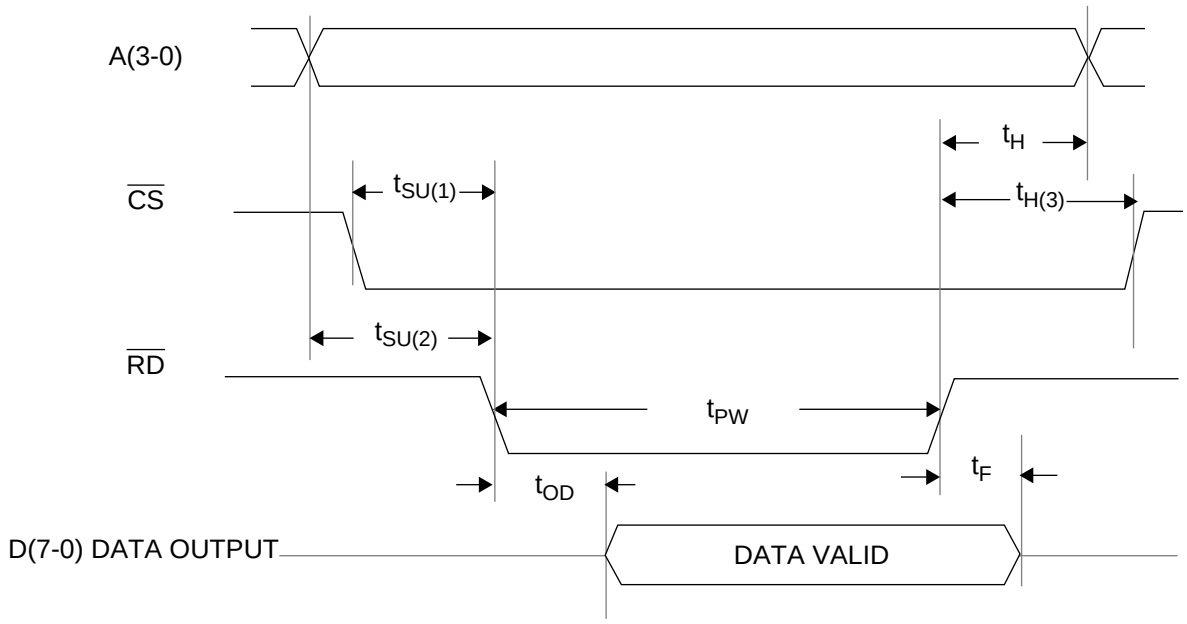
Parameter	Symbol	Min	Typ	Max	Unit
TXCK clock period	t_{CYC}	12.8			ns
TXCK high time	t_{PWH}	5.4	1/2 t_{CYC}		ns
TXCK low time	t_{PWL}	5.4	1/2 t_{CYC}		ns
TXCKEN set-up time before TXCK↑	t_{SU}	2.5			ns
TXCKEN hold time after TXCK↓	t_H	2.5			ns
TXBC output delay after TXCK↑	t_{OD}			5.0	ns
TXBC high time	$t_{PWH(1)}$	5.4			ns

Note: The clock (TXCK) may be gapped or stretched without the use of TXCKEN to accommodate overhead bit times. The set-up and hold times specified for TXCKEN must be met to ensure correct operation.



Parameter	Symbol	Min	Typ	Max	Unit
TXD output delay after TXBC↓	t_{OD}			5.0	ns
$\overline{\text{TSPF}}$ set-up time before TXCK↑	t_{SU}	2.5			ns
$\overline{\text{TSPF}}$ hold time after TXCK↑	t_H	2.5			ns

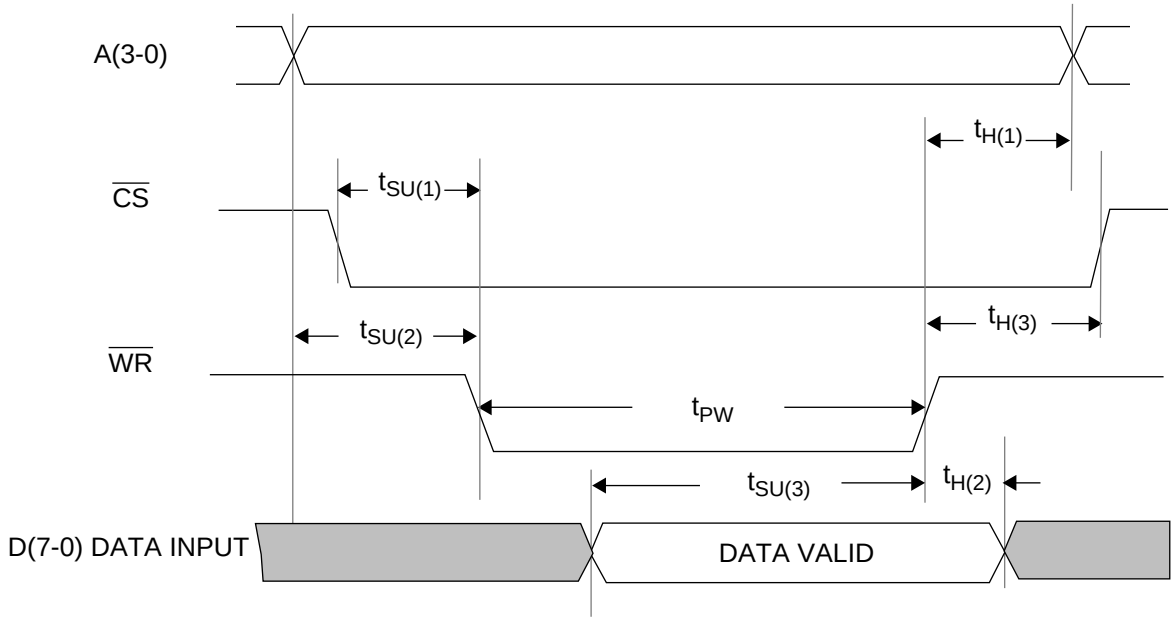
Figure 10. Microprocessor Read Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(3-0) set-up time before $\overline{RD}\downarrow$	$t_{SU(2)}$	10.0			ns
$\overline{CS}$ set-up time before $\overline{RD}\downarrow$	$t_{SU(1)}$	5.0			ns
A(3-0) hold time after $\overline{RD}\uparrow$	t_H	10.0			ns
$\overline{RD}$ pulse width	t_{PW}	38			ns
DATA output delay after $\overline{RD}\downarrow$	t_{OD}			8.0	ns
DATA float time after $\overline{RD}\uparrow$	t_F			2.0	ns
$\overline{CS}$ hold time after $\overline{RD}\uparrow$	$t_{H(3)}$	5.0			ns

Note: A minimum of 10 TXCK clock cycles must occur after power-up, before the read cycles will operate correctly.

Figure 11. Microprocessor Write Timing



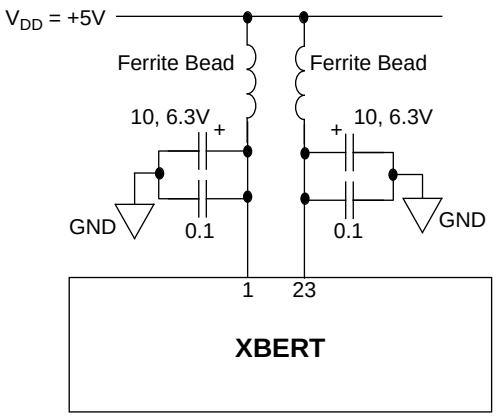
Parameter	Symbol	Min	Typ	Max	Unit
A(3-0) set-up time before $\overline{WR}\downarrow$	$t_{SU(2)}$	10.0			ns
$\overline{CS}$ set-up time before $\overline{WR}\downarrow$	$t_{SU(1)}$	5.0			ns
A(3-0) hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	10.0			ns
$\overline{WR}$ pulse width	t_{PW}	38			ns
DATA set-up time before $\overline{WR}\uparrow$	$t_{SU(3)}$	10.0			ns
DATA hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	5.0			ns
$\overline{CS}$ hold time after $\overline{WR}\uparrow$	$t_{H(3)}$	5.0			ns

Note: A minimum of 10 TXCK clock cycles must occur after power-up, before the write cycles will operate correctly.

OPERATION

DECOUPLING OF POWER SUPPLY PINS

Each of the two +5 volt power supply pins of the XBERT device, pins 1 and 23, should be decoupled using a series inductor (ferrite bead) and capacitors that are effective at both low and high frequencies, as shown in Figure 12. These external components should be placed close to the pin, especially the lower-valued RF capacitor.



Notes:
1. Fair-Rite Products Part No. 2743002111, or equivalent, should be used for each ferrite bead (Walkill, NY, 914-895-2055).
2. All capacitor values are shown in microfarads.

Figure 12. Recommended Decoupling of Power Supply Pins

EXTERNAL CIRCUIT FOR PROPER UPDATING OF BIT ERROR AND CLOCK COUNTERS

Under certain combinations of microprocessor access and telecommunications usage, the Bit Error Counter (at memory map addresses 06H, 07H and 08H) and the Clock Counter (at memory map addresses 09H, 0AH and 0BH) may not be updated correctly by the XBERT device. Since it is not possible to specify all the combinations of conditions under which this incorrect operation can occur, it is recommended that users of the XBERT device should either contact the Applications Engineering Department at TranSwitch for advice on the susceptibility of their particular applications, or avoid any potential problems in their designs by employing the external circuit and special software precautions described below.

The two 24-bit counters are specially designed to record their event counts accurately even when the counters are being read by the microprocessor. The counters latch during a microprocessor read operation, and both counters must be read together by six read cycles performed on addresses 09H (first), 0AH, 0BH, 06H, 07H and 08H (last). The final reading of address 08H starts a state machine that transfers the counts synchronously with the receive clock. This transfer occurs upon the third ungapped receive clock after the rising edge of the $\overline{RD}$ input signal applied during the address 08H read access. However, the state machine is cleared from its update sequence upon the next microprocessor initiation of active $\overline{RD}$ or $\overline{WR}$ input signals, so correct update operation requires that one of these does not occur before the update has been processed, i.e., before three clock periods have elapsed. Incorrect operation will result in a failure to update the counters, which will appear to be stuck.

This problem may avoided by employing an external circuit and special software to ensure that the XBERT does not experience an active $\overline{RD}$ or $\overline{WR}$ input during the critical period of three clock cycles. The circuit shown in Figure 13 gates the read and write lines with the XBERT's chip select input to ensure that the XBERT does not see any read or write signals intended for other devices, which may occur during the critical period (the gate in the chip select line is intended only to equalize the gate delays on all three input pins so that the microprocessor read/write cycle timing diagrams of this Data Sheet are applicable without special adjustment for differences in the relative timing between $\overline{RD}$ or $\overline{WR}$ and $\overline{CS}$). Read or write signals which are intended for the XBERT (i.e., those which are active when $\overline{CS}$ is low) must be programmed not to occur during the critical period. The hold-off time from reading address 08H to the next read or write of the group starting with address 09H must be arranged to be a minimum of:

[3 + (maximum number of successive read clock gaps)] x 1/(receive clock frequency)

For example, a T1 application requires the following hold-off time from accessing address 08H to accessing address 09H:

[3 + (1 overhead bit time)] x 1/1.544MHz = 4 x 0.666 = 2.664 microseconds (rounded up to 2.7).

.

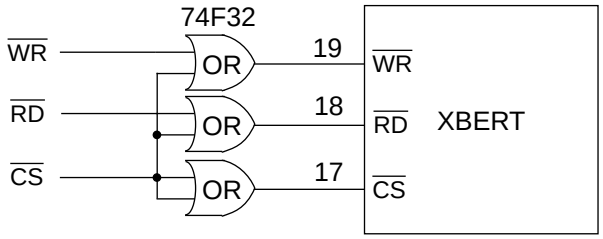


Figure 13. Protection of XBERT from Read/Write Signals Intended for other Devices

MEMORY MAP

The XBERT memory map consists of register bit positions and counters, which may be accessed by a microprocessor for read and (except for counters) write cycles. The unused bit position at bit 3 of register 01H is a "don't care" bit, but it is recommended that it should be set to 0.

Address (Hex)	Mode*	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	R/W	POLY	PROG	SEL1	SEL0	RESET	INVTD	MODE1	MODE0
01	R/W	ERR1	ERR0	SSE	RESETC	Unused	TRLBK	TEST	LOF
02	R/W	Programmable Word, Byte 4							
03	R/W	Programmable Word, Byte 3							
04	R/W	Programmable Word, Byte 2							
05	R/W	Programmable Word, Byte 1							
06	R	Bit Error Counter (MS Byte)							
07	R	Bit Error Counter (Middle Byte)							
08	R	Bit Error Counter (LS Byte)							
09	R	Clock Counter (MS Byte)							
0A	R	Clock Counter (Middle Byte)							
0B	R	Clock Counter (LS Byte)							

*Read/write (R/W); Read only (R).

MEMORY MAP DESCRIPTIONS

<table>
<tr><th>Address*</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>00</td><td>7
6
5
4</td><td>POLY
PROG
SEL1
SEL0</td><td>Test Pattern Generator and Detector: Bits 7 through 4 are used to select a test pattern according to the truth table shown below. The 2^{20} - 1 pseudo-random test pattern designator ZS stands for zero suppression. The 2^{20} - 1 with zero suppression is also defined as a QRSS signal. This test pattern is not supported in the byte mode. The test pattern is common for both generation and detection (including programmable words). For “in frame” and Loss Of Frame conditions please refer to the LOF bit description for Address 01H, bit 0.
<table>
<tr><th>Polynomial (POLY)</th><th>Program (PROG)</th><th>Select 1 (SEL1)</th><th>Select 0 (SEL0)</th><th>Test Pattern</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0000000000. . . .</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1111111111. . . .</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1010101010. . . .</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1100110011. . . .</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Byte 1 only</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Bytes 1 & 2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Bytes 1,2 &3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Bytes 1, 2, 3 & 4</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>2^{15} - 1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>2^{20} - 1(ZS)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>2^{20} - 1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>2^{23} - 1</td></tr>
</table></td></tr>
<tr><td></td><td>3</td><td>RESET</td><td>Reset XBERT: A global reset occurs when a one is written to this bit position. This must be followed by writing a zero into this location. Reset clears the internal counters, generators, and detectors, as well as the control bits and performance counters in the memory map. All R/W memory map bit positions must be set to their desired values after a reset.</td></tr>
<tr><td></td><td>2</td><td>INVTD</td><td>Invert Transmit Data: A one written into this position causes the data to be inverted for transmission. The data is inverted for the bit-serial, nibble-parallel, and byte-parallel interfaces.</td></tr>
<tr><td></td><td>1
0</td><td>MODE1
MODE0</td><td>XBERT Interface Selection: The XBERT transmit and receive interface is selected according to the following table:
<table>
<tr><th>MODE1</th><th>MODE0</th><th>Interface Selected</th></tr>
<tr><td>0</td><td>0</td><td>Bit-serial</td></tr>
<tr><td>0</td><td>1</td><td>Nibble-parallel</td></tr>
<tr><td>1</td><td>1</td><td>Byte-parallel</td></tr>
</table></td></tr>
</table>

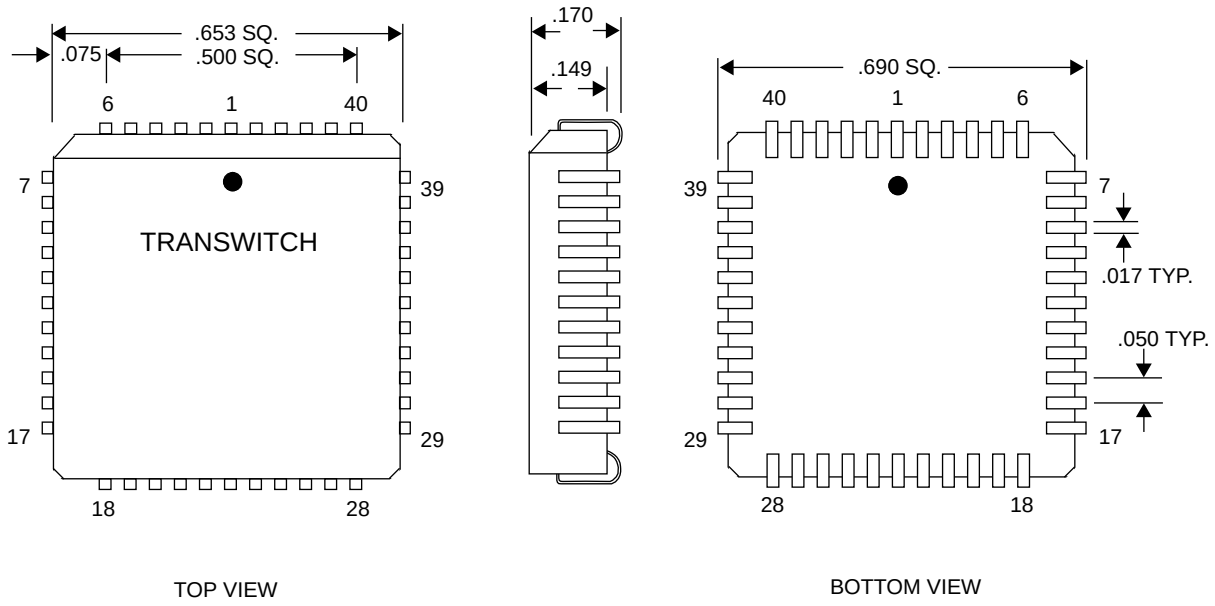
* Note: All addresses are shown in hexadecimal form.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>01</td><td>7
6</td><td>ERR1
ERR0</td><td>Transmit Error Rate: These two bits control the generation of the fixed bit error rates given in the table below. For example, a $10E^{-3}$ error rate results in the XBERT transmitting one bit in a thousand in error. The error is generated by inverting a single bit in the bit pattern. The error rate generation is independent of the pattern selected (pseudo-random, fixed word, or programmable).
<table>
<tr><th>ERR1</th><th>ERR0</th><th>Error Rate</th></tr>
<tr><td>0</td><td>0</td><td>No errors</td></tr>
<tr><td>0</td><td>1</td><td>10^{-3} error rate</td></tr>
<tr><td>1</td><td>0</td><td>10^{-6} error rate</td></tr>
</table></td></tr>
<tr><td></td><td>5</td><td>SSE</td><td>Send Single Error: A single bit error is transmitted by writing a one into this bit position. The error is sent in the next bit time after being written. After sending the single error, the bit is reset by the XBERT. The microprocessor must write a one in order to send another single bit error.</td></tr>
<tr><td></td><td>4</td><td>RESETC</td><td>Reset Performance Counters: A one causes the bit error counter (locations 06H, 07H, and 08H) and the clock counter (locations 09H, 0AH, and 0BH) to be reset to 0. XBERT resets this bit after the performance counters have been reset. This bit does not affect registers 00H through 05H.</td></tr>
<tr><td></td><td>3</td><td></td><td>Unused.</td></tr>
<tr><td></td><td>2</td><td>TRLBK</td><td>Transmit-to-Receive (TR) Loopback: A one activates the transmit-to-receive loopback testing feature. Data is transmitted and is also looped back as receive data. The receive data input is disabled.</td></tr>
<tr><td></td><td>1</td><td>TEST</td><td>TranSwitch Test: A zero must be written into this bit position.</td></tr>
<tr><td></td><td>0</td><td>LOF</td><td>Loss of Frame: An “in frame” condition for any fixed word pattern (e.g., 1100, 1010) occurs when two consecutive error-free 4-bit patterns are received. Loss of frame occurs when three consecutive 4-bit patterns are received in error or when 30 or more bits in a block of 1000 consecutive bits are in error.
An “in frame” condition for any programmable word occurs when two consecutive error-free word patterns are received. The programmable word pattern can vary from 1 to 4 words, which equates to 2 to 8 words before an “in frame” condition can occur. Loss of frame occurs when three consecutive word patterns are received in error or when 30 or more bits in a block of 1000 consecutive bits are in error.
An “in frame” condition for any PRBS pattern occurs when the start of frame pulse sequence is received. The length of the start of frame pulse sequence equals the exponent number of the PRBS pattern. Therefore, a 2^{23-1} PRBS pattern has a 23 consecutive ones sequence for its start of frame pulse sequence and a 2^{15-1} PRBS pattern has a 15 consecutive ones sequence. If the $\overline{\text{TSPF}}$ and $\overline{\text{RSPF}}$ pins are activated, the PRBS pattern will reset and begin with a start of frame pulse sequence, which will be detected with minimum delay. Loss of frame occurs when 30 or more bits in a block of 1000 consecutive bits are in error.
For all word patterns and PRBS sequences, the clock counter maintains its functionality during a LOF condition and the bit error counter is disabled.</td></tr>
</table>

Address	Bit	Symbol	Description
02	7-0		**Programmable Word, Byte 4:** The XBERT provides four register locations (02H, 03H, 04H, and 05H) for four bytes of programmable test word pattern. The actual number of bytes that comprise the test word pattern (1-4) is selected by bits 7-4 in the 00H register location. The word is transmitted with byte 1 sent last. Bit 7 in each byte is its most significant bit and the first bit transmitted. Bit 0 in byte 1 is the last bit transmitted in the test word sequence. For example, the test sequence for a four-byte test word pattern bounded by bits MSB and LSB is shown below: Byte 4 Byte 3 Byte 2 Byte 1 Byte 4 ← MSBXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXLSB MSBXXXXXXX Bit 7 0 7 0 7 0 7 0 7 0 For a single-byte test word, only byte 1 is used. The receive detector checks the incoming data for frame alignment by comparing it with the programmed test word pattern.
03	7-0		**Programmable Word, Byte 3:** See Address 02H.
04	7-0		**Programmable Word, Byte 2:** See Address 02H.
05	7-0		**Programmable Word, Byte 1:** See Address 02H.
06 07 08	7-0		**Bit Error Counter:** Register locations 06H, 07H, and 08H provide a total count of the number of bit errors that have occurred for the three interface modes. Multiple errors in a single nibble or byte are counted separately. The counter is enabled after frame alignment occurs for the test pattern selected. Bit 7 in address 06H is the most significant bit, while bit 0 in address 08H is the least significant bit. The counter is non-saturating and will roll-over to zero when it becomes full. To ensure that no counts are lost, all clock counter registers plus all bit error counter registers must be read together in the following order: 09H, 0AH, 0BH, 06H, 07H, 08H. They will all be simultaneously latched when register 08H is read last. If the counter registers are always read in the same order, then no counts will be lost. The counter is cleared by writing a one to bit 4 (RESETC) in address 01H, or through a global reset (bit 3 in address 00H).
09 0A 0B	7-0		**Clock Counter:** Register locations 09H, 0AH, and 0BH provide a total count of the number of clock pulses that have been received. When XBERT is in serial mode, the clock counter provides a count of the total number of received data bits. When XBERT is in nibble-parallel or byte-parallel mode, the clock counter indicates the number of received nibbles or bytes, respectively. The counter is enabled upon power-up. Events are counted even during a LOF condition. Bit 7 in address 09H is the most significant bit, while bit 0 in address 0BH is the least significant bit. The counter is non-saturating and will roll-over to zero when it becomes full. It takes approximately 0.32 seconds for the counter to roll-over for a 51.84 Mbit/s bit-serial signal. To ensure that no counts are lost, all clock counter registers plus all bit error counter registers must be read together in the following order: 09H, 0AH, 0BH, 06H, 07H, 08H. They will all be simultaneously latched when register 08H is read last. If the counter registers are always read in the same order, then no counts will be lost. The counter is cleared by writing a one to bit 4 (RESETC) in address 01H, or through a global reset (bit 3 in address 00H).

PACKAGE INFORMATION

The XBERT is available in a 44-pin plastic leaded chip carrier as illustrated in Figure 14.



Note: All dimension values are shown in inches and are nominal unless otherwise indicated.

Figure 14. XBERT TXC-06125 44-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

Part Number: TXC-06125-ACPL 44-pin plastic leaded chip carrier

RELATED PRODUCTS

TXC-02020, ART VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ART performs the transmit and receive line interface functions required for transmission of STS-1 (51.840 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02021, ARTE VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ARTE has the same functionality as ART, plus expanded features.

TXC-02050, MRT Multi-Rate Line Interface VLSI Device. The MRT provides the functions for terminating ITU-specified 8448 kbit/s (E2) and 34368 kbit/s (E3) line rate signals, or 6312 kbit/s (JT2) line signals specified in the Japanese NTT Technical Reference for High Speed Digital Leased Circuits. An optional HDB3 codec is provided for the two ITU line rates.

TXC-02623, STAF VLSI Device (SONET/SDH Transceiver and Framer). The STAF is a 622/155.5 Mbit/s device that combines multiplexing, demultiplexing, SONET/SDH framing, clock synthesis PLL and loopback functions in a single chip.

TXC-02624, CDR VLSI Device (SONET/SDH Clock and Data Recovery). The CDR is a 622 Mbit/s monolithic clock and data recovery component that receives NRZ data, extracts the high-speed clock, and presents the separated data and clock as its outputs.

TXC-03301, M13 VLSI Device (DS3/DS1 Mux/Demux). This single-chip multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals.

TXC-03303, M13E VLSI Device, Extended feature version of the TXC-03301 (M13).

TXC-03401, DS3F VLSI Device (DS3 Framer). Maps broadband payloads into the DS3 frame format. Operates in either the C-bit parity or M13 operating modes.

TXC-03701 E2/E3F Framer VLSI device. The E2/E3 Framer directly interfaces with the MRT and provides multi-mode framing for ITU-T Rec. G.751/G.753 (34368 kbit/s) or ITU-T Rec. G.742/G.745 (8448 kbit/s) signals.

TXC-03702 JT2F Framer VLSI device. The JT2F Framer directly interfaces with the MRT and provides framing for ITU-T Rec. G.704 (6312 kbit/s) signals.

TXC-20153D, DS3/STS-1 Line Interface Module (DS3LIM-SN). Complete and compact analog to digital interface serving B3ZS encoded DS3 signals.

TXC-21075, XBERT Evaluation Board. A complete, ready-to-use board that demonstrates the functions and features of the XBERT VLSI device.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

IEEE (U.S.A.)

The Institute of Electrical and Electronics Engineers, Inc.
Customer Service Department
445 Hoes Lane
P. O. Box 1331
Piscataway, NJ 08855-1331
Tel: 800-701-4333 (In U.S.A.)
Tel: 908-981-0060
Fax: 908-981-9667

ITU-TSS (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (TSS)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated XBERT Data Sheet that have technical differences relative to the previous and now superseded XBERT Data Sheet:

Updated XBERT Data Sheet: Edition 3, August 1995

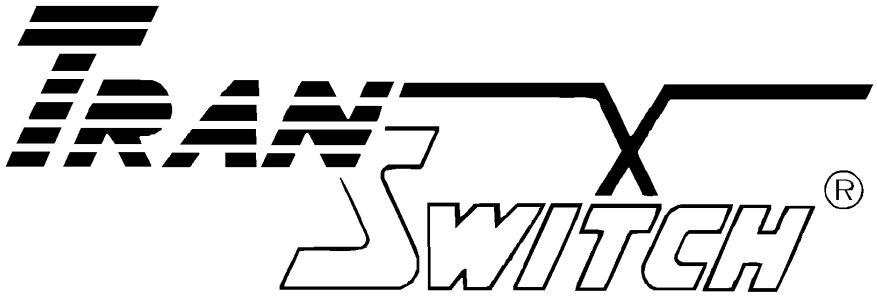
Superseded XBERT Data Sheet: Edition 2, August 1992

The page numbers indicated below of this updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed Document status by deleting Preliminary.
1	Changed edition number and date.
1	Made changes to Features list.
1	Made changes to Description list.
1	Made minor clarifications to the figure.
2-33	Added edition number and date to the bottom.
2	Added Table of Contents and List of Figures.
3	Made changes to Figure 1.
3-4	Made changes to Block Diagram Description section.
5-7	Changed $\overline{\text{RSF}}$ to $\overline{\text{RSPF}}$ and $\overline{\text{TSF}}$ to $\overline{\text{TSPF}}$.
5	Made changes to Figure 2.
5	Made changes to Name/Function column for GND.
6	Made changes to Name/Function column for RXSD/RXD0, RXD3, RXD7 and $\overline{\text{RSPF}}$.
6	Added notes to the bottom to explain Type column heading and to indicate restrictions on the use of RXCK and RXCKEN inputs to disable data input.
7	Made changes to Name/Function column for TXCK, TXSD/TXD0, TXD3, TXD7 and $\overline{\text{TSPF}}$.
8	Made changes to Name/Function column for D(7-0) and A(3-0).
9	Changed Max for P_C row and modified the second note to Absolute Maximum Ratings section.
9	Added Test Conditions to Thermal Characteristics table.
9	Deleted Typ and added Max to Thermal resistance - junction to case.
9	Modified the note under Power Requirements table.
10	Modified Figure 3.
11	Input Parameters For TTLp: changed Typ for input capacitance.

Page Number of Updated Data Sheet	Summary of the Change
11	Output Parameters For TTL8mA: changed Min, Typ and Max for t_{RISE} and t_{FALL}.
11	Input/Output Parameters For TTL8mA: changed Type for input capacitance and changed Min, Typ and Max for t_{RISE} and t_{FALL}.
12-17	In Figures 4-9, changed timing parameters to correspond to highest clock frequency of 78 MHz instead of 52 MHz. Added note to timing diagrams in Figures 4-6.
18-19	Added last row and a note to the table.
20-21	Changed Operation section.
22	Made changes to Memory Map section
23-25	Made changes to Memory Map Descriptions section.
26	Made minor changes to Package Information section.
27	Changed Ordering Information and Related Products sections.
28	Added Standards Documentation Sources section.
29-30	Added List of Data Sheet Changes section.
33	Added Documentation Update Registration Form.

- NOTES -



TranSwitch VLSI:
Powering Communication Innovation

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DOCUMENTATION UPDATE REGISTRATION FORM

If you would like be added to our database of customers who have registered to receive updated documentation for this device as it becomes available, please provide your name and address below, and fax or mail this page to Mary Koch at TranSwitch. Mary will ensure that relevant Product Information Sheets, Data Sheets, Application Notes and Technical Bulletins are sent to you.

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Please describe briefly your intended application for this device, and indicate whether you would care to have a TranSwitch applications engineer contact you to provide assistance:

_____

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Please fax this page to Mary Koch at (203) 926-9453 or fold, tape and mail it (see other side)

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