TRANSWITCH®

L3M Device
Level 3 Mapper
TXC-03452B

DATA SHEET

FEATURES

- Maps DS3 (44.736 Mbit/s) or E3 (34.368 Mbit/s) line formats into SDH/SONET formats as follows:
  - DS3 to/from STM-1/TUG-3
  - DS3 to/from STS-3/STS-1 SPE or STS-1 SPE
  - E3 to/from STM-1/TUG-3 only
- SDH/SONET bus access:
  - Drop/add data byte access (with clock, C1J1, SPE, and parity)
  - Add bus interface timing derived from drop bus, add bus, or external timing
- Path overhead byte processing:
  - Microprocessor or external interface
  - B3 generation and detection with test mask
  - B3 performance counter (16-bit) and block error counter (8-bit)
  - C2 mismatch and unequipped detection
  - G1 processing
  - FEBE count by block or bits (16-bit counter)
- Microprocessor access:
  - Motorola or Intel compatible (selected via a lead)
  - Hardware/software interrupt capability
- Line Interface
  - Transmit and receive NRZ or rail operation with split operation capability
- Testing functions:
  - SONET, facility, or line loopback
  - Transmit and receive 2^{15}-1 or 2^{23}-1 generators and shared analyzer
  - Boundary scan capability (IEEE 1149.1)
- 144-lead plastic quad flat package (PQFP) or 208-lead plastic ball grid array package (PBGA)

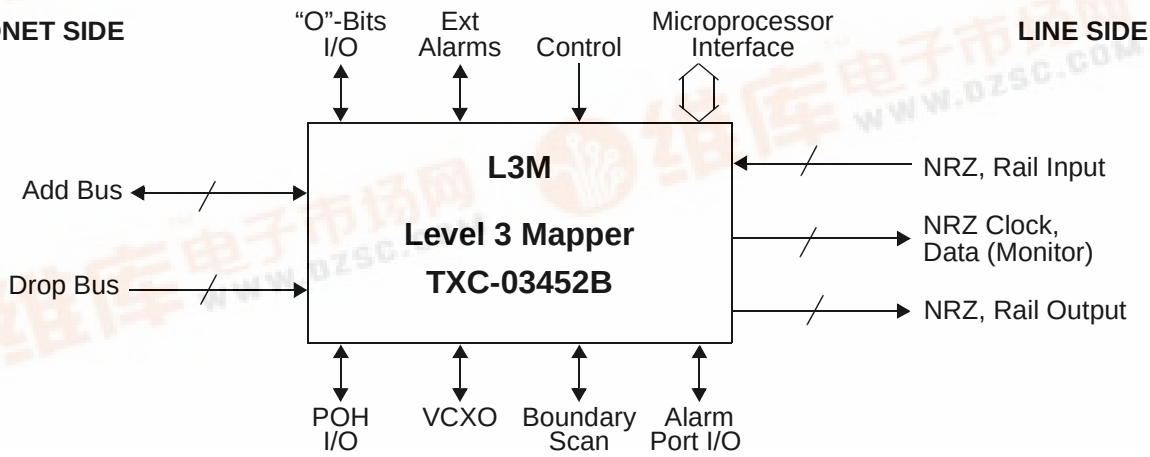
DESCRIPTION

The L3M maps a DS3 line signal into an STM-1 TUG-3 or STS-3/STS-1 SPE or STS-1 SPE SDH/SONET signal. An E3 line signal is mapped into an STM-1 TUG-3 signal only. The L3M provides a TUG-3 formatted signal for STM-1 operation, or an STS SPE for STS-3 or STS-1 operation. The SDH/SONET signal is transmitted via an add bus with timing derived from the drop side, add side or from external timing (STS-1 only). An option is provided to generate the A1, A2 framing pattern, C1 byte and H1, H2 pointer towards the add bus when external timing mode is selected.

Individual POH bytes for the transmitted SDH/SONET signal are mapped from the L3M memory map or an external interface. An option is provided to generate an unequipped status or TUG-3 path AIS signal. External accesses are provided for the communications channel "O"-bits and alarms for ring operation. The received signal is desynchronized from drop bus STM-1/TUG-3, STS-3/STS-1 SPE, or STS-1 signals. Internal pointer processing is performed for the TUG-3 signal. All POH bytes are provided for the microprocessor.

APPLICATIONS

- Add/drop multiplexers
- Digital cross-connect systems
- Broadband switching systems
- Transmission equipment



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* Please note that TranSwitch provides documentation for all of its products. Current editions of many documents are available from the Products page of the TranSwitch Website at www.transwitch.com. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

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BLOCK DIAGRAM

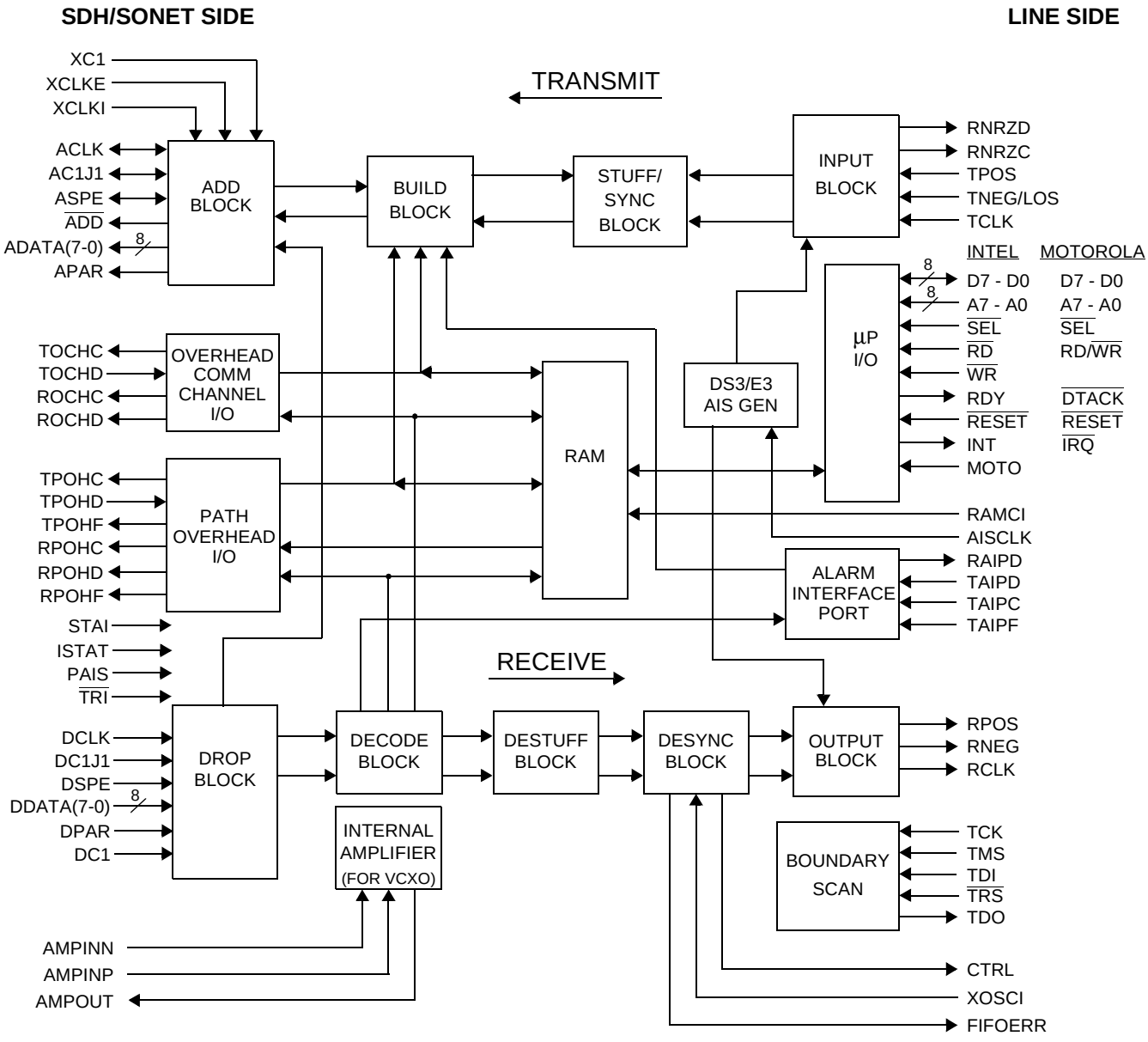
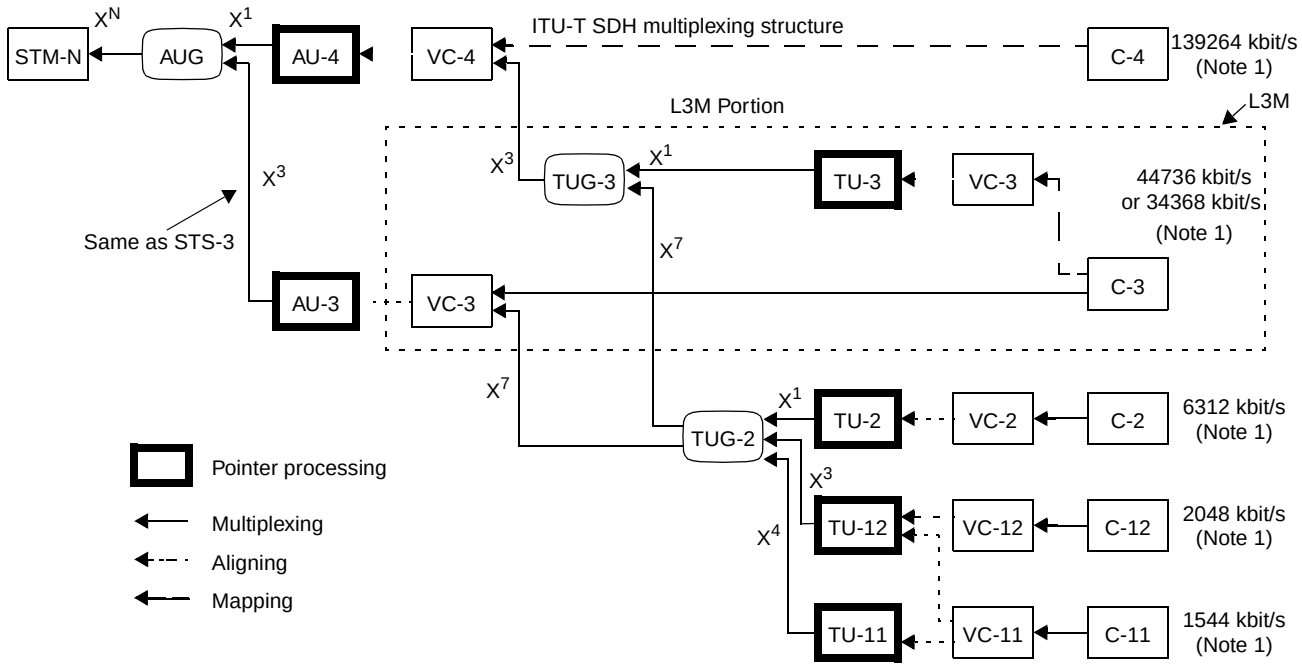


Figure 1. L3M TXC-03452B Block Diagram

BLOCK DIAGRAM DESCRIPTION

Transmit And Receive Paths, Overhead Communications, Alarms And Control

A simplified block diagram of the L3M device is shown in Figure 1. The portion of the ITU-T SDH multiplexing structure implemented by the L3M device is shown in Figure 2. In the Transmit direction, positive/negative (P/N) rail data and clock input signals, or NRZ data and clock input signals, operating at 44.736 Mbit/s (DS3) or 34.368 Mbit/s (E3), are connected to the Input Block. The transmit line input consists of positive rail/NRZ signal lead (TPOS), negative rail signal lead (TNEG), and input clock (TCLK). A control bit is provided in software that inverts the clock signal if required. The Input Block performs either an HDB3 or B3ZS decoder function if the input line termination is a rail signal. Separate NRZ data (RNRZD) and clock (RNRZC) output signals are provided for external performance monitoring circuits. Illegal coding violations are counted in a 16-bit performance counter. When the line termination is NRZ, the negative rail signal lead (TNEG) can be used to clock in an external loss of signal indication. The transmit signal and clock are both monitored for operation, and alarms are reported for failure conditions. Control bits are provided that enable the L3M device to send a line AIS when either signal or clock failure is detected. The Input Block also monitors the line signal for an E3 AIS and it has a 2^{15}-1 or 2^{23}-1 pseudo-random binary sequence (PRBS) test generator for testing.



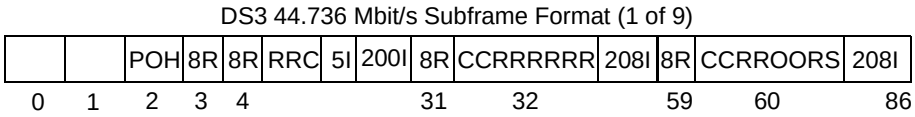
Note 1: G.702 tributaries associated with containers C-x are shown. Other signals (e.g., ATM) can also be accommodated.

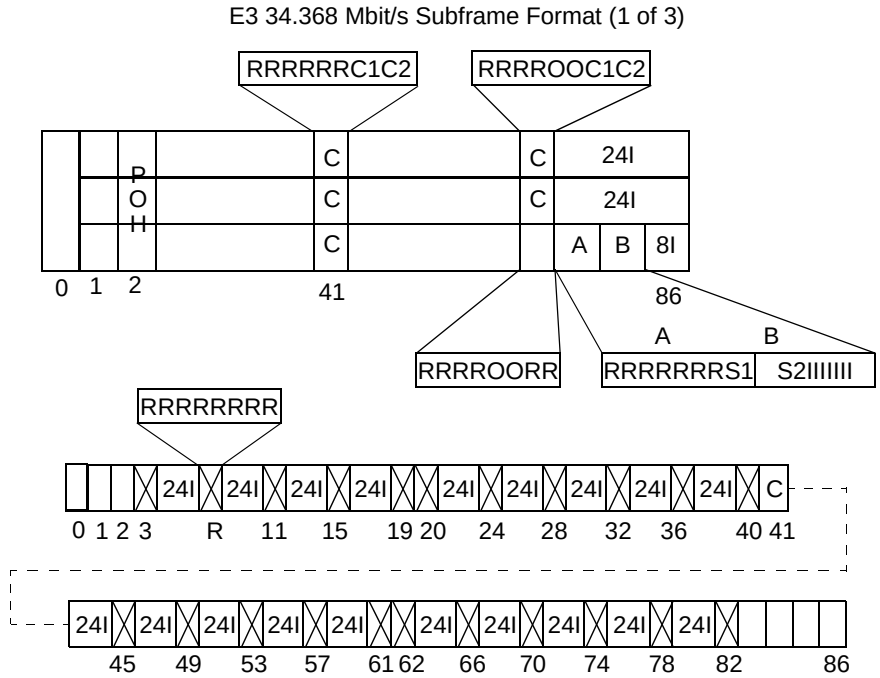
Figure 2. L3M Multiplexing Structure

The Stuff/Sync Block and Build Blocks work together for mapping a DS3 signal into a TUG-3 or STS-1 SPE or an E3 signal into a TUG-3. The mapped formats are shown in Figures 3 and 4. The stuffing algorithm for the DS3 signal format uses one set of five control bits (C-bits) with one stuff opportunity bit (S-bit) for frequency justification, per subframe (9 subframes). The E3 format uses five pairs of control bits (C1, C2 bits) to control two stuff opportunity bits (S1 and S2) per subframe (one subframe per three rows for a total of three subframes per frame). A read clock and timing indications are given by the Build Block for reading the transmit FIFO. A FIFO overflow or underflow alarm indication is provided. Should an underflow/overflow condition occur, the FIFO is immediately reset to the start-up preset value. The transmit FIFO also tracks the incoming line signal that can have an average frequency error as high as +/- 20 ppm, and simultaneously accepts this signal with up to 5 UI Peak-to-Peak jitter (where UI = 1/f).

The Build Block, with signals exchanged between itself and the Stuff/Sync Block, constructs one of two 87 column by 9 row formats: an ITU-TSS TUG-3 signal (Figure 3) or a SONET STS-1 (for STS-3) signal (Figure 4). The L3M generates a stuff byte in column 0 when control bit NOPOH is set to 0, to fill out the 87 columns of the SPE such that three L3M devices will provide inputs for a VC-4 of 261 columns, as shown in Figure 2. This column position is overwritten with the VC-4 POH when the device is mapped into the first TUG-3, while fixed stuff is used for the second and third TUG-3s. A fixed pointer value of 6800H is used as the initial value when building a TUG-3 format. There are two levels of pointer movements in TUG-3 mapping. When the TUG-3 mode is selected in drop timing mode, the transmit TUG-3 pointer value will change when there is a receive STM-1 AU-4 pointer increment or decrement. However, this feature may be disabled. Pointer movements on the STM-1 bus, which are detected using the C1J1 and SPE bus signals, are compensated by creating a TUG-3 pointer movement in the opposite direction. An “O”-bit serial interface, or two bits in RAM, are used for mapping the two “O”-bits into the DS3 SONET format subframes. The “O”-bit interface consists of an output clock (TOCHC) and an input data lead (TOCHD). The nine Path Overhead bytes are mapped individually into the SONET format from either the POH interface (except the B3 byte), from microprocessor-written RAM positions, or from internal logic (such as the path RDI state in bit 5 of G1). The POH interface consists of an output clock (TPOHC), a framing pulse (TPOHF) and an input data lead (TPOHD). A control bit enables the POH interface bytes to be written into RAM when transmitted. Enable bits are provided for controlling the FEBE and path RDI states as a result of local alarms or remote status information received during ring operation. A B3 test mask or fixed byte can also be transmitted. Control bits are provided for generating a TUG-3 path AIS, or an unequipped status condition (payload and POH bytes are equal to zero). An alarm interface provides FEBE and path RDI (FERF) input indications from a mate L3M device for ring operation. The alarm interface leads consist of input data (TAIPD), framing pulse (TAIPF), and clock signal (TAIPC).

The Add Block uses an external byte rate clock signal (XCLKI), or the Add or Drop bus clock and the SPE and C1J1 timing signals, for building and adding a TUG-3, STS-3/STS-1 SPE, or STS-1 SPE to the Add bus. The Add Block supports the STM-1/STS-3 bus signaling rate of 19.44 MHz and the STS-1 signaling rate of 6.48 MHz. The external clock is enabled by placing a high on the external clock enable lead (XCLKE), and is intended for STS-1 operation. The external clock generates the Add bus clock (ACLK), C1J1 indication (AC1J1), and SPE indication (ASPE). The output data to the bus is 3-state, active true. A software control bit enables the transport overhead A1, A2, C1, and H1/H2 bytes to be generated. The H1 and H2 bytes will carry the value of 6000H and the C1 byte carries the value of 01H. An optional C1 signal (XC1 signal lead) can be applied to the L3M device to align the start of the frame (A1, A2 bytes).





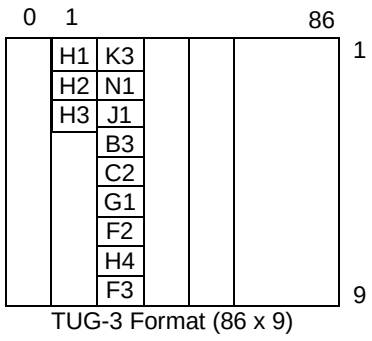


Figure 3. ITU-TSS TUG-3 Build Format

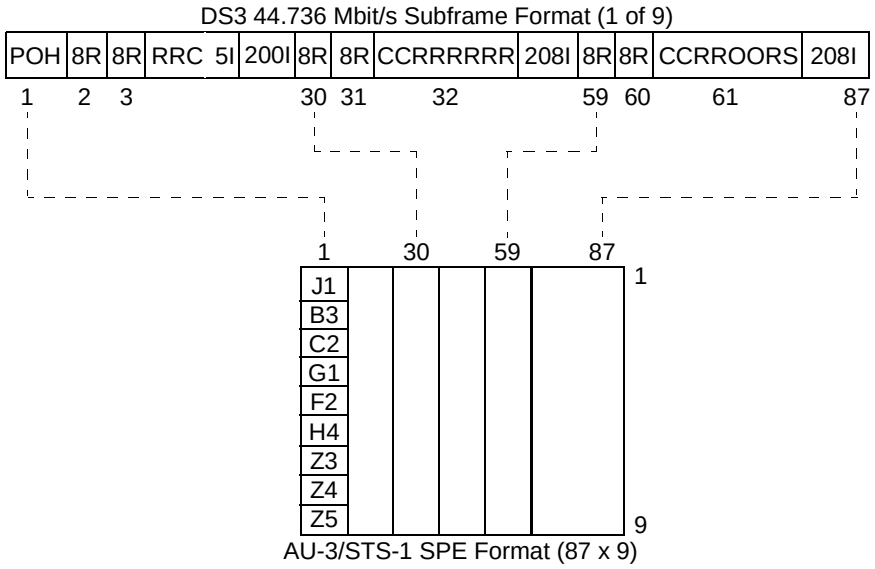


Figure 4. SONET AU-3/STS-1 SPE Build Format

When Add bus timing is selected, the clock (ACLK), C1J1 indication (AC1J1), and SPE indication (ASPE) become input signals from the Add bus. When Drop timing is selected, the L3M device supports DC1J1 pointer movements on the Drop bus, and adjusts the pointer value in the TUG-3s accordingly. An active low Add indicator ($\overline{\text{ADD}}$) is also provided to indicate the location of all time slots that are added to the bus by the L3M device (e.g., TUG-3 A, B or C). In TUG-3 mode, the VC-4 path overhead bytes are optionally sent as output to the bus when control bit NOPOH (Address CA, Bit 5) is set to 0. The selected clock is monitored for operation, and an odd parity signal (APAR) is calculated for the bus data, including the SPE and C1J1 signals when these signals are outputs (i.e., in external timing mode).

The Drop Block supports the STM-1/STS-3 bus signaling rate of 19.44 MHz and the STS-1 signaling rate of 6.48 MHz. The Drop Block uses the clock (DCLK), C1J1 indication (DC1J1) and a separate DC1 signal if required, and SPE indication (DSPE) from a Drop bus for determining the location of the Path Overhead J1 byte in the VC-4, the three J1 bytes in the three STS-1 SPEs in the STS-3 signal, and the single SPE for STS-1 operation. The C1 pulse is required, and is synchronous with the first C1 byte in the STM-1 Section Overhead bytes, or in the STS-3 or STS-1 Transport Overhead Bytes. The C1 pulse provides a framing indication for determining the location of the bytes corresponding to the TUG-3 or STS-1 selected, and is also used by the desynchronizer as a frame reference. The C1 pulse can be present in the DC1J1 signal or provided as a separate signal (DC1). The Drop SPE (DSPE) is active during the POH and payload byte times. The Drop Bus clock and composite C1J1 signal are monitored for operation, and odd parity is calculated and compared against the incoming parity bit.

The Decode Block contains the logic for performing pointer interpretation and tracking for the selected TUG-3 signal, removing the Path Overhead bytes and Overhead Communication bits, and detecting the E1 byte for an upstream AIS detection. The E1 byte carries an AIS indication from an associated TranSwitch SOT-3 or SOT-1 device. The SOT-3 or SOT-1 generates an AIS signal in one E1 byte for TUG-3 mode, or in each of the three E1 bytes for the three STS-1s, when a loss of frame, loss of pointer, loss of signal, or line AIS is detected. This indication is used by the L3M device to generate a Path RDI indication, and for generating a received DS3 or E3 AIS. In place of the E1 byte AIS, the L3M device also supports an alarm indication provided on the ISTAT and PAIS signal leads. The TUG-3 pointer is monitored for loss of pointer, New Data Flag, and Path AIS. Performance counters are provided for monitoring pointer movements. All POH bytes are written into RAM locations and are also provided at the POH interface. The POH interface consists of an output data lead (RPOHD),

framing pulse (RPOHF), and clock signal (RPOHC). The L3M device also provides a microprocessor-written location for performing C2 mismatch detection, and unequipped detection based on ANSI and ITU-TSS standards. The received "O"-bits are available at an external interface and a 2-bit RAM location for these bits is updated each frame. The "O"-bit interface consists of a data lead (ROCHD) and clock signal (ROCHC). An alarm indication port is provided for ring operation. The alarm indication port consists of a data lead (RAIPD), which is used with the POH interface framing pulse (RPOHF) and clock signal (RPOHC). The signal on the data lead (RAIPD) consists of the FEBE count and a path RDI (FERF) status indication.

The Desynchronize Block removes the effect on the output DS3 or E3 signals of systemic jitter due to signal mapping and pointer movements. The output has an average frequency equal to the source frequency, and has jitter characteristics that meet ITU-TSS and ANSI standards. The Desynchronize Block consists of two circuits, a Pointer Leak circuit and a Phase-Locked Loop circuit. The function of the Pointer Leak circuit is to absorb the immediate effect of up to eight consecutive pointer movements (any combination of SPE or TUG-3 pointer movements) in either direction, and filter them out in time. A single pointer adjustment is an 8 Unit Interval (UI) phase step. The Pointer Leak circuit turns the phase step into eight 1-UI steps, widely spaced in time, allowing the Phase-Locked Loop circuit to track. In normal operation, the output is one data bit and one clock cycle for each input bit. When a negative stuff occurs 8 extra bits are pulled from the signal and absorbed. Following this operation, the normal operation of one bit in for one bit out continues except that one extra bit is pulled from the FIFO every n frames. In this way, the pointer step is leaked out in 8 x n frames. The value of n is programmed via the microprocessor.

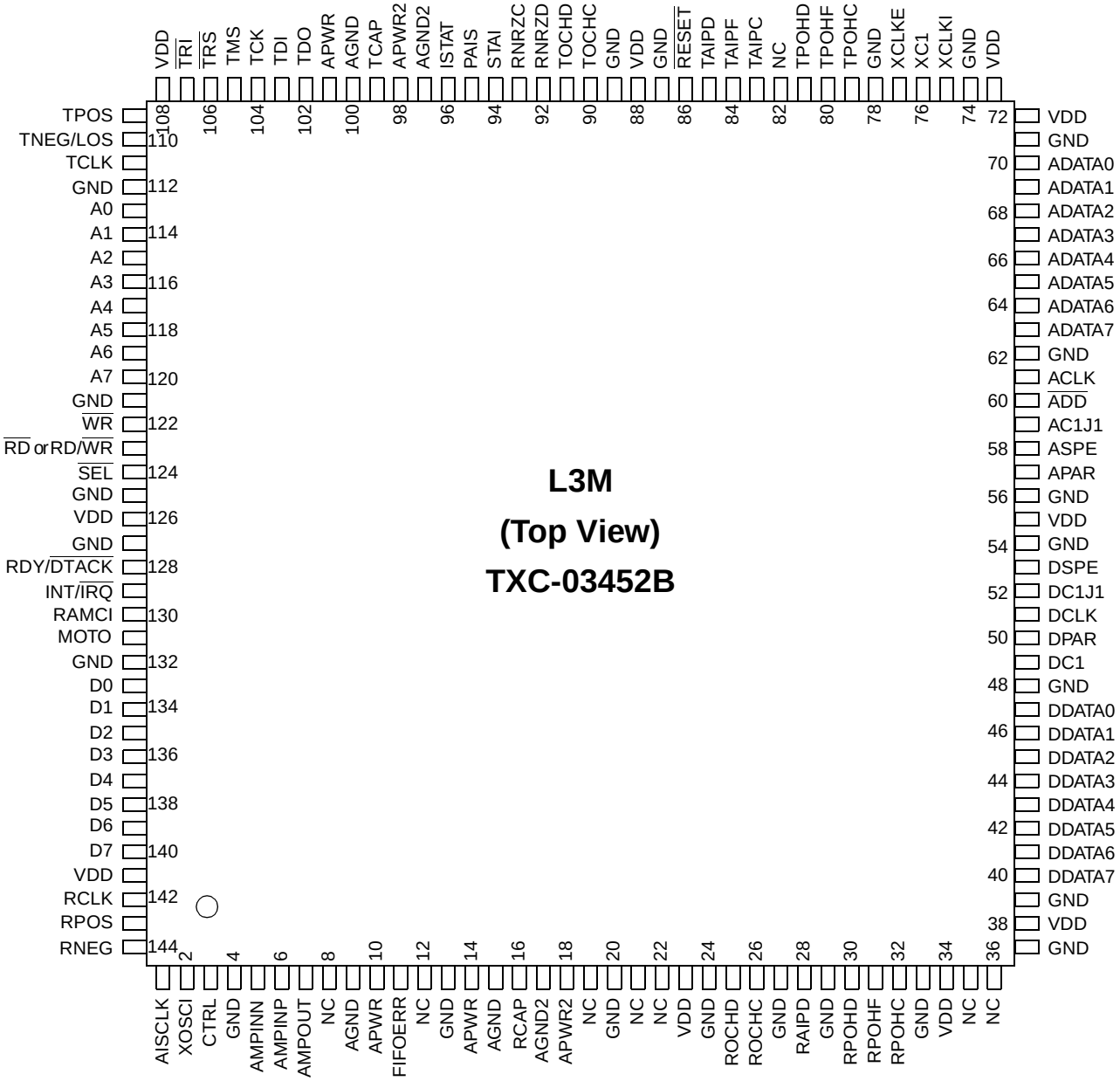
The Phase-Locked Loop (PLL) circuit of the Desynchronize Block is externally connected to a line-frequency voltage controlled crystal oscillator (VCXO) via a filter. Details of the external circuit for the PLL are provided in the Operation section of this Data Sheet under the heading "PLL Filter Connection to VCXO".

In the Receive direction, the Output Block provides either a positive (RPOS) and negative (RNEG) rail line signal or a NRZ line signal (RPOS), and a clock signal (RCLK). The HDB3/B3ZS coder operates independently of the transmitter. For interface flexibility, a control bit is provided for inverting the output clock. The receive data and clock outputs can be forced to a high impedance state for the purpose of tying two L3M devices together for ring operation or redundancy. An additional 2^{15}-1 or 2^{23}-1 pseudo-random test generator is provided. The Output Block and the Input Block share a 2^{15}-1 or 2^{23}-1 analyzer that can compare the desynchronizer output or transmit data against a fixed pattern. An alarm is provided when the analyzer and incoming data are not synchronous. Errors are counted in the 16-bit coding violation counter. Loopbacks between the Input and Output Blocks facilitate board and network debugging.

All of the control registers and performance counters, and the status and alarm indications, are accessible through the L3M device's compatible microprocessor bus interface in the Microprocessor I/O Block. The L3M device supports both Intel and Motorola microprocessor bus interfaces, with both hardware and software interrupt capability. The Motorola compatible microprocessor interface is selected by placing a high on the MOTO signal lead.

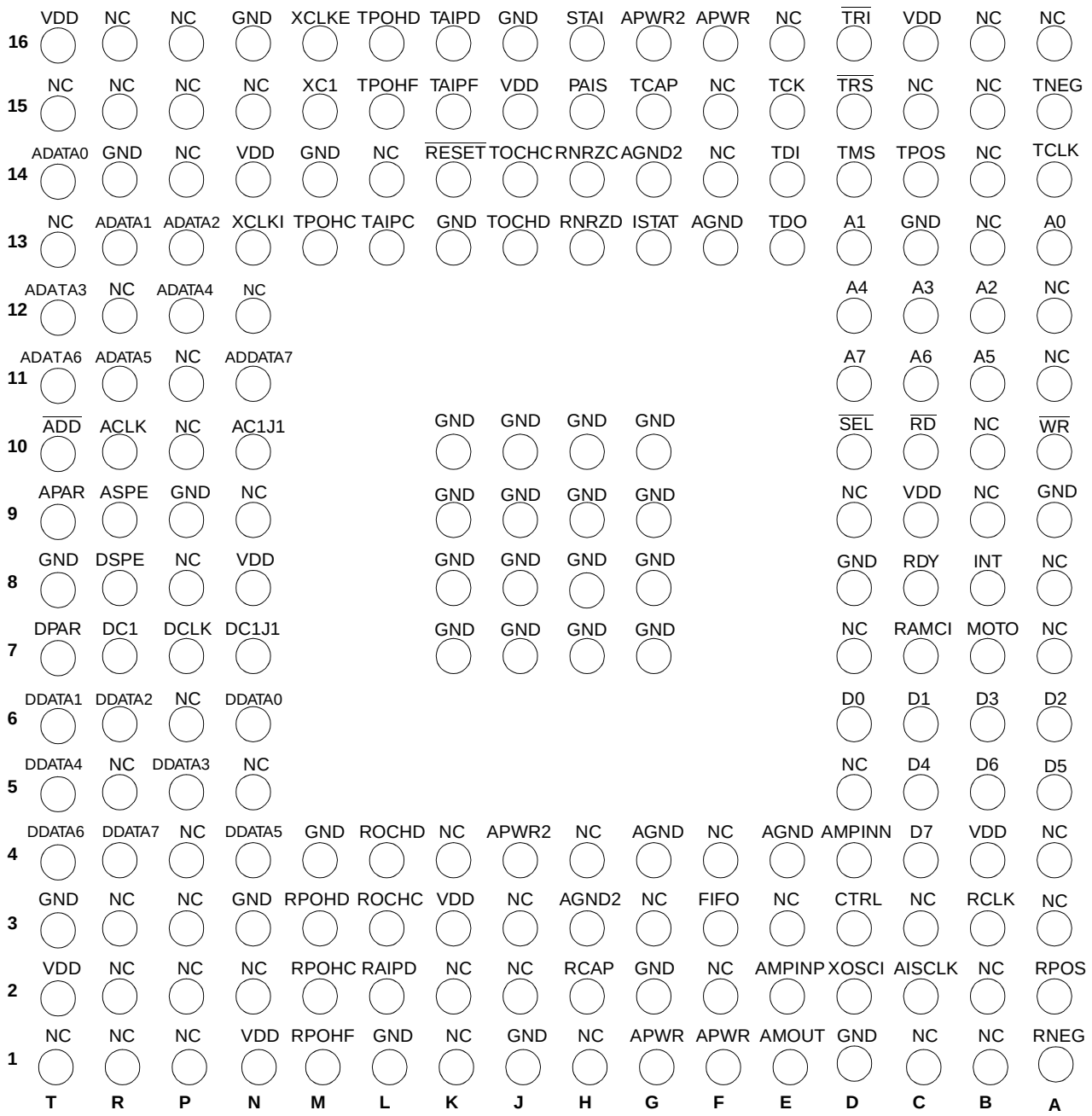
The Boundary Scan Block provides a mechanism for external access to the input and output leads of the device, so that they may be observed and tested. The structure and operation of this Block are described in the Operation section.

LEAD DIAGRAMS



Note: See Figure 37 for package information.

Figure 5. Lead Diagram for L3M TXC-03452B 144-Lead Plastic Quad Flat Package



Note: This is the bottom view. The leads are solder balls. See Figure 38 for package information. Some signal Symbols have been abbreviated to fit the space available. The Symbols are shown in full in the Lead Descriptions section.

Figure 6. Lead Diagram for L3M TXC-03452B 208-Lead Plastic Ball Grid Array Package

LEAD DESCRIPTIONS

POWER SUPPLY, GROUND AND NO CONNECTS

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P*	Type**	Name/Function
VDD	23,34,38,55, 72,73,88, 108,126,141	B4, C9, C16, K3, J15, N1, N8, N14, T2, T16	P		**VDD:** +5 volts, ± 5% power supply.
APWR	10,14,101	F1, F16, G1,	P		**Analog VDD:** +5 volts, ± 5% power supply.
APWR2	18,98	G16, J4	P		**Analog VDD2:** +5 volts, ± 5% power supply.
GND	4,13,20,24, 27,29,33,37, 39,48,54,56, 62,71,74,78, 87,89,112, 121,125, 127,132	A9, C13, D1, D8, G2, G7, G8, G9, G10, H7, H8, H9, H10, J1, J7, J8, J9, J10, J16, K7, K8, K9, K10, K13, L1, M4, M14, N3, N16, P9, R14, T3, T8	P		**Ground:** 0 volts reference.
AGND	9,15,100	E4, F13, G4	P		**Analog Ground:** 0 volts reference.
AGND2	17,97	G14, H3	P		**Analog Ground2:** 0 volts reference.
NC	8,12,19 21,22,35 36,82	A3, A4, A7, A8, A11, A12, A16, B1, B2, B9, B10, B13, B14, B15, B16, C1, C3, C15, D5, D7, D9, E3, E16, F2, F4, F14, F15, G3, H1, H4, J2, J3, K1, K2, K4, L14, N2, N5, N9, N12, N15, P1, P2, P3, P4, P6, P8, P10, P11, P14, P15, P16, R1, R2, R3, R5, R12, R15, R16, T1, T13, T15			**No Connect:** NC leads are not to be connected, not even to another NC lead, but must be left floating. Connection of these leads may impair performance or cause damage to the device.

*Note: I = Input; O = Output; P = Power; T = Tri-State

**Note: See Input, Output and Input/Output Parameters section below for the Type definitions.

LINE INTERFACE

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
RNRZD	92	H13	O	CMOS 4mA	**Receive Line NRZ Data:** Output provided for an optional external performance monitoring circuit. This serial NRZ output is provided after the decoder (transmit direction), independent of whether the input is NRZ or rail. Data is always clocked out on positive transitions of clock (RNRZC). This lead goes to a high impedance state when control bit L3Z is set to 1.
RNRZC	93	H14	O	CMOS 4mA	**Receive Line Clock:** NRZ data on lead RNRZD is clocked out of the L3M device on positive transitions of this clock. This lead goes to a high impedance state when control bit L3Z is set to 1.
TPOS	109	C14	I	CMOS	**Transmit NRZ Line Data/Positive Rail Data:** Serial NRZ input for the 44.736 or 34.368 Mbit/s asynchronous line data. This lead also provides the positive rail data input for an internal decoder.
TNEG/ LOS	110	A15	I	CMOS	**Transmit Negative Rail Data:** When operating in the P/N rail mode, this lead provides a negative rail input for the internal decoder. When operating in the NRZ mode, a high on this lead instead indicates an external loss of signal alarm, so that the lead must be tied to ground if it is not used for input of an external loss of signal indication.
TCLK	111	A14	I	CMOS	**Transmit Line Clock:** NRZ or rail data is clocked into the L3M device using the TPOS/TNEG signal leads on positive transitions of this clock when control bit INVCI is set to 0. NRZ or rail data is clocked in on negative transitions when control bit INVCI is set to 1. TCLK is used as the input clock for the transmit PRBS generator and it must be present to generate a test pattern.
RCLK	142	B3	O	CMOS 4mA	**Receive Line Clock:** Line data present on the RPOS/ RNEG signal leads (44.736 or 34.368 Mbit/s) is clocked out of the L3M device on negative transitions of this clock when control bit INVCO is set to 0. NRZ or rail data is clocked out on positive transitions of this clock when control bit INVCO is set to 1. This lead goes to a high impedance state when control bit L3Z is set to 1.
RPOS	143	A2	O	CMOS 4mA	**Receive Line NRZ Data/Positive Rail Data:** Serial NRZ output for the 44.736 or 34.368 Mbit/s asynchronous line data. This lead also provides the positive rail output when the rail interface is selected. This lead goes to a high impedance state when control bit L3Z is set to 1.
RNEG	144	A1	O	CMOS 4mA	**Receive Negative Rail Data:** This lead provides a negative rail interface from the internal coder. This lead goes to a high impedance state when control bit L3Z is set to 1. When the NRZ interface is selected, this lead outputs a 0.

MICROPROCESSOR INTERFACE

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
A(7-0)	120 - 113	D11, C11, B11, D12, C12, B12, D13, A13	I	TTL	**Address Bus:** These are address line inputs that are used by the microprocessor for accessing the L3M RAM for a read/write cycle. A0 is defined as the least significant bit. High is logic 1.
$\overline{WR}$	122	A10	I	TTL	**Write (I mode):** Intel Mode - An active low signal generated by the microprocessor for writing to the L3M RAM locations. Motorola Mode - Not used.
$\overline{RD}$ RD/$\overline{WR}$	123	C10	I	TTL	**Read (I mode) or Read/Write (M mode):** Intel Mode - An active low signal generated by the microprocessor for reading the L3M RAM locations. Motorola Mode - A high signal generated by the microprocessor for reading the L3M RAM locations. A low signal is used for writing to L3M RAM locations.
$\overline{SEL}$	124	D10	I	TTLp	**Select:** A low enables data transfers between the microprocessor and the L3M device during a read/write cycle.
RDY/ $\overline{DTACK}$	128	C8	O(T)	TTL8mA	**Ready (I mode) or Data Transfer Acknowledge (M mode):** Intel Mode - A high is an acknowledgment from the addressed RAM location that the transfer can be completed. A low indicates that the L3M has not completed the transfer cycle, and the microprocessor must wait before latching read data or completing the write cycle. Motorola Mode - During a read bus cycle, a low signal indicates the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data.
INT/$\overline{IRQ}$	129	B8	O(T)	TTL4mA	**Interrupt:** Intel Mode - A high on this output lead signals an interrupt request to the microprocessor. The off state is low when control bit INTZ (bit 2, register C2) is 0, and 3-state when INTZ is 1. Motorola Mode - A low on this lead signals an interrupt request to the microprocessor. The off state is high when INTZ is 0, and 3-state when INTZ is 1.
RAMCI	130	C7	I	CMOS	**RAM Clock Input:** Clock input for the internal RAM. This clock allows an outside clock to provide an arbitrator function for accessing the internal RAM structure. This clock must operate between 12 and 25 MHz with a duty cycle of 50 +/- 10 percent. This clock and the microprocessor timing signals may operate asynchronously with respect to each other.
MOTO	131	B7	I	TTL	**Motorola/Intel Microprocessor Select:** A high selects the Motorola microprocessor compatible bus interface. A low selects the Intel microprocessor compatible bus interface.

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
D(7-0)	140 - 133	C4, B5, A5, C5, B6, A6, C6, D6	I/O	TTL8mA	**Data Bus:** Bi-directional data lines used for transferring data between the L3M device and an external microprocessor. D0 is defined as the least significant bit. High is logic 1.

DROP BUS INTERFACE

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
DDATA (7-0)	40 - 47	R4, T4, N4, T5, P5, R6, T6, N6	I	TTL	**Drop Data Byte:** Byte data that corresponds to the STM-1/STS-3/STS-1 signal from the drop bus. The first bit received corresponds to bit 7.
DC1	49	R7	I	TTL	**Drop C1 Pulse:** External positive C1 pulse that may be provided on this lead instead of in the DC1J1 signal. This signal is ORed internally with the DC1J1 signal to form a composite C1J1 signal. If this lead is not used it must be grounded. This lead is used for special applications.
DPAR	50	T7	I	TTL	**Drop Bus Parity Bit:** This is an odd parity input for each data byte, the DSPE signal, and the composite DC1J1 pulses. The status bit BUSERR (bit 5 in registers B0 and B1) indicates when this input differs from an internally-generated odd parity for these signals, but no other action is taken upon occurrence of this drop bus parity error.
DCLK	51	P7	I	TTL	**Drop Bus Clock:** This clock operates at 19.44 MHz for STM-1/STS-3 operation, and at 6.48 MHz for STS-1 bus operation. Drop bus byte-wide data (DDATA7-0), parity (DPAR), payload indicator (DSPE), and C1/J1 (DC1J1 and DC1) are clocked into the L3M device on negative transitions of this clock.
DC1J1	52	N7	I	TTL	**Drop Bus C1 and J1 Indicator:** The C1 pulse is an active high, one clock cycle wide timing pulse that indicates the location of the first C1 time slot in the STM-1 or STS-3 frame. If the C1 pulse is not present in this signal, it must be provided at the DC1 lead. A J1 pulse, also one clock cycle wide, identifies the location of the J1 byte.
DSPE	53	R8	I	TTL	**Drop Bus SPE Indicator:** A signal that is high during the STM-1 VC-4, and the STS-3/STS-1 SPE period.

ADD BUS INTERFACE

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
APAR	57	T9	O(T)	TTL4mA	**Add Bus Parity Bit:** This output bit represents the odd parity calculation for each data byte in the add timing and drop timing modes. In the external timing mode, the parity calculation also includes the ASPE and AC1J1 signals which become outputs. This lead is forced to a high impedance state when the control bit ADDZ is set to 1, or when $\overline{ADD}$ is inactive (high).
ASPE	58	R9	I/O(T)	TTL4mA	**Add Bus SPE Indicator:** An input signal that is high during the STM-1 VC-4 period, and STS-3/STS-1 SPE period. When enabled by the external clock enable (XCLKE) control lead, this signal becomes an output. This lead is forced to a high impedance state when the control bit ADDZ is set to 1, or when the drop timing mode is selected.
AC1J1	59	N10	I/O(T)	TTL4mA	**Add Bus C1 and J1 Indicator:** The C1 pulse is an active high, one clock cycle wide input timing pulse that identifies the location of the first C1 time slot in the STM-1 or STS-3 frame. A J1 pulse, also one clock cycle wide, identifies the location of the J1 byte. When enabled by the external clock enable (XCLKE) control lead, this signal becomes an output. This lead goes to a high impedance state when control bit ADDZ is set to 1, or when the drop timing mode is selected.
$\overline{ADD}$	60	T10	O	TTL4mA	**Add Indicator:** An active low signal that identifies the position of the data time slots being mapped onto the add bus. This signal will be high when - Data is not present - Reset is present - Add bus loss of clock occurs - When control bit ADDZ is set to 1. - Until the first two C1 pulses are received in either the add bus or drop bus timing mode. This avoids bus contention during start up. This signal will be a high impedance when the $\overline{TRI}$ lead is low.
ACLK	61	R10	I/O	TTL4mA	**Add Bus Clock:** This clock operates at 19.44 MHz for STM-1/STS-3 operation, and at 6.48 MHz for STS-1 bus operation. The add clock is used for Build Block timing and for sourcing the add bus byte-wide data (ADATA(7-0)), parity (APAR), and add indicator ($\overline{ADD}$). When enabled by the external clock enable (XCLKE) control lead, this signal becomes an output. This lead goes to a high impedance state when control bit ADDZ is set to 1.

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
ADATA (7-0)	63 - 70	N11, T11, R11, P12, T12, P13, R13, T14	O(T)	TTL4mA	**Add Data Byte:** Byte-wide data that corresponds to the STM-1/STS-3/STS-1 time slots that are placed on the add bus. Bit 7 corresponds to bit 1 in the STM-1/SONET transmission format. This bus is forced to a high impedance state when the control bit ADDZ is set to 1, or when $\overline{\text{ADD}}$ is inactive (high).

OVERHEAD COMMUNICATIONS CHANNEL INTERFACE

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
ROCHD	25	L4	O	TTL4mA	**Receive Overhead Comm Channel Data:** Unaligned data output for the overhead communications channel “O”-bits from the DS3 or E3 formats. The “O”-bits are clocked out of the L3M device on negative transitions of the ROCHC clock signal.
ROCHC	26	L3	O	TTL4mA	**Receive Overhead Comm Channel Clock:** A gapped 720 kHz output clock with an average frequency of 144 kHz for clocking out the transmit overhead communications channel bits to external circuitry.
TOCHC	90	J14	O	TTL4mA	**Transmit Overhead Comm Channel Clock:** A gapped 720 kHz output clock with an average frequency of 144 kHz for sourcing the transmit overhead communications channel bits from external circuitry.
TOCHD	91	J13	I	TTL	**Transmit Overhead Comm Channel Data:** Data input for the overhead communications channel in the DS3 or E3 formats. Data is clocked into the L3M device on positive transitions of the TOCHC clock signal. The bits are multiplexed into the “O”-bit positions unaligned regarding bit position and subframe number. This input is enabled by the EXOO control bit. When enabled, the lead must be grounded if it is desired to insert zeroes in the corresponding fixed stuff locations.

PATH OVERHEAD INTERFACE

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
RPOHD	30	M3	O	TTL4mA	**Receive Path Overhead Data:** The serial output for the nine path overhead bytes. The POH bytes are clocked out on negative transitions of the clock signal (RPOHC).
RPOHF	31	M1	O	TTL4mA	**Receive Path Overhead Framing:** A positive one clock cycle (RPOHC) wide output framing pulse that is synchronous with the J1 data of RPOHD. This signal is also used as the framing pulse for the receive alarm indication port data (RAIPD).
RPOHC	32	M2	O	TTL4mA	**Receive Path Overhead Clock:** A gapped clock used for clocking out the path overhead bytes, and receive alarm indication port data (RAIPD).
TPOHC	79	M13	O	TTL4mA	**Transmit Path Overhead Clock:** A gapped clock used for clocking the path overhead bytes from an external circuit into the L3M device.
TPOHF	80	L15	O	TTL4mA	**Transmit Path Overhead Framing:** A positive one clock cycle (TPOHC) wide output framing pulse that determines the start of the J1 byte in TPOHD.
TPOHD	81	L16	I	TTL	**Transmit Path Overhead Data:** A serial input for the following path overhead bytes: J1, C2, G1, F2, H4, Z3, Z4, and Z5 bytes. The POH bytes are clocked into the L3M device on positive transitions of the TPOHC clock signal. Eight bits are clocked in during the B3 byte time, but they are ignored by the L3M device.

ALARM INDICATION PORT

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
RAIPD	28	L2	O	TTL4mA	**Receive Alarm Indication Port Data:** A serial output that provides the 4-bit FEBE count (B3 error count) and Path RDI alarm indication to a mate L3M device for ring operation. This lead is normally connected to the TAIPD lead at the mate L3M device. The RPOHC signal is used to clock this signal out of the L3M device. The RPOHF signal provides the frame reference signal. The bits are sent in the following format: Bits: 1 2 3 4 | 5 | 6 7 8 B3 Count | RDI | 0 0 1 Bit 1 is the MSB and is sent first in the bit stream.
TAIPC	83	L13	I	TTL	**Transmit Alarm Indication Port Clock:** This clock input is normally connected to the RPOHC clock lead at the mate L3M device for ring operation. Transmit alarm data (TAIPD) is clocked into the L3M device on positive transitions of the RPOHC clock.
TAIPF	84	K15	I	TTL	**Transmit Alarm Indication Port Framing Pulse:** Normally connected to RPOHF lead at the mate L3M device for ring operation. Used to indicate the first bit in the first byte for the external alarm indications.
TAIPD	85	K16	I	TTL	**Transmit Alarm Indication Port Data:** This serial input lead is normally connected to the RAIPD lead at the mate L3M device for ring operation. Provides an input for the four bit FEBE count (B3 error count), and Path RDI alarm indication (as shown above for RAIPD).

ADDITIONAL SIGNALS

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
AISCLK	1	C2	I	CMOS	**AIS Clock Input:** Clock input for the L3M device's AIS generator. This clock must be present for the AIS generator to function. The clock must have the operating line rate of either 44.736 or 34.368 MHz, and have a frequency stability of +/- 20 ppm.
XCLKI	75	N13	I	TTL	**External Clock Input:** Used to derive output timing and data for the add bus. Enabled by placing a high on the lead labeled XCLKE. A byte clock frequency of 6.48 MHz is required for STS-1 operation. This clock is monitored for loss of clock when the external timing mode is selected.

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
XC1	76	M15	I	TTL	**External C1 Input:** Optional C1 input signal used to synchronize the frame start when the external timing mode is selected for the add bus. This lead must be held low when the external timing mode is not used.
XCLKE	77	M16	I	TTL	**External Clock Enable:** A high on this lead enables add bus timing to be derived from the XCKLI lead (external clock signal). The ASPE, AC1J1, and ACLK signal leads become output leads.
$\overline{\text{RESET}}$	86	K14	I	TTLp	**Hardware Reset:** A low clears all counters and initiates reframing in the transmit direction upon its release. This lead is provided with an internal pull-up resistor. The reset signal must be low for a minimum of 200 nanoseconds. The bus clocks, line clocks, microprocessor clock and VCXO clock must be present during the reset signal. The add bus outputs are held in a high impedance state during the reset period. The add bus high impedance state is released on the occurrence of the C1 pulse.
FIFOERR	11	F3	O	TTL8mA OD	**FIFO Reset Indication:** This lead requires an external 4.7 kΩ pull-up resistor to +5V. A high on this lead indicates that the receive side FIFOs have been reset. The reset condition occurs after a hardware reset ($\overline{\text{RESET}}$, lead 86 or K14) or a software reset (control bit RXRST), or after a FIFO error (underflow or overflow). After the hardware or software reset, or the FIFO error, clears, FIFOERR stays high for a minimum of 125 microseconds and a maximum of 250 microseconds before returning to its normal low level.
STAI	94	H16	I	TTL	**STS Network Alarm Indication:** A high on this lead will generate a count of 9 in bits 1 through 4 of G1 when control bit FEBE9EN is equal to 1. An indication is also provided as the XSTAI status bit. The lead is normally grounded.
PAIS	95	H15	I	TTL	**External Path AIS Indication:** A high on this lead may be used to indicate an external Path AIS has occurred. It causes the XPAIS status bit to be set to 1. This lead is enabled when control bit XALM2AIS is a 1. When enabled, the in-band upstream AIS indication provided via the TOH E1 byte is disabled.
ISTAT	96	G13	I	TTL	**External STS-1 Alarm Indication:** A high on this lead may be used to indicate an external SONET/SDH alarm has occurred. It causes the XISTAT status bit to be set to 1.
$\overline{\text{TRI}}$	107	D16	I	TTLp	**High Impedance Enable:** A low causes all L3M device digital outputs and bi-directional leads to be set to a high impedance state for test purposes. This lead is provided with an internal pull-up resistor.

RECEIVE AND TRANSMIT PHASE LOCKED LOOPS

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
RCAP	16	H2	I	Analog	**Receiver Internal Phase Locked Loop Capacitor:** Optional capacitor used for an internal receive phase locked loop. This lead must be left floating.
TCAP	99	G15	I	Analog	**Transmitter Internal Phase Locked Loop Capacitor:** Optional capacitor used for an internal transmit phase locked loop. This lead must be left floating.

RECEIVE DESYNCHRONIZER

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
XOSCI	2	D2	I	CMOS	**External Oscillator Input:** This input is connected to the output of the external VCXO, as shown in the PLL connections diagram (Figure 32).
CTRL	3	D3	O	CMOS 4mA	**Phase Detector Output**: Normally connected to the external low pass filter consisting of external components and the internal amplifier.
AMPINN	5	D4	I	Analog	**Internal Amplifier - Negative Port Input:** Negative port of an internal amplifier which can be used in the desynchronizer loop filter.
AMPINP	6	E2	I	Analog	**Internal Amplifier - Positive Port Input:** Positive port of an internal amplifier which can be used in the desynchronizer loop filter.
AMPOUT	7	E1	O	Analog	**Internal Amplifier - Output:** Output of an internal amplifier which can be used in the desynchronizer loop filter.

BOUNDARY SCAN TESTING

Symbol	144-Lead QFP Lead No.	208-Lead BGA Lead No.	I/O/P	Type	Name/Function
TDO	102	E13	O(T)	TTL4mA	**Boundary Scan Test Data Output:** Serial data clocked out on negative transitions of TCK.
TDI	103	E14	I	TTL	**Boundary Scan Test Data Input:** Serial data input for boundary scan test messages.
TCK	104	E15	I	TTL	**Boundary Scan Test Clock:** The input clock for boundary scan testing. The TDI and TMS states are clocked in on positive transitions.
TMS	105	D14	I	TTLp	**Boundary Scan Test Mode Select:** The signal present on this lead is used to control test operations.
$\overline{\text{TRS}}$	106	D15	I	TTLp	**Boundary Scan Test Reset:** To asynchronously reset the Test Access Port (TAP) controller, this lead must either be held low or asserted low for at least 200 ns and then held high (i.e., pulsed low). The TAP controller may also be reset by holding the TMS signal lead high for at least five clock cycles of TCK. Failure to perform this reset may cause the TAP controller to take control of the output leads. In applications which will not be using the boundary scan feature, this lead must be tied low, thereby holding the TAP controller reset.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+7.0	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	Notes 1, 3
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient Operating Temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Component Temperature x Time	TI		270 x 5	^oC x s	Note 1
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Notes 4, 5

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the “CAUTION” label on the drypack bag in which devices are supplied.
3. V_{IN} may not exceed the actual operating supply voltage (V_{DD}) by more than 0.5 volt.
4. Test method for ESD per MIL-STD-883D, Method 3015.7.
5. This note applies to product TXC-03452CIOG only. AGND leads F13 and G4 have shown an ESD sensitivity at absolute levels of 1500 volts and above. APWR lead F16, APWR lead G1 and APWR2 lead G16 have shown an ESD sensitivity at absolute levels of 1500 volts and above.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
144-lead QFP thermal resistance: junction to ambient			34	$^oC/W$	0 ft/min linear airflow
208-lead BGA thermal resistance: junction to ambient			29.0	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.00	5.25	V	
I_{DD}			220	mA	
Analog V_{DD}	4.75	5.00	5.25	V	
Analog I_{DD}			30	mA	
Analog V_{DD2}	4.75	5.00	5.25	V	
Analog I_{DD2}			1	mA	
P_{DD}			1320	mW	Inputs switching

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

INPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			1.65	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current			-10	µA	$V_{DD} = 5.25$; $V_{IN} = 0$
Input capacitance		3.5		pF	

INPUT PARAMETERS FOR TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current			-10	µA	$V_{DD} = 5.25$; $V_{IN} = 0$
Input capacitance		3.5		pF	

INPUT PARAMETERS FOR TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current		-0.5	-1.4	mA	$V_{DD} = 5.25$; $V_{IN} = 0$
Input capacitance		3.5		pF	

OUTPUT PARAMETERS FOR CMOS 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	$V_{DD(MIN)}$ - 0.7			V	$V_{DD} = 4.75$; $I_{OH} = -4.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	1.2	2.8	5.0	ns	$C_{LOAD} = 15pF$
t_{FALL}	0.9	2.0	4.1	ns	$C_{LOAD} = 15pF$

OUTPUT PARAMETERS FOR CMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	$V_{DD(MIN)}$ - 0.7			V	V_{DD} = 4.75; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}	1.2	2.8	5.0	ns	C_{LOAD} = 15pF
t_{FALL}	0.9	2.0	4.1	ns	C_{LOAD} = 15pF

INPUT/OUTPUT PARAMETERS FOR TTL 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤ V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤ V_{DD} ≤ 5.25
Input leakage current			-10	µA	V_{DD} = 5.25; V_{IN} = 0
Input capacitance		3.5		pF	
V_{OH}	2.4V			V	V_{DD} = 4.75; I_{OH} = -4.0 (Note 1)
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0 (Note 1)
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	2.5	5.5	10.0	ns	C_{LOAD} = 15pF
t_{FALL}	1.0	2.0	4.0	ns	C_{LOAD} = 15pF

INPUT/OUTPUT PARAMETERS FOR TTL 8mA AND TTL 8mA OD (OPEN DRAIN)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤ V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤ V_{DD} ≤ 5.25
Input leakage current			-10	µA	V_{DD} = 5.25; V_{IN} = 0
Input capacitance		3.5		pF	
V_{OH}	2.4V			V	V_{DD} = 4.75; I_{OH} = -8.0 (Note 1)
V_{OL} (Note 2)			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0 (Note 1)
I_{OL} (Note 2)			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}	1.9	4.5	8.0	ns	C_{LOAD} = 25pF
t_{FALL} (Note 2)	0.8	1.5	3.1	ns	C_{LOAD} = 25pF

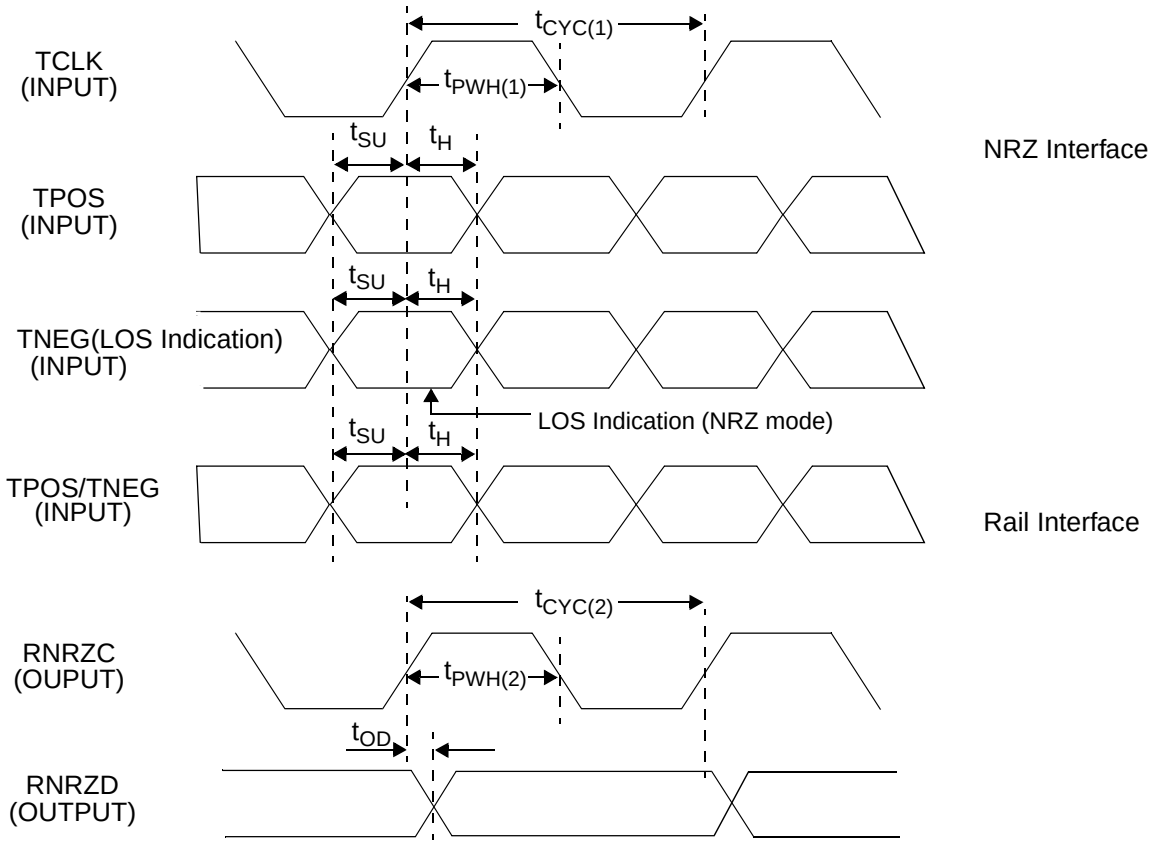
Notes:

1. Output drivers will output CMOS logic levels into CMOS loads.
2. V_{OL}, I_{OL} and t_{FALL} are the only parameters applicable to TTL 8mA OD.

TIMING CHARACTERISTICS

Detailed timing diagrams for the L3M device are illustrated in Figures 7 through 29, with values of the timing intervals tabulated below the diagrams. All output times are measured with a maximum 25 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals.

Figure 7. Line Side Transmit Timing

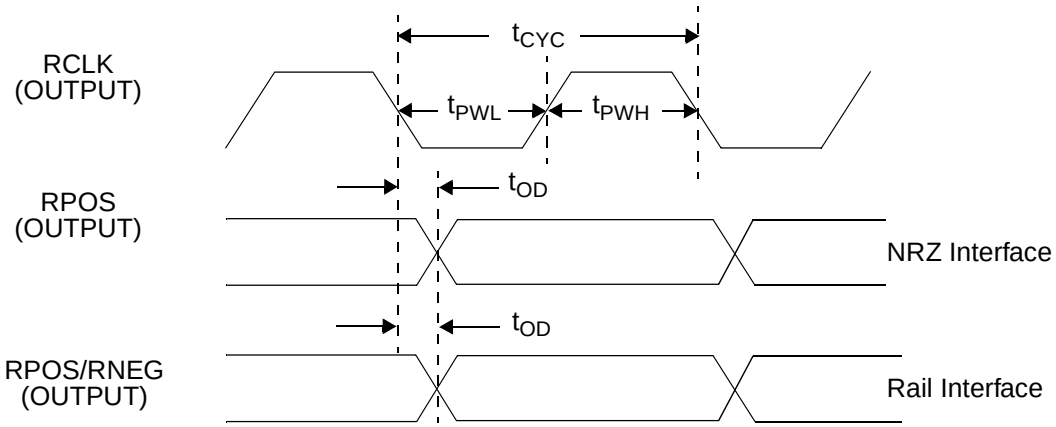


Note: Shown for INVCI equal to 0; data is clocked in on the negative edge when INVCI equals 1. RNRZD is always clocked out on the positive transitions of RNRZC. The delay between the input clock TCLK and output clock RNRZC is not specified.

Parameter	Symbol	Min	Typ	Max	Unit
TCLK clock period	$t_{CYC(1)}$		*		ns
TCLK duty cycle, $t_{PWH(1)}/t_{CYC(1)}$	--	40	50	60	%
TPOS/TNEG input set-up time to TCLK↑	t_{SU}	4.0			ns
TPOS/TNEG input hold time after TCLK↑	t_H	2.0			ns
RNRZC clock period	$t_{CYC(2)}$		*		ns
RNRZC duty cycle, $t_{PWH(2)}/t_{CYC(2)}$	--	40	50	60	%
RNRZD output delay after RNRZC↑	t_{OD}	-2.0		5.0	ns

* 22.35 ns (DS3) or 29.10 ns (E3).

Figure 8. Line Side Receive Timing



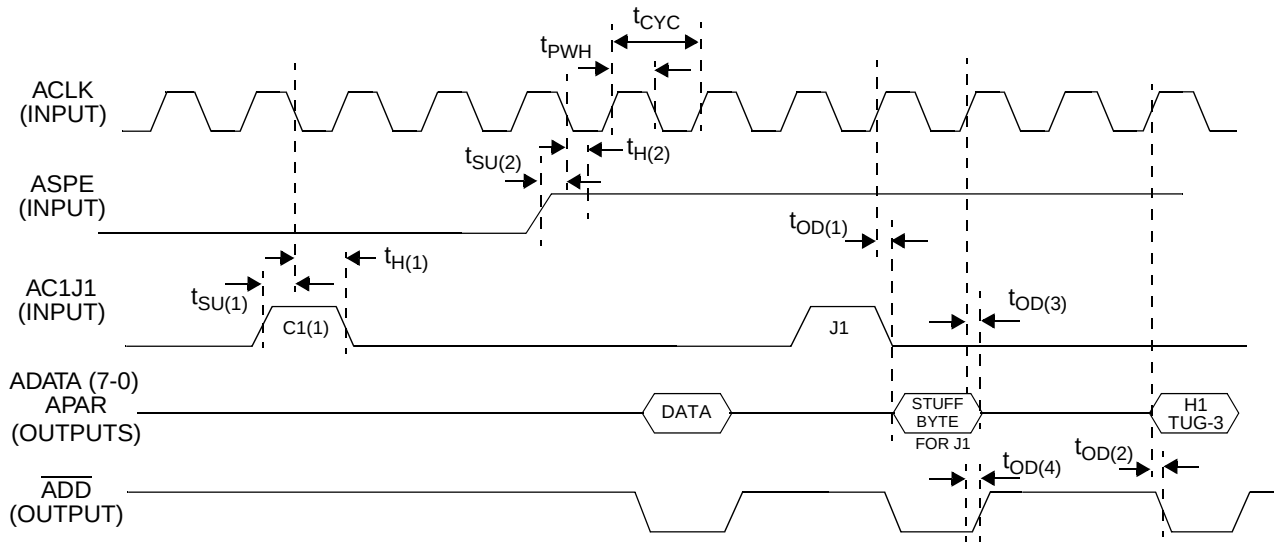
Note: Shown for INVCO equal to 0; data is clocked out on the positive edge when INVCO equals 1. The three signals are forced to a high impedance state when control bit L3Z is set to 1.

Parameter	Symbol	Min	Typ	Max	Unit
RCLK clock period	t_{CYC}		See Note 1		ns
RCLK high time	t_{PWH}		$t_{CYC}/2$		ns
RCLK low time	t_{PWL}		$t_{CYC}/2$		ns
RCLK duty cycle, t_{PWH}/t_{CYC} (See Note 2)	---	45	50	55	%
RPOS/RNEG data output delay after RCLK↓	t_{OD}	-2.0		5.0	ns

Notes:

1. 22.35 ns (DS3) or 29.10 ns (E3).
2. The RCLK output is derived from the XOSCI input from the external VCXO.

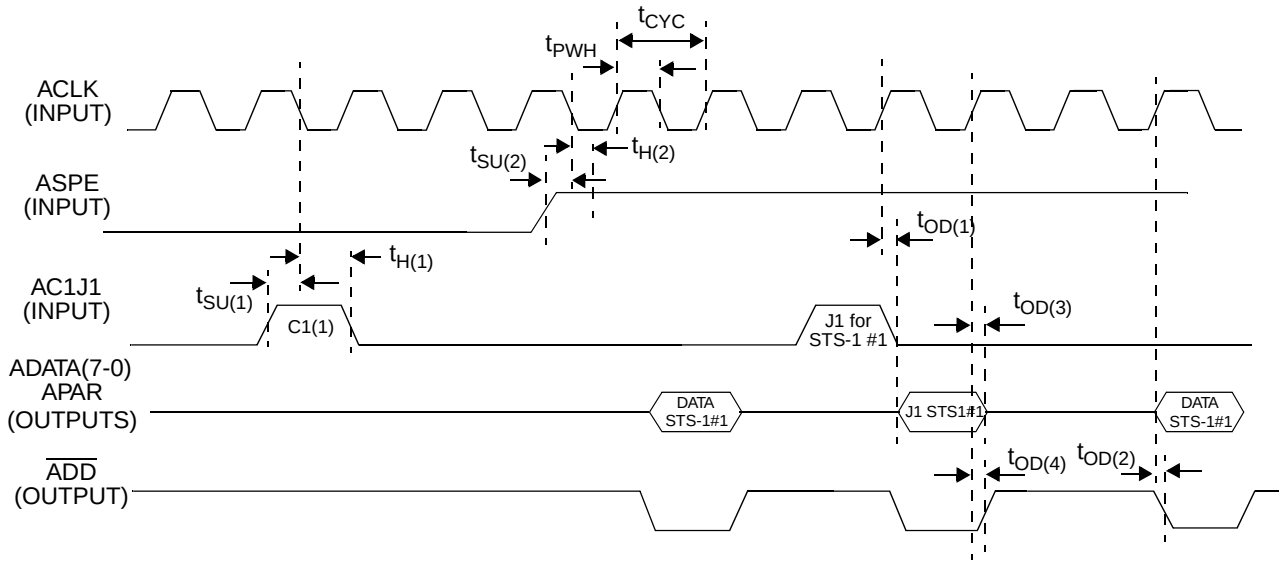
Figure 9. STM-1 Add Bus Derived Interface Timing



Note: The relationship between J1 and the SPE signal is shown for illustration purposes only. For the STM-1 format, there will be one J1 pulse which indicates the start of the VC-4 that carries the three TUG-3s. The TUG-3 added to the bus is shown for the TUG-3 designated as A. TUG-3 B will occur one clock cycle later. There is always a one byte delay between the output ADATA and AC1J1/ASPE inputs.

Parameter	Symbol	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}		51.44		ns
ACLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
AC1J1 set-up time to ACLK$\downarrow$	$t_{SU(1)}$	7.0			ns
AC1J1 hold time after ACLK$\downarrow$	$t_{H(1)}$	3.0			ns
ASPE set-up time to ACLK$\downarrow$	$t_{SU(2)}$	10.0			ns
ASPE hold time after ACLK$\downarrow$	$t_{H(2)}$	5.0			ns
ADATA(7-0) data and APAR output delay from ACLK$\uparrow$	$t_{OD(1)}$	3.0		30	ns
$\overline{\text{ADD}}$ low output delay from ACLK$\uparrow$	$t_{OD(2)}$	3.0		25	ns
ADATA(7-0) and APAR tri-state delay from ACLK$\uparrow$	$t_{OD(3)}$	12		25	ns
$\overline{\text{ADD}}$ high output delay from ACLK$\uparrow$	$t_{OD(4)}$	12		25	ns

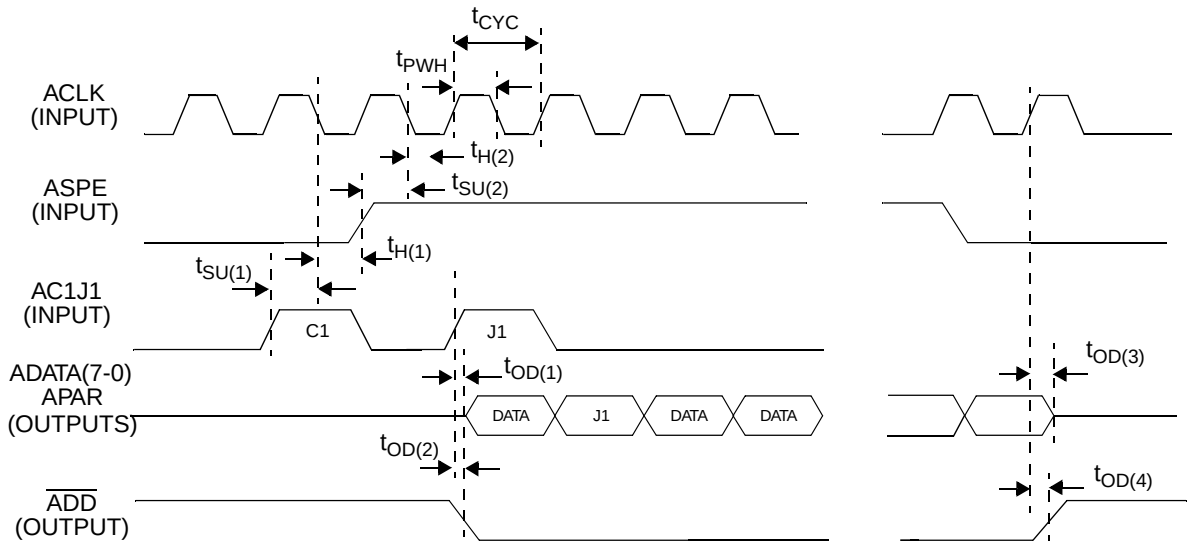
Figure 10. STS-3 Add Bus Derived Interface Timing



Note: The relationship between J1 and the SPE signal is shown for illustration purposes only. For the STS-3 format, there will be three J1 pulses which indicate the start of each of the STS-1 SPEs. The STS-1 SPE added to the bus is shown for STS-1 number 1. STS-1 number 2 will occur one clock cycle later. There is always a one byte delay between the output ADATA and AC1J1/ASPE inputs.

Parameter	Symbol	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}		51.44		ns
ACLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
AC1J1 set-up time to ACLK$\downarrow$	$t_{SU(1)}$	7.0			ns
AC1J1 hold time after ACLK$\downarrow$	$t_{H(1)}$	3.0			ns
ASPE set-up time to ACLK$\downarrow$	$t_{SU(2)}$	10.0			ns
ASPE hold time after ACLK$\downarrow$	$t_{H(2)}$	5.0			ns
ADATA(7-0) data and APAR output delay from ACLK$\uparrow$	$t_{OD(1)}$	3.0		30	ns
$\overline{ADD}$ low output delay from ACLK$\uparrow$	$t_{OD(2)}$	3.0		25	ns
ADATA(7-0) and APAR tri-state delay from ACLK$\uparrow$	$t_{OD(3)}$	12		25	ns
$\overline{ADD}$ high output delay from ACLK$\uparrow$	$t_{OD(4)}$	12		25	ns

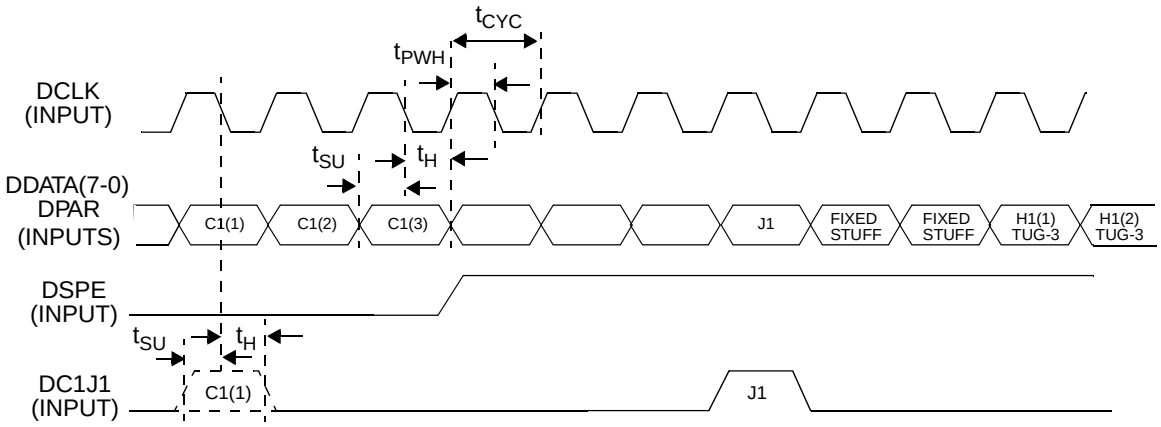
Figure 11. STS-1 Add Bus Derived Interface Timing



Note: The relationship between J1 and the SPE signal is shown for illustration purposes only. There is always a one byte delay between the output ADATA and AC1J1/ASPE inputs.

Parameter	Symbol	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}		154.32		ns
ACLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
AC1J1 set-up time to ACLK↓	$t_{SU(1)}$	7.0			ns
AC1J1 hold time after ACLK↓	$t_{H(1)}$	3.0			ns
ASPE set-up time to ACLK↓	$t_{SU(2)}$	10.0			ns
ASPE hold time after ACLK↓	$t_{H(2)}$	5.0			ns
ADATA(7-0) data and APAR output delay from ACLK↑	$t_{OD(1)}$	3.0		30	ns
$\overline{ADD}$ low output delay from ACLK↑	$t_{OD(2)}$	3.0		25	ns
ADATA(7-0) and APAR tri-state delay from ACLK↑	$t_{OD(3)}$	12		25	ns
$\overline{ADD}$ high delay from ACLK↑	$t_{OD(4)}$	12		25	ns

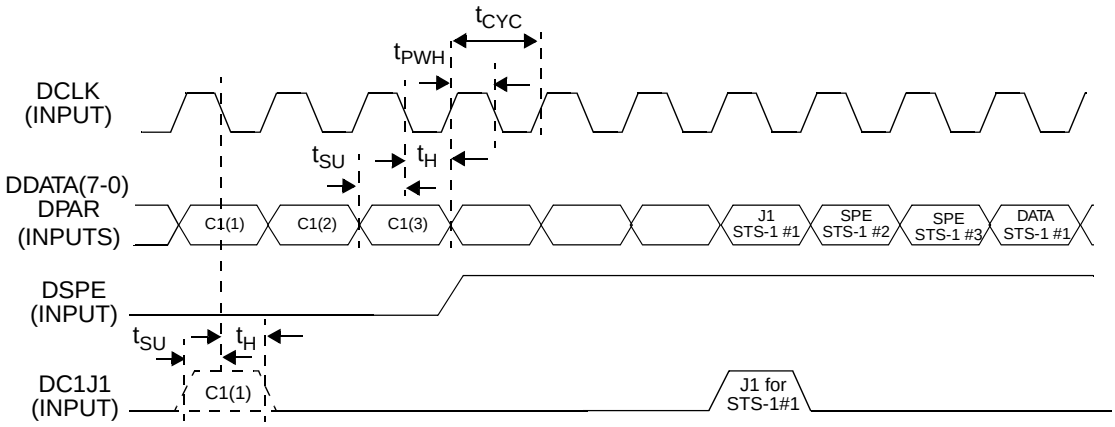
Figure 12. STM-1 Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STM-1 format, there will be one J1 pulse which indicates the start of the VC-4 that carries the three TUG-3s. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
DDATA(7-0) data/DPAR/DC1J1 set-up time to DCLK↓	t_{SU}	7.0			ns
DDATA(7-0) data/DPAR/DC1J1 hold time after DCLK↓	t_H	3.0			ns

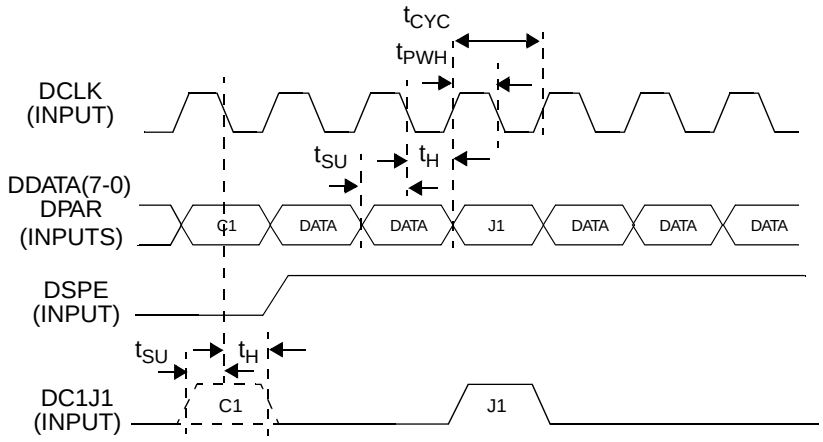
Figure 13. STS-3 Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STS-3 format, there will be three J1 pulses which indicate the start of each of the STS-1 SPEs. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
DDATA(7-0) data/DPAR/DC1J1 set-up time to DCLK↓	t_{SU}	7.0			ns
DDATA(7-0) data/DPAR/DC1J1 hold time after DCLK↓	t_H	3.0			ns

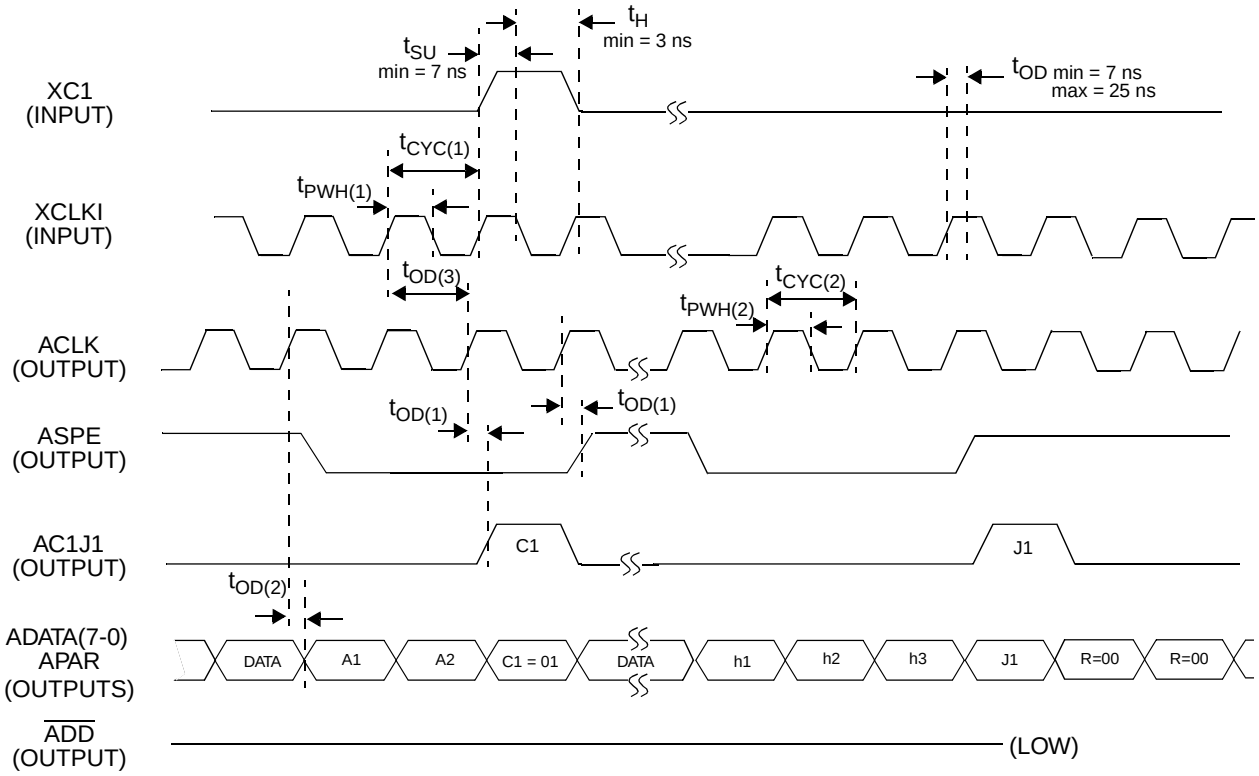
Figure 14. STS-1 Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STS-1 format, there will be one J1 pulse which indicates the start of the STS-1 SPE. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		154.32		ns
DCLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
DDATA(7-0) data/DPAR/DC1J1 set-up time to DCLK↓	t_{SU}	7.0			ns
DDATA(7-0) data/DPAR/DC1J1 hold time after DCLK↓	t_H	3.0			ns

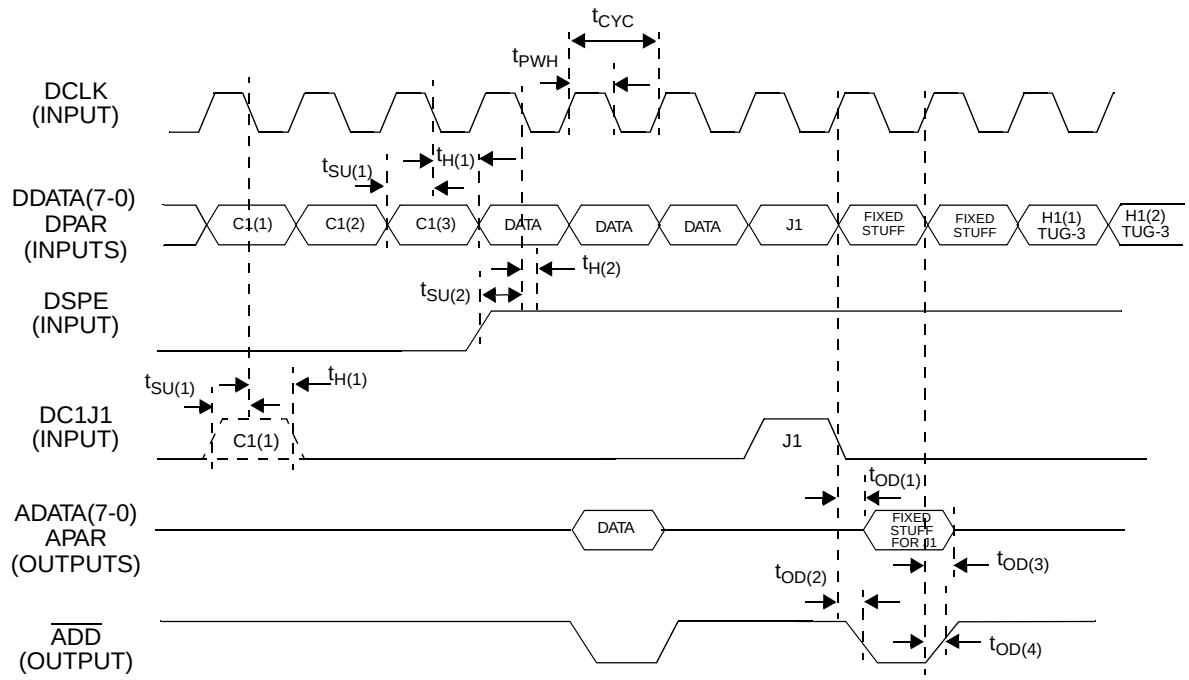
Figure 15. STS-1 Add Bus Interface Timing Using an External Clock



Note: Timing is shown for STS-1 signal. Pointer value is transmitted with a value equal to 0. When the TOHOUT bit is set to 1, the A1, A2, C1, H1, and H2 bytes are generated. Different from add/drop mode, output AC1J1/ASPE and ADATA are synchronous in the external clock mode.

Parameter	Symbol	Min	Typ	Max	Unit
XCLKI clock period	$t_{CYC(1)}$		154.32		ns
XCLKI duty cycle, $t_{PWH(1)}/t_{CYC(2)}$	--	40	50	60	%
ACLK clock period	$t_{CYC(2)}$		154.32		ns
ACLK duty cycle, $t_{PWH(2)}/t_{CYC(2)}$	--	40	50	60	%
AC1J1/ASPE delay after ACLK↑	$t_{OD(1)}$	0.0		5.0	ns
ADATA(7-0) data and APAR delay after ACLK↑	$t_{OD(2)}$	0.0		12	ns
ACLK↑ clock delay after XCLKI↑	$t_{OD(3)}$	3.0		25	ns

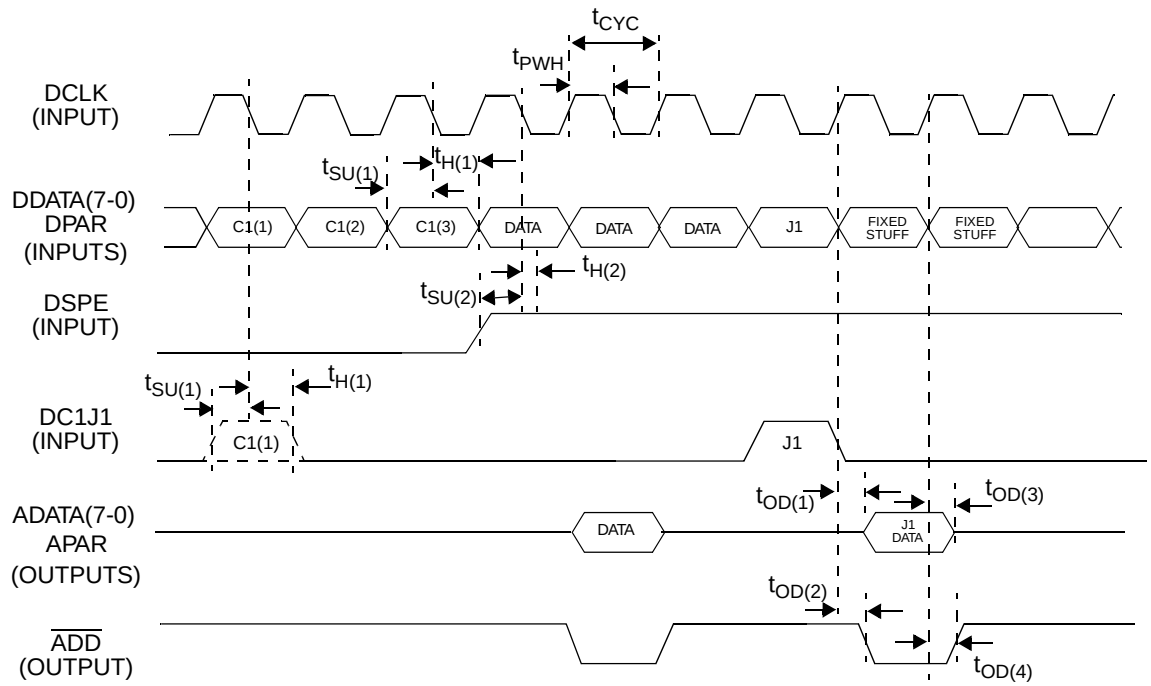
Figure 16. STM-1 Add/Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STM-1 format, there will be one J1 pulse which indicates the start of the VC-4 that carries the three TUG-3s. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded. Shown is TUG-3 A being added to the Add bus.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
DDATA(7-0) data/DPAR/DC1J1 set-up time to DCLK↓	$t_{SU(1)}$	7.0			ns
DDATA(7-0) data/DPAR/DC1J1 hold time after DCLK↓	$t_{H(1)}$	3.0			ns
DSPE set-up time to DCLK↓	$t_{SU(2)}$	10.0			ns
DSPE hold time after DCLK↓	$t_{H(2)}$	5.0			ns
ADATA(7-0) data and APAR delay after DCLK↑	$t_{OD(1)}$	3.0		30	ns
$\overline{ADD}$ indicator delayed after DCLK↑	$t_{OD(2)}$	3.0		25	ns
ADATA(7-0) data and APAR tri-state after DCLK↑	$t_{OD(3)}$	12		25	ns
$\overline{ADD}$ high after DCLK↑	$t_{OD(4)}$	12		25	ns

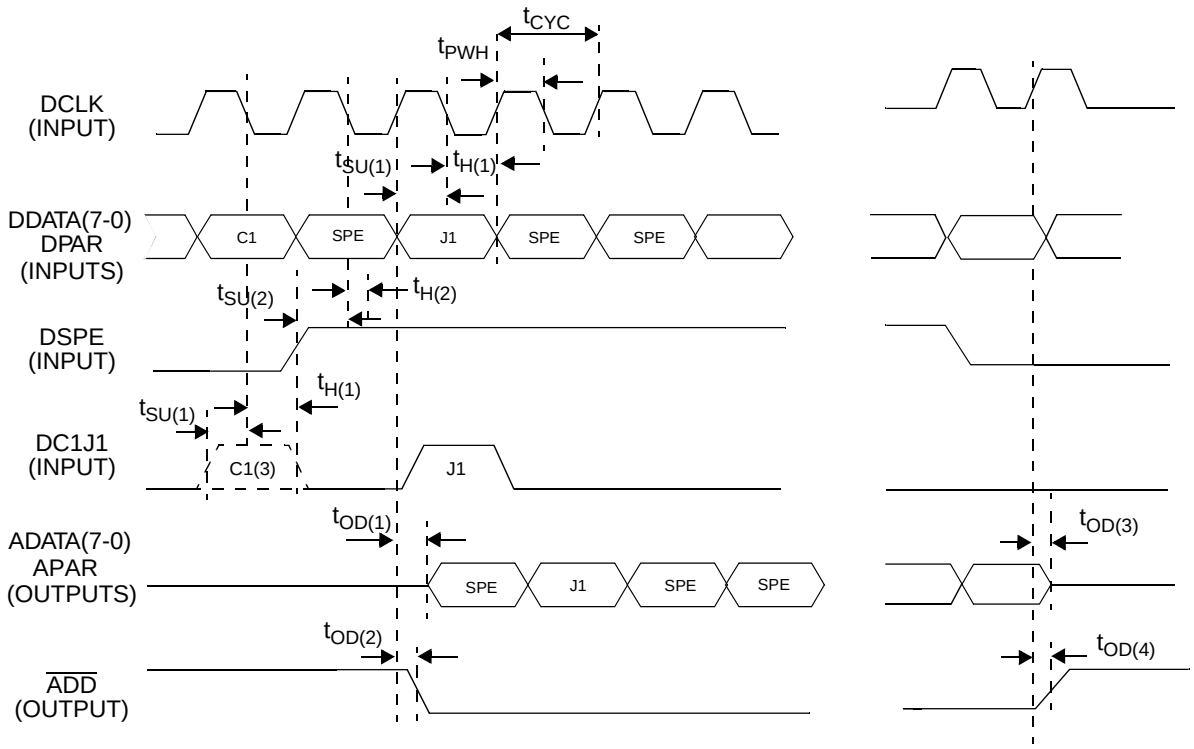
Figure 17. STS-3 Add/Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STS-3 format, there will be three J1 pulses with each J1 pulse indicating the start of an STS-1. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded. Shown is STS-1 number 1 being added to the Add bus.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
DDATA(7-0) data/DPAR/DC1J1 set-up time to DCLK↓	$t_{SU(1)}$	7.0			ns
DDATA(7-0) data/DPAR/DC1J1 hold time after DCLK↓	$t_{H(1)}$	3.0			ns
DSPE set-up time to DCLK↓	$t_{SU(2)}$	10.0			ns
DSPE hold time after DCLK↓	$t_{H(2)}$	5.0			ns
ADATA(7-0) data and APAR delay after DCLK↑	$t_{OD(1)}$	3.0		30	ns
$\overline{ADD}$ indicator delayed after DCLK↑	$t_{OD(2)}$	3.0		25	ns
ADATA(7-0) data and APAR tri-state after DCLK↑	$t_{OD(3)}$	12		25	ns
$\overline{ADD}$ indicator high after DCLK↑	$t_{OD(4)}$	12		25	ns

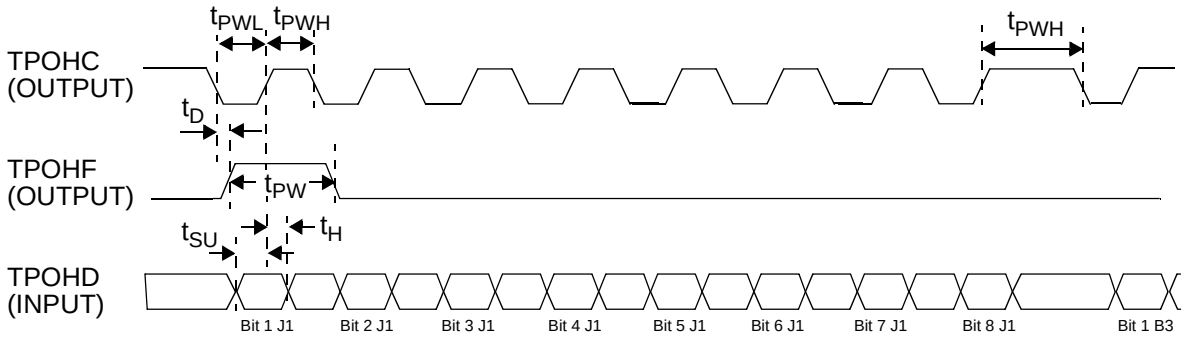
Figure 18. STS-1 Add/Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STS-1 format, there will be one J1 pulse which indicates the start of the STS-1. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		154.32		ns
DCLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
DDATA(7-0) data/DPAR/DC1J1 set-up time to DCLK↓	$t_{SU(1)}$	7.0			ns
DDATA(7-0) data/DPAR/DC1J1 hold time after DCLK↓	$t_{H(1)}$	3.0			ns
DSPE set-up time to DCLK↓	$t_{SU(2)}$	10.0			ns
DSPE hold time after DCLK↓	$t_{H(2)}$	5.0			ns
ADATA(7-0) data and APAR delay after DCLK↑	$t_{OD(1)}$	3.0		30	ns
$\overline{ADD}$ indicator delayed after DCLK↑	$t_{OD(2)}$	3.0		25	ns
ADATA(7-0) data and APAR tri-state after DCLK↑	$t_{OD(3)}$	12		25	ns
$\overline{ADD}$ indicator high after DCLK↑	$t_{OD(4)}$	12		25	ns

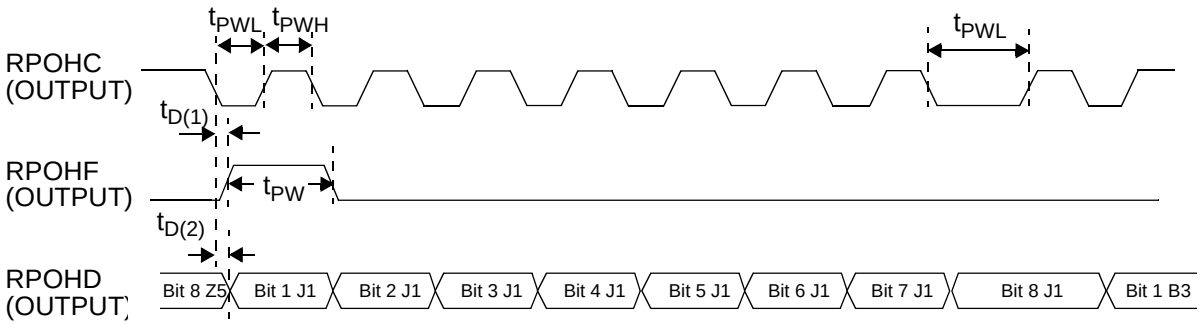
Figure 19. Transmit Path Overhead Timing



Note: The clock cycle that corresponds to bit 8 in each overhead byte is stretched.

Parameter	Symbol	Min	Typ	Max	Unit
TPOHC high time	t_{PWH}	617		3395	ns
TPOHC low time	t_{PWL}		771.7		ns
TPOHF output delay after TPOHC↓	t_D	-2.0		5.0	ns
TPOHD set-up time to TPOHC↑	t_{SU}	7.0			ns
TPOHD data hold time after TPOHC↑	t_H	3.0			ns
TPOHF pulse width	t_{PW}		1388.9		ns

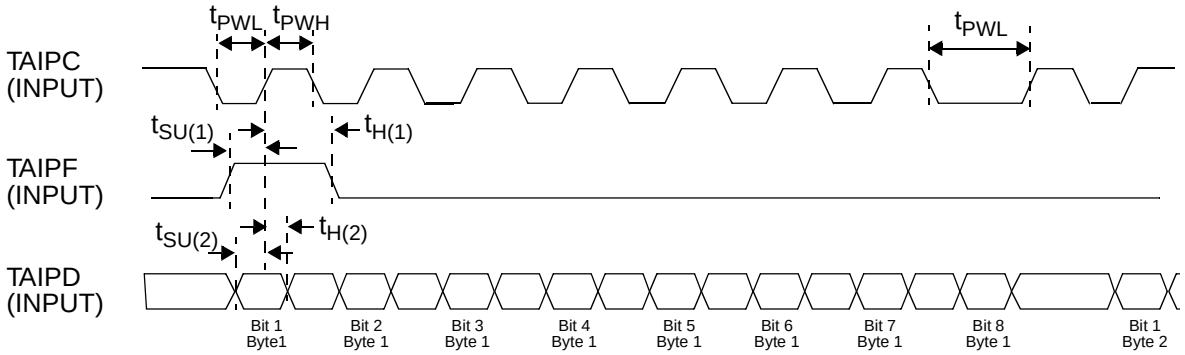
Figure 20. Receive Path Overhead Timing



Note: The clock cycle that corresponds to bit 8 in each overhead byte is stretched.

Parameter	Symbol	Min	Typ	Max	Unit
RPOHC low time	t_{PWL}	617		3395	ns
RPOHC high time	t_{PWH}		771.7		ns
RPOHF output delay after RPOHC↓	$t_{D(1)}$	-2.0		5.0	ns
RPOHD output delay after RPOHC↓	$t_{D(2)}$	-2.0		5.0	ns
RPOHF pulse width	t_{PW}		1388.9		ns

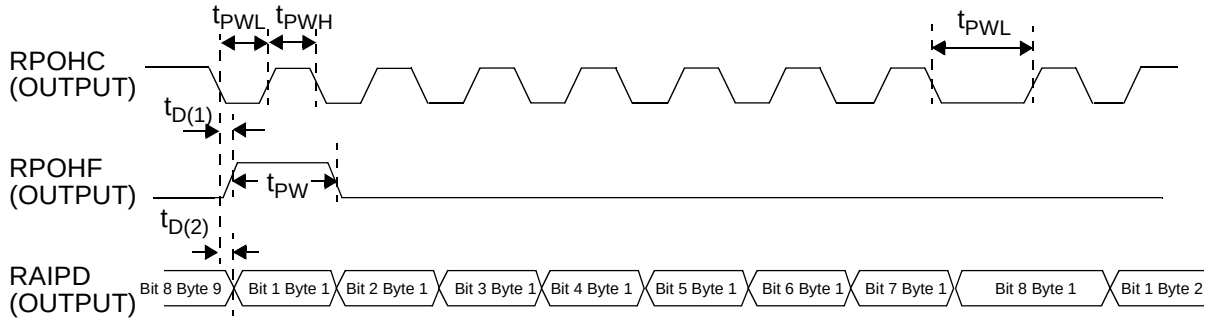
Figure 21. Transmit Alarm Indication Port Timing



Note: Alarm indication byte consists of eight bits and is repeated nine times. Bit 8 in each byte is stretched. The first four bits correspond to the FEBE count (bits 1 through 4 in G1), bit 5 is the path RDI value, and bits 6 and 7 are set to 0, while bit 8 is set to 1.

Parameter	Symbol	Min	Typ	Max	Unit
TAIPC low time	t_{PWL}	617		3395	ns
TAIPC high time	t_{PWH}		771.7		ns
TAIPF set-up time to TAIPC↑	$t_{SU(1)}$	7.0			ns
TAIPF hold time after TAIPC↑	$t_{H(1)}$	3.0			ns
TAIPD set-up time to TAIPC↑	$t_{SU(2)}$	7.0			ns
TAIPD set-up time after TAIPC↑	$t_{H(2)}$	3.0			ns

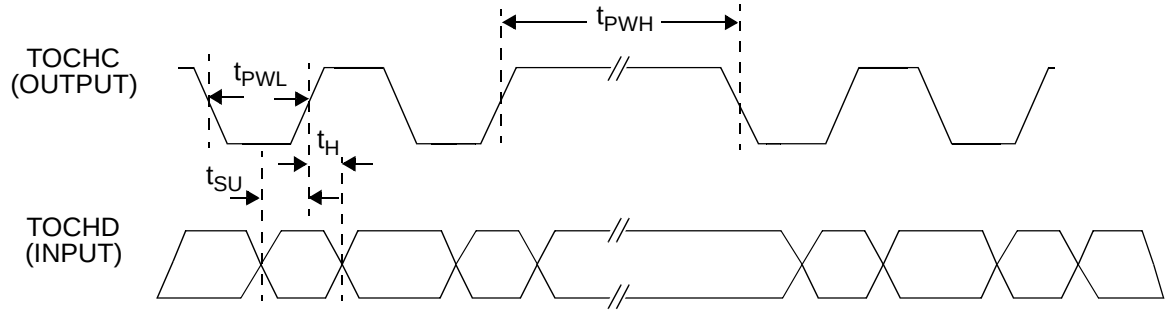
Figure 22. Receive Alarm Indication Port Timing



Note: Alarm indication byte consists of eight bits and is repeated nine times. Bit 8 in each byte is stretched. The first four bits correspond to the FEBE count (bits1 through 4 in G1), bit 5 is the path RDI value, and bits 6 and 7 are set to 0, while bit 8 is set to 1.

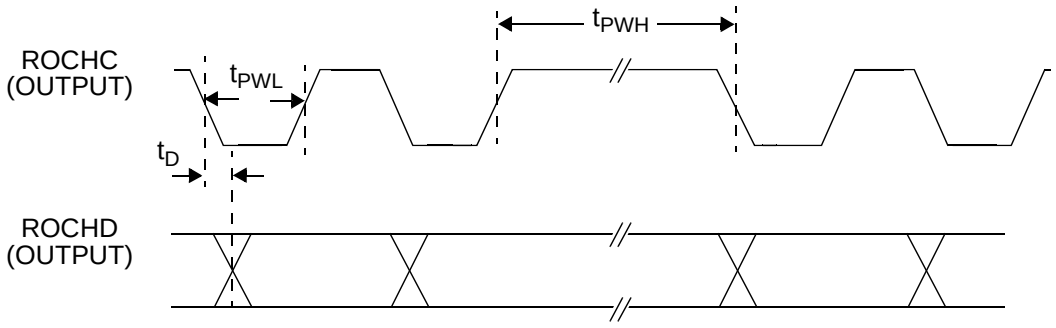
Parameter	Symbol	Min	Typ	Max	Unit
RPOHC low time	t_{PWL}	617		3395	ns
RPOHC high time	t_{PWH}		771.7		ns
RPOHF output delay after RPOHC↓	$t_{D(1)}$	-2.0		5.0	ns
RAIPD output delay after RPOHC↓	$t_{D(2)}$	-2.0		5.0	ns
RPOHF pulse width	t_{PW}		1388.9		ns

Figure 23. Transmit Overhead Communications Channel Timing



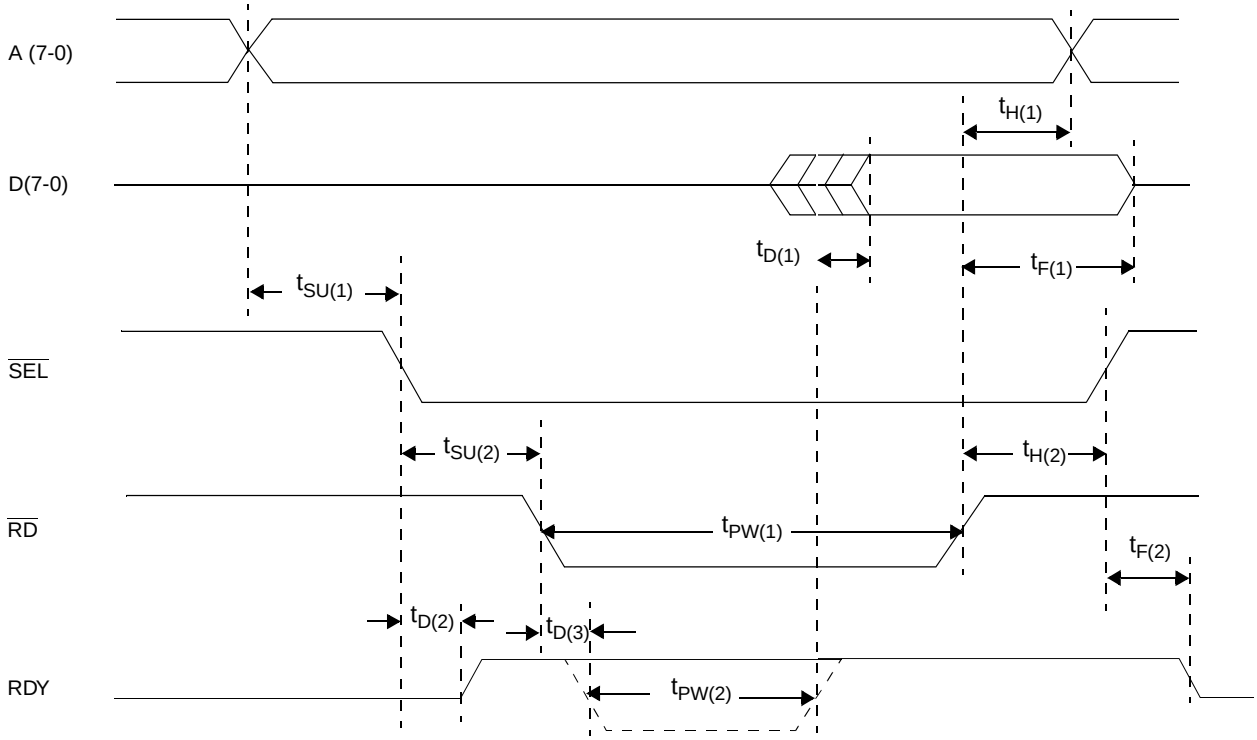
Parameter	Symbol	Min	Typ	Max	Unit
TOCHC high time	t_{PWH}	617		11729	ns
TOCHC low time	t_{PWL}		771.2		ns
TOCHD set-up time to TOCHC↑	t_{SU}	7.0			ns
TOCHD hold time after TOCHC↑	t_H	3.0			ns

Figure 24. Receive Overhead Communications Channel Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
ROCHC high time	t_{PWH}	617		11729	ns
ROCHC low time	t_{PWL}		771.2		ns
ROCHD output delay after ROCHC↓	t_D	-2.0		5.0	ns

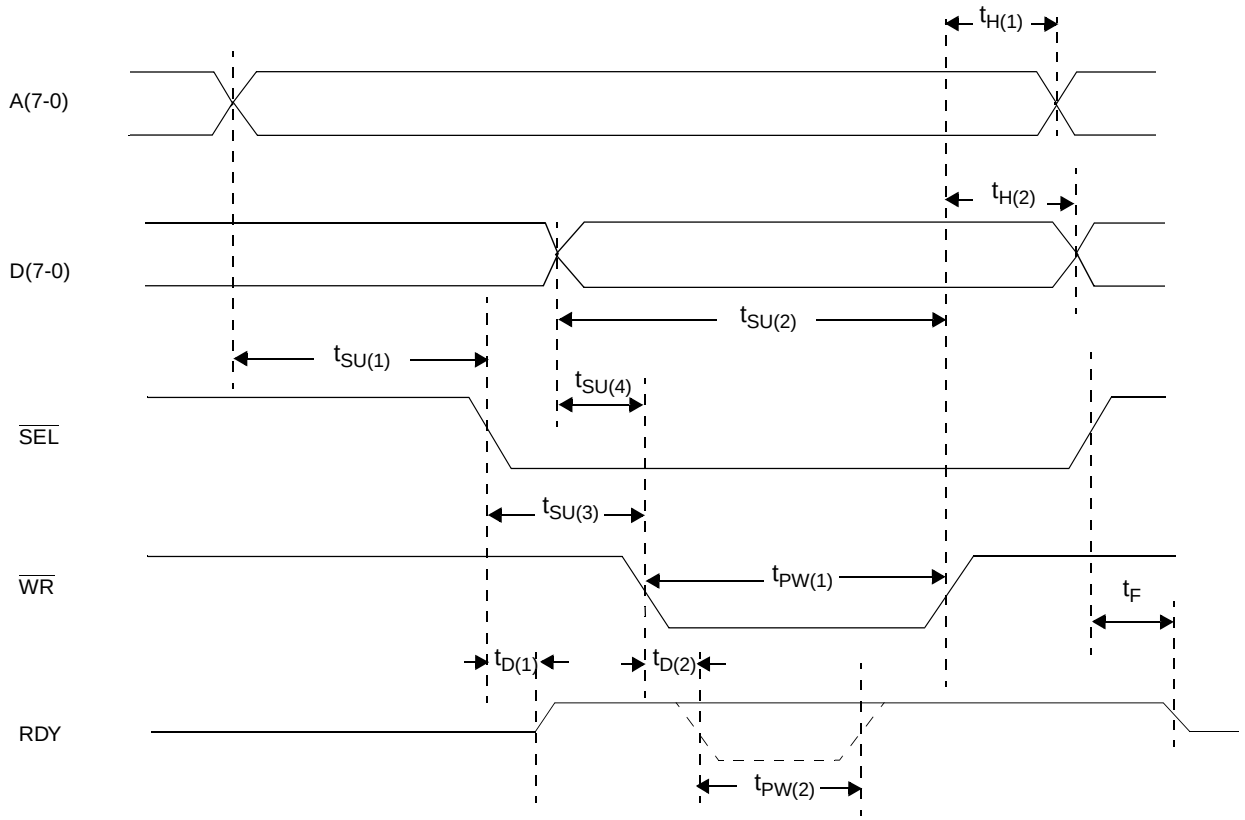
Figure 25. Intel Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	3.0			ns
A(7-0) address set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
D(7-0) data valid delay after RDY$\uparrow$	$t_{D(1)}$			7.0	ns
D(7-0) data float time after $\overline{RD}\uparrow$	$t_{F(1)}$			6.0	ns
$\overline{RD}$ pulse width	$t_{PW(1)}$	40.0			ns
$\overline{SEL}\downarrow$ set-up time to $\overline{RD}\downarrow$	$t_{SU(2)}$	10.0			ns
$\overline{SEL}\downarrow$ hold time after $\overline{RD}\uparrow$	$t_{H(2)}$	0.0			ns
RDY$\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			10.0	ns
RDY$\downarrow$ delay after $\overline{RD}\downarrow$	$t_{D(3)}$			16.0	ns
RDY pulse width *	$t_{PW(2)}$	0.0		48 * Rcyc	µs
RDY float time after $\overline{SEL}\uparrow$	$t_{F(2)}$			10.0	ns

* Note: RDY goes low when the address being read corresponds to a RAM location but remains high during status or control register access.
Rcyc is the period, in nanoseconds, of the RAM clock (RAMCI) (e.g., RAMCI @ 25MHz yields $t_{PW(2)}$ = 1.92µs max)

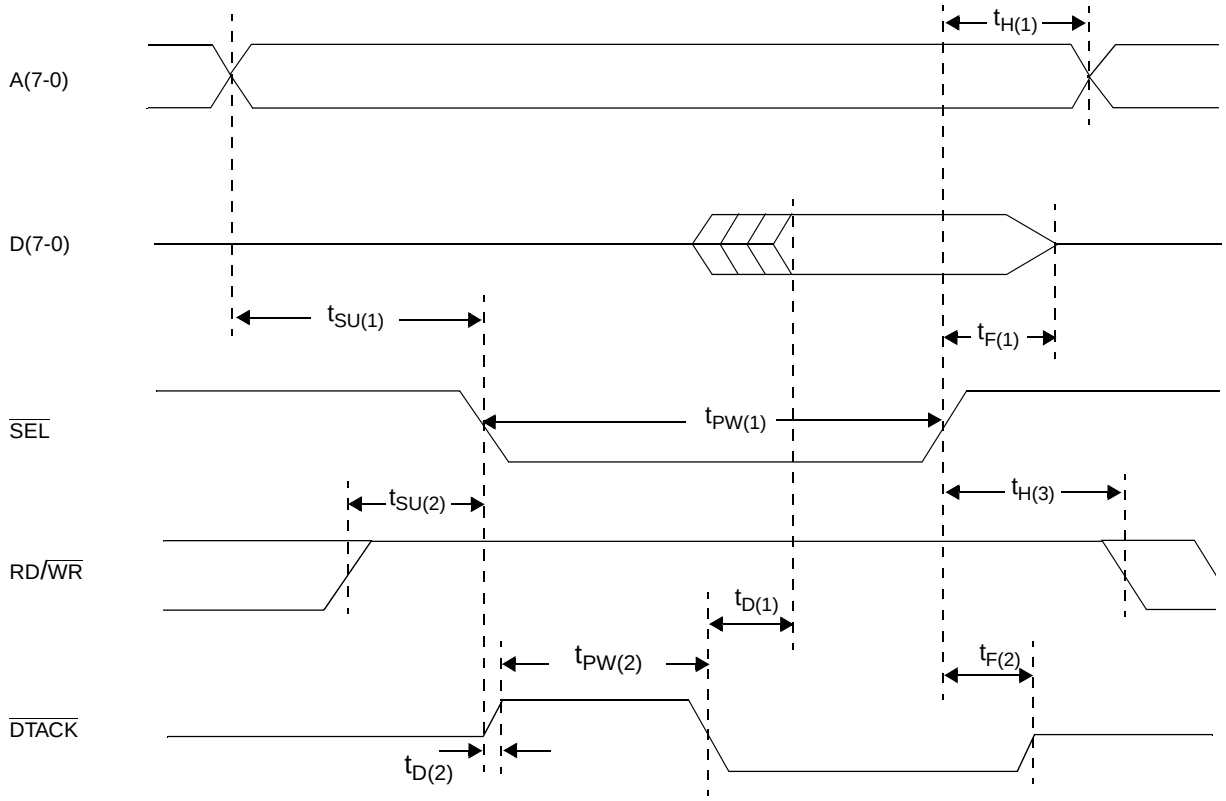
Figure 26. Intel Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	3.0			ns
A(7-0) address set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
D(7-0) data valid set-up time to $\overline{WR}\uparrow$	$t_{SU(2)}$	8.0			ns
D(7-0) data hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	6.0			ns
$\overline{SEL}\downarrow$ set-up time to $\overline{WR}\downarrow$	$t_{SU(3)}$	10.0			ns
$\overline{WR}$ pulse width	$t_{PW(1)}$	40.0			ns
RDY$\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(1)}$			10.0	ns
RDY$\downarrow$ delay after $\overline{WR}\downarrow$	$t_{D(2)}$			16.0	ns
RDY pulse width *	$t_{PW(2)}$	0.0		48 * Rcyc	ns
RDY float time after $\overline{SEL}\uparrow$	t_F			10.0	ns
RAM cycle D(7-0) valid set-up time to $\overline{WR}\downarrow$	$t_{SU(4)}$	-2 * Rcyc			ns

* Note: RDY goes low when the address being written to corresponds to a RAM location but remains high during status or control register access.
Rcyc is the period, in nanoseconds, of the RAM clock (RAMCI) (e.g., RAMCI @ 25MHz yields: $t_{SU(4)}$=-80ns min, $t_{PW(2)}$ = 1.92µs max)

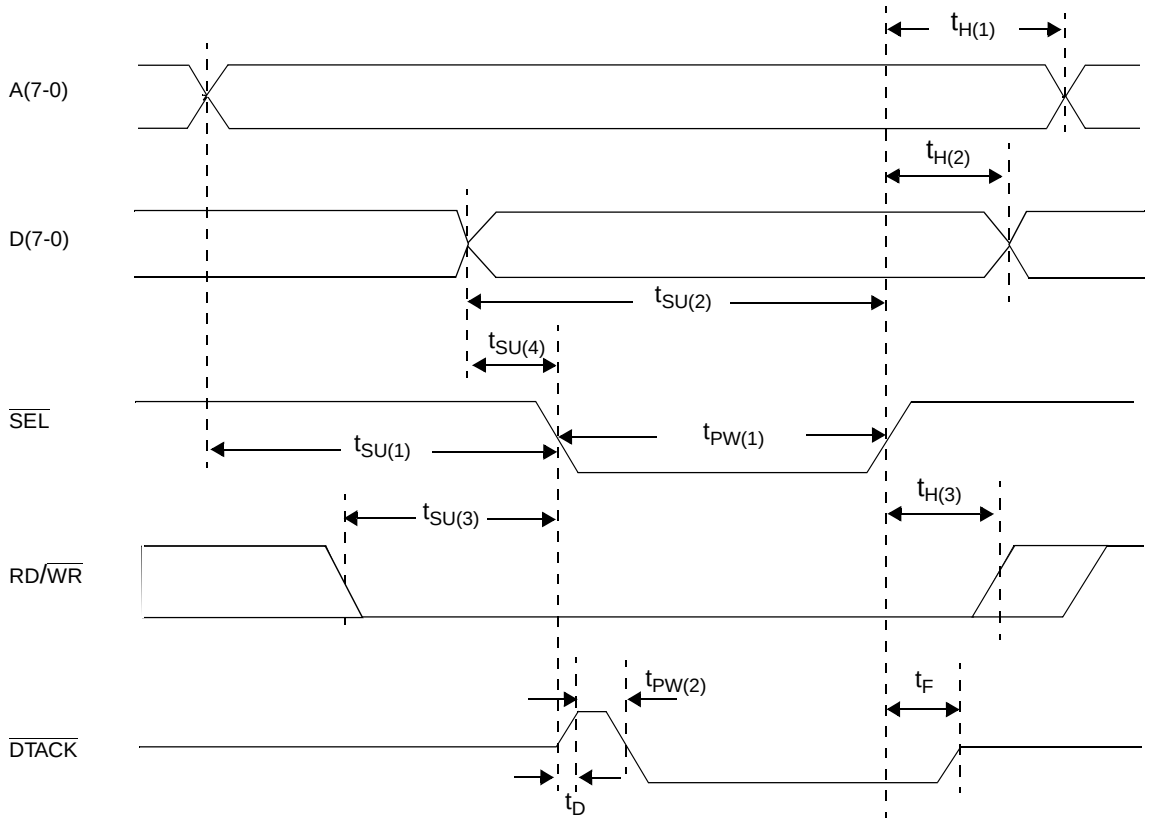
Figure 27. Motorola Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	3.0			ns
A(7-0) address valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10.0			ns
D(7-0) data valid delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$			5.0	ns
D(7-0) data float time after $\overline{SEL}\uparrow$	$t_{F(1)}$			6.0	ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	40.0			ns
RD/$\overline{WR}\uparrow$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	5.0			ns
RD/$\overline{WR}\uparrow$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	3.0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			16.0	ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0.0		48 * Rcyc	µs
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	$t_{F(2)}$			10.0	ns

Note: Rcyc is the period, in nanoseconds, of the RAM clock (RAMCI) (e.g., RAMCI @ 25 MHz yields $t_{PW(2)}$ = 1.92µs max).

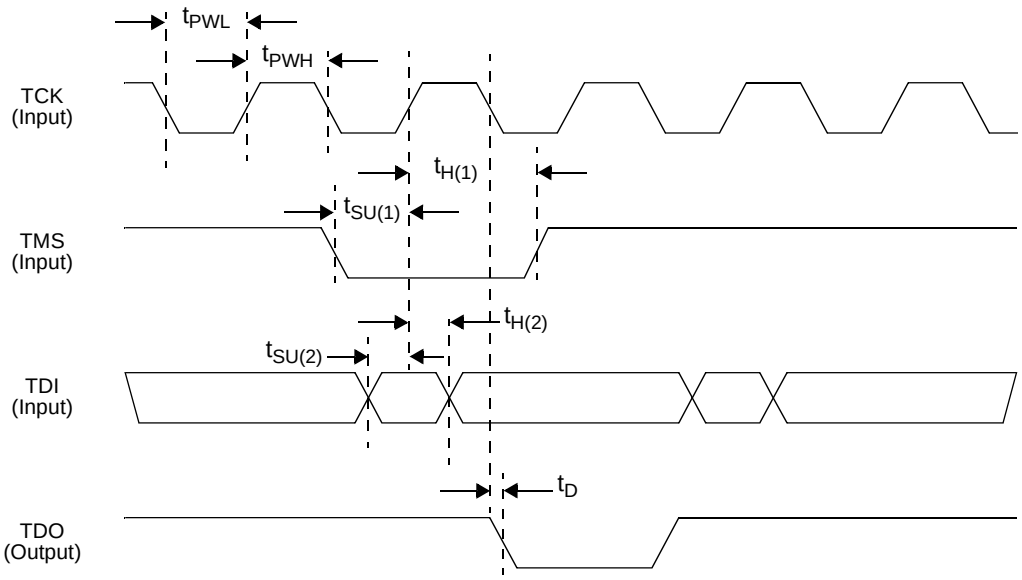
Figure 28. Motorola Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	3.0			ns
A(7-0) address valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10.0			ns
D(7-0) data valid set-up time to $\overline{SEL}\uparrow$	$t_{SU(2)}$	8.0			ns
D(7-0) data hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	6.0			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	40.0			ns
RD/$\overline{WR}\downarrow$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	5.0			ns
RD/$\overline{WR}\downarrow$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	3.0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	t_D			15.0	ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0.0		48 * Rcyc	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			10.0	ns
RAM cycle D(7-0) valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(4)}$	-2 * Rcyc			ns

Note: Rcyc is the period, in nanoseconds, of the RAM clock (RAMCI)
(e.g., RAMCI @ 25MHz yields: $t_{SU(4)}$=-80ns min, $t_{PW(2)}$ = 1.92µs max).

Figure 29. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time to TCK↑	$t_{SU(1)}$	3.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	5.0	-	ns
TDI setup time to TCK↑	$t_{SU(2)}$	6.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	5.0	-	ns
TDO output delay after TCK↓	t_D	-	10	ns

OPERATION

L3M POWER-UP RESET SEQUENCE

The L3M requires that the clocks are valid and stable for a minimum of 200 nanoseconds in order for a reset to take effect (refer to Hardware Reset function, $\overline{\text{RESET}}$, lead 86 or K14).

The sequence shown in Figure 30 is recommended on L3M power-up:

1. When a system reset is initiated, the L3M input leads $\overline{\text{RESET}}$ and $\overline{\text{TRI}}$ are set low at the same time.
2. The L3M $\overline{\text{RESET}}$ lead is held low for a minimum of 200 nanoseconds after the system reset has been completed and all of the L3M clocks have become stable.
3. The L3M $\overline{\text{TRI}}$ lead then remains low to hold the L3M outputs with tri-state capability in the tri-state condition until the TUG-3 position in register C0H has been programmed.
4. Once the L3M is programmed for the assigned TUG-3 in register C0H, the $\overline{\text{TRI}}$ lead is set high and the L3M will lock to the C1 pulse and map data to and from the positions selected by the DPOSn and APOSn settings.

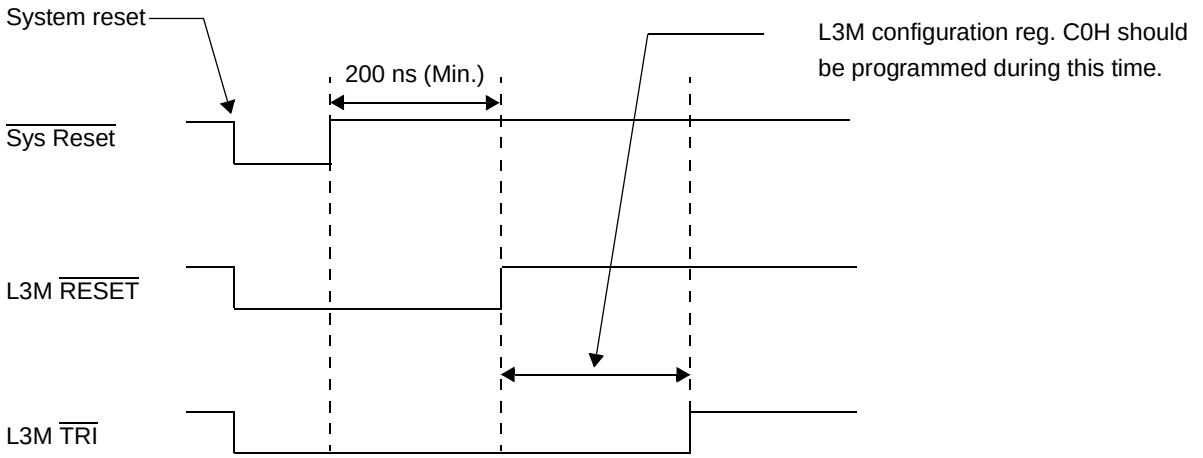
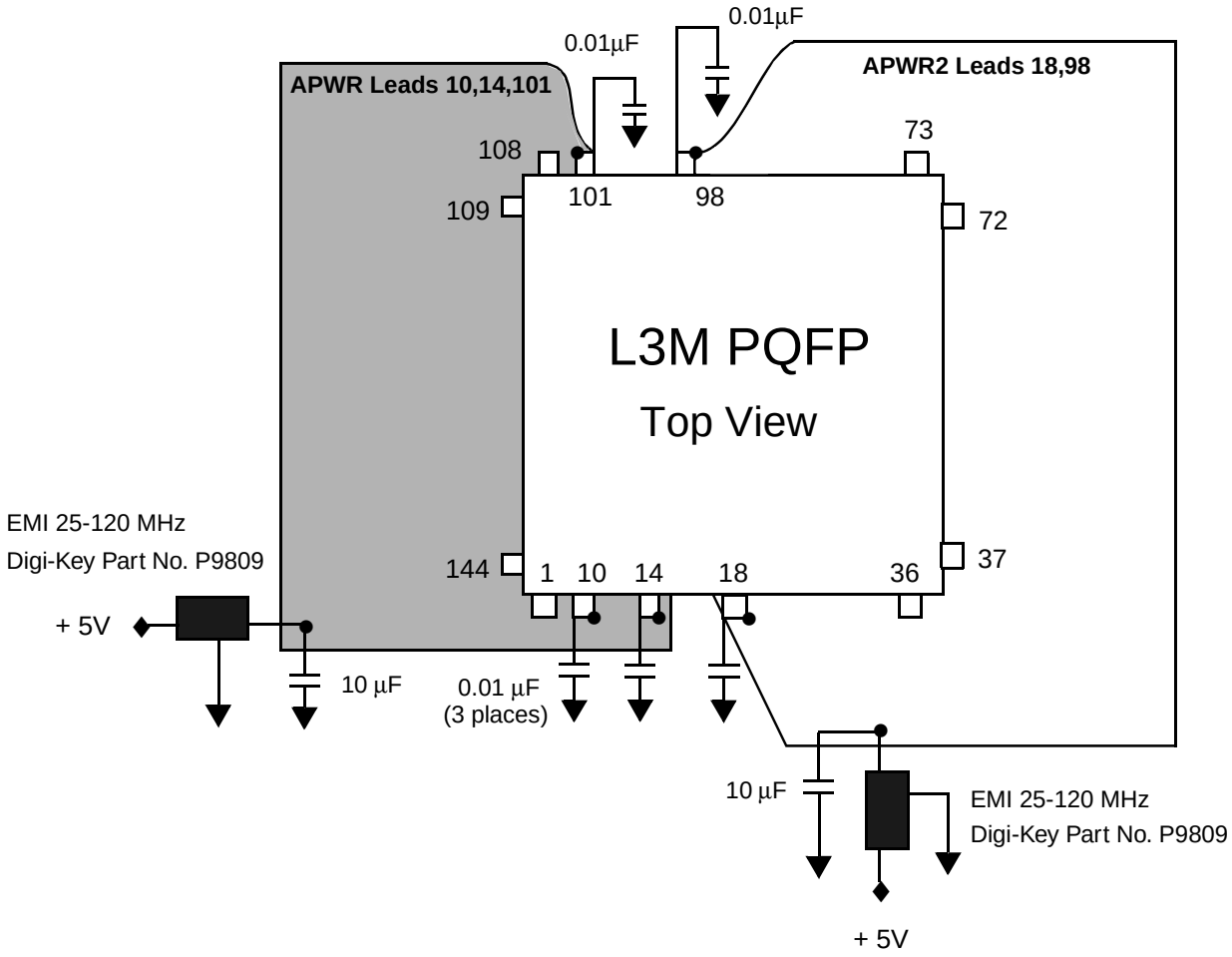


Figure 30. L3M Power-Up Reset Sequence

For application circuit boards that require the capability for hot insertion, a suitable circuit must be included to ensure that the L3M $\overline{\text{RESET}}$ and $\overline{\text{TRI}}$ input leads are forced low until the L3M power supply leads have all reached the normal operating voltage range.

It is important to remember that, when reading the latched registers in the L3M, the contents should be read a second time before determining the current status.

Figure 31. Physical Design For Analog Power Distribution



Note: The 10 µF capacitors may be polarized types.

Separate power islands should be used for APWR and APWR2, as shown in Figure 31. Traces should be kept as short as possible when connecting the EMI filter to the analog power planes. Place the 0.01 microfarad decoupling capacitors as close as possible to the associated device lead and on the same board side as the L3M. Place the 10 microfarad capacitors close to the EMI filters. Leads 1, 36, 37, 72, 73, 108, 109 and 144 are shown for reference only, they are not connected to the APWR or APWR2 power islands.

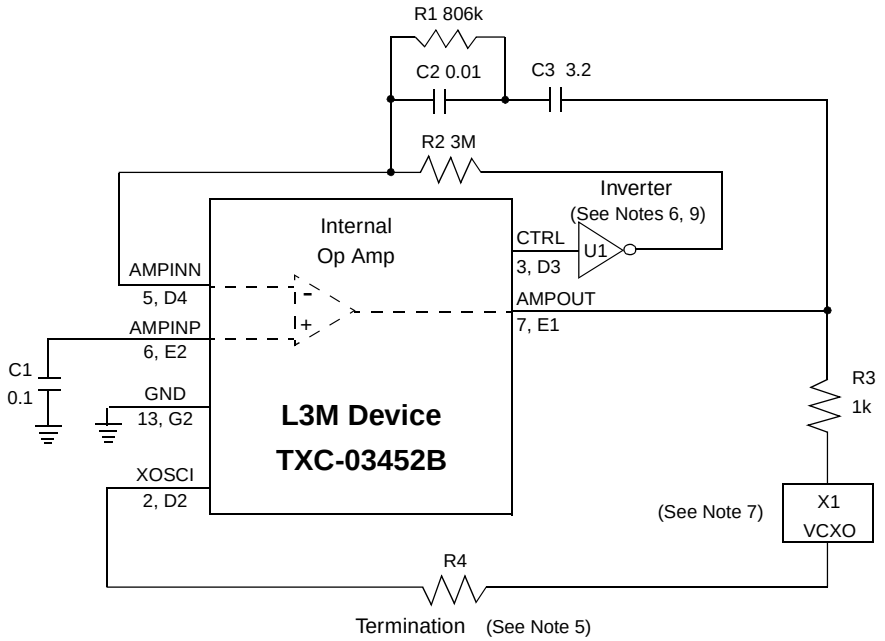
Similar design considerations apply to the PBGA package.

PLL FILTER CONNECTION TO VCXO

The Desynchronize Block in the receive line side path contains a phase-locked loop (PLL) circuit, which must be connected to an external voltage-controlled crystal oscillator (VCXO) via an external filter. This arrangement is designed to meet limits for jitter on the asynchronous line output signal, which is due to signal mapping and pointer movements.

Figure 32 shows the external filter circuit that is recommended for connecting the L3M PLL circuit to the VCXO. Figure 33 shows the jitter results obtained with the circuit shown in Figure 32.

Figure 32. PLL Connection to External VCXO



Notes:

1. The VCXO PLL filter design is a 2-pole integrator that is designed to supply reliable jitter performance and capture range with good margins for implementation in high volume production applications. Due to the characteristics of the filter network the signal at AMPOUT will go to a rail in the absence of a DS3/E3 signal in the SONET/SDH payload. In systems that experience extended Loss of Signal in the TUG-3/STS payload, this characteristic can cause long capture times, which can exceed 30 seconds.
2. This filter arrangement can be used for TUG-3/DS3, TUG-3/E3, STS-1/DS3 and STS-3/STS-1/DS3 mapping modes. It provides a bandwidth of 0.3 Hz for DS3 and 0.23 Hz for E3.
3. All resistance (Ω) and capacitance (µF) values must be within 5% and 10%, respectively, of the values shown to meet the requirements of Figure 33. Two components in series or parallel may be used, where needed.
4. All capacitors must be high quality, non-polarized ceramic types.
5. Termination resistor R4 must be chosen to suit the physical design adopted (e.g., 75 or 50 ohms).
6. Inverter U1 is a Signetics 74HCT04 or equivalent.
7. VCXO X1 is a Fordahl DFV 14-MHR 44.736 MHz V14112 or DFV 14-KHR 34.368 MHz V14111 or equivalent, depending on the application signal rate.
8. Setting the DIV4 bit (bit 4 in register C7) controls the gain of the phase detector. This bit must be set to 1.
9. Setting the INVCTRL bit (bit 3 in register C7) controls the polarity of the CTRL signal on lead 3 or D3. This bit must be set to 0 for the circuit shown, which provides the results tabulated in Figure 33. Control bit INVCTRL allows the use of an external circuit that does not include the inverter U1, if INVCTRL is set to 1.
10. Please contact the TranSwitch Applications Engineering Department if questions arise concerning the PLL filter design and characteristics.

L3M Jitter Results for STS-3/DS3 Mapping

Bellcore, GR-253-CORE, Rev. 2, Jan 1999	Maximum Measured Jitter (UI P-P)	Maximum Jitter Specified by GR-253-CORE (UI P-P)
Mapping Jitter	0.16	0.4
Single Pointer Adjustment	0.12	A0 + 0.3
Pointer Adjustment Burst	0.38	1.3
Phase Transient Pointer Adjustment Burst	0.19	1.2
Periodic Pointer Adjustments without added or canceled pointer adjustments	0.47 (T = 34 ms) 0.13 (T = 10 s)	1.0
Periodic Pointer Adjustments with added or canceled pointer adjustments	0.54 (T = 34 ms) 0.16 (T = 10 s)	1.3
Periodic Pointer Adjustments Continuous Pattern	0.08 (T = 34 ms) 0.14 (T = 10 s)	1.0
Periodic Pointer Adjustments Continuous Pattern with added or canceled pointer adjustment	0.17 (T = 34 ms) 0.24 (T = 10 s)	1.3

L3M Jitter Results for TUG-3/E3 Mapping

PA Sequence specified by ETSI document ETS-DE/TM-1015-1:Nov-93	Maximum Measured Jitter (UI P-P)		Maximum Allowed Jitter (UI P-P) Specified by ETS-DE/TM-1015-1:Nov-93	
	HP1/LP	HP2/LP	HP1/LP	HP2/LP
A	0.021	0.012		0.075
B	0.024	0.016	0.4	0.75
C	0.028	0.016	0.75	0.75
D	0.026	0.016	0.4	0.75
E	0.026	0.016	0.4	0.75

Figure 33. Jitter Results for STS-3/DS3 and TUG-3/E3 Mappings

TESTING

Loopbacks

Three loopback capabilities are provided: facility, line and SDH/SONET. Diagrams illustrating the three types of loopback are provided in the Memory Map Descriptions Section, Address C1, Bits 2-0.

Writing a 1 to control bit FLBK enables facility loopback. Facility loopback and line loopback operations are shown in Figure 34. When facility loopback is enabled, the internal DS3/E3 transmit signal becomes the internal receive signal. Either interface may be used, P/N rail or NRZ.

Line loopback is enabled by writing a 1 to control bit L3LBK. The DS3/E3 receive output becomes the transmit line input. The receive output may be P/N rail or NRZ.

Writing a 1 to control bit SLBK enables a SDH/SONET loopback. SDH/SONET loopback disables the STM-1/STS-3/STS-1 signal input on the drop bus, and enables the add signals to become the drop bus signals. The add signals are provided at the add bus.

Test Generators and Analyzers

Two pseudo-random binary sequence (PRBS) test generators are provided, as shown in Figure 34. Each generator can provide a 2^{15}-1 or 2^{23}-1 pseudo-random pattern. The test sequence of 2^{23}-1 is selected when a 1 is written into control bit PAT23. When PAT23 is 0, the pattern is 2^{15}-1.

The transmit test generator is enabled by writing a 1 to control bit TPRBS. When enabled, the transmit test generator transmits the pseudo-random pattern in place of transmit NRZ data. The transmit test generator must have a clock signal provided at the Transmit Line Clock (TCLK) input lead in order to generate a test pattern. For applications where no transmit line clock is present and the system is required to generate a transmit PRBS signal, a Loss of Clock detection circuit and a circuit to multiplex the transmit line clock and the AISCLK should be used externally to maintain a valid clock, as shown in Figure 34.

The receive test generator is enabled by writing a 1 to control bit RPRBS. When enabled, the receive test generator inserts the pseudo-random test pattern in place of the received desynchronized NRZ data.

The test analyzer is enabled by writing a 1 to control bit ENANA. The test sequence of 2^{23}-1 is selected when a 1 is written into control bit PAT23. Receive NRZ data is analyzed when a 0 is written to control bit TXANA. When a 1 is written to control bit TXANA, the transmit NRZ data path is monitored. The selection of the test analyzer disables the decoder CV output to the 16-bit counter. The 16-bit counter now counts received errors from the test analyzer, when the analyzer is in lock.

Figure 34. Loopbacks, Test Generators and Analyzer

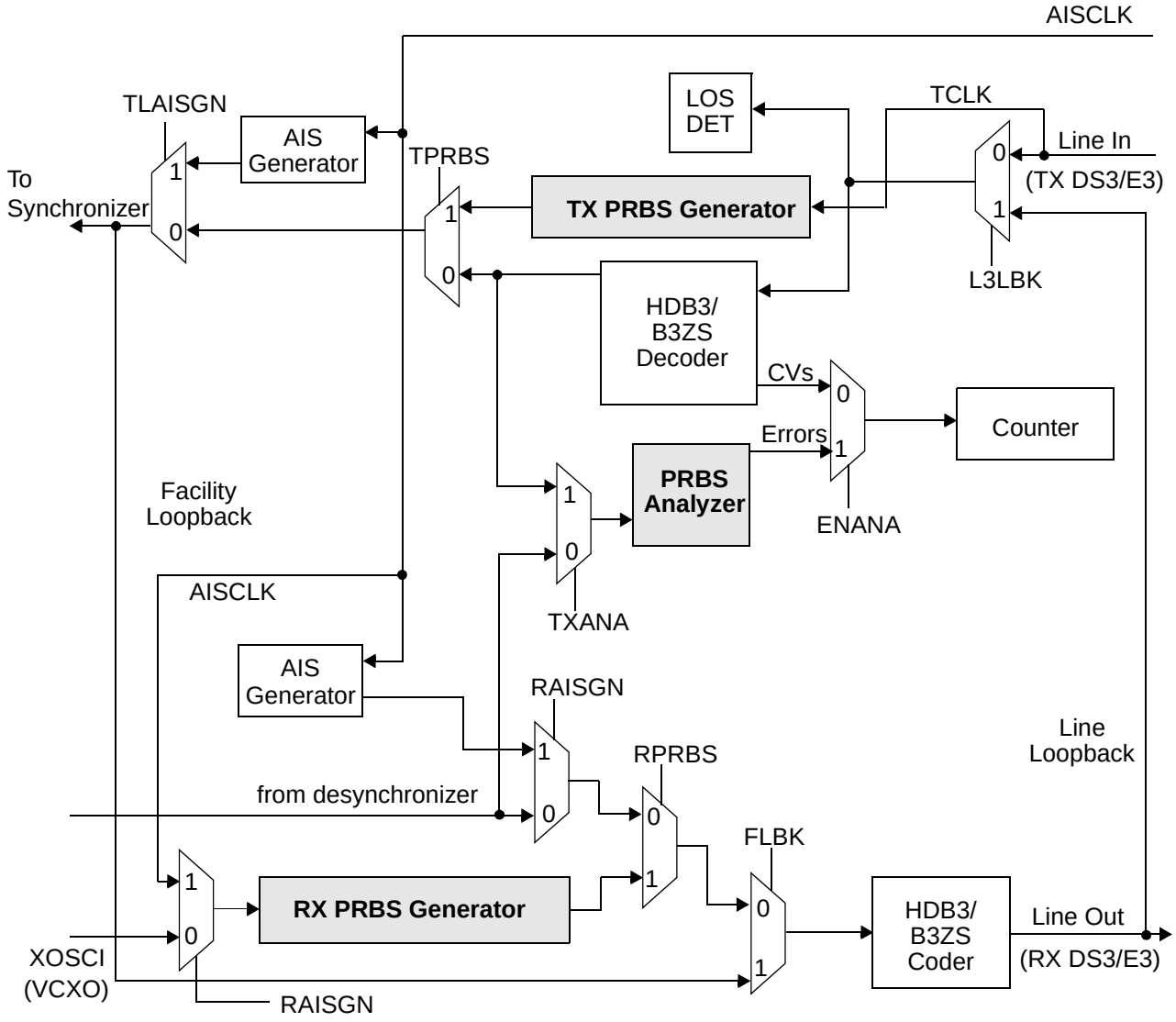
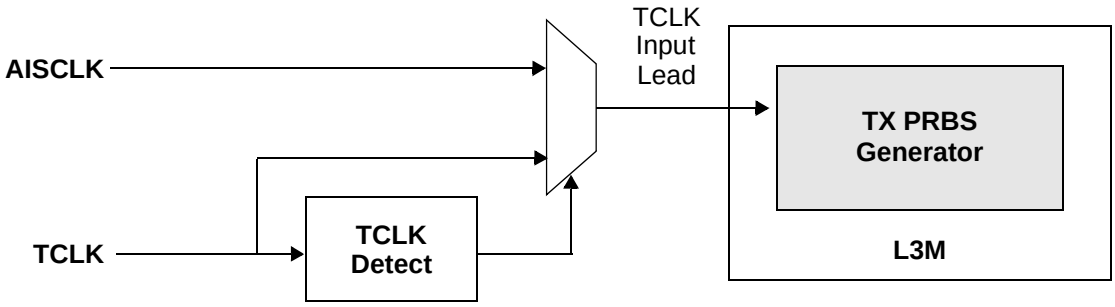


Figure 35. External Circuit to Maintain Clock Input to TX PRBS Generator



BOUNDARY SCAN

Introduction

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. As shown in Figure 36, one cell of a boundary scan register is assigned to each input or output lead to be observed or tested (bidirectional leads may have two cells). The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register bordering the input and output leads. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$)) and a Test Data Output (TDO) output signal. Boundary scan signal timing is shown in Figure 29.

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select (TMS) signal, and sends control signals to the internal scan paths. The TAP controller is reset by asserting the $\overline{\text{TRS}}$ lead low for a minimum of 5 nanoseconds. Detailed information on the operation of this state machine can be found in the IEEE 1149.1 standard. The serial scan path architecture consists of an instruction register, a boundary scan register and a bypass register. These three serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in Figure 36.

The boundary scan function will be reset and disabled by holding lead $\overline{\text{TRS}}$ low. When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the L3M device's internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations.

Boundary Scan Operation

The maximum frequency the L3M device will support for boundary scan is 10 MHz. The timing diagrams for the boundary scan interface leads are shown in Figure 29.

The instruction register contains three bits. The L3M device performs the following three boundary scan test instructions:

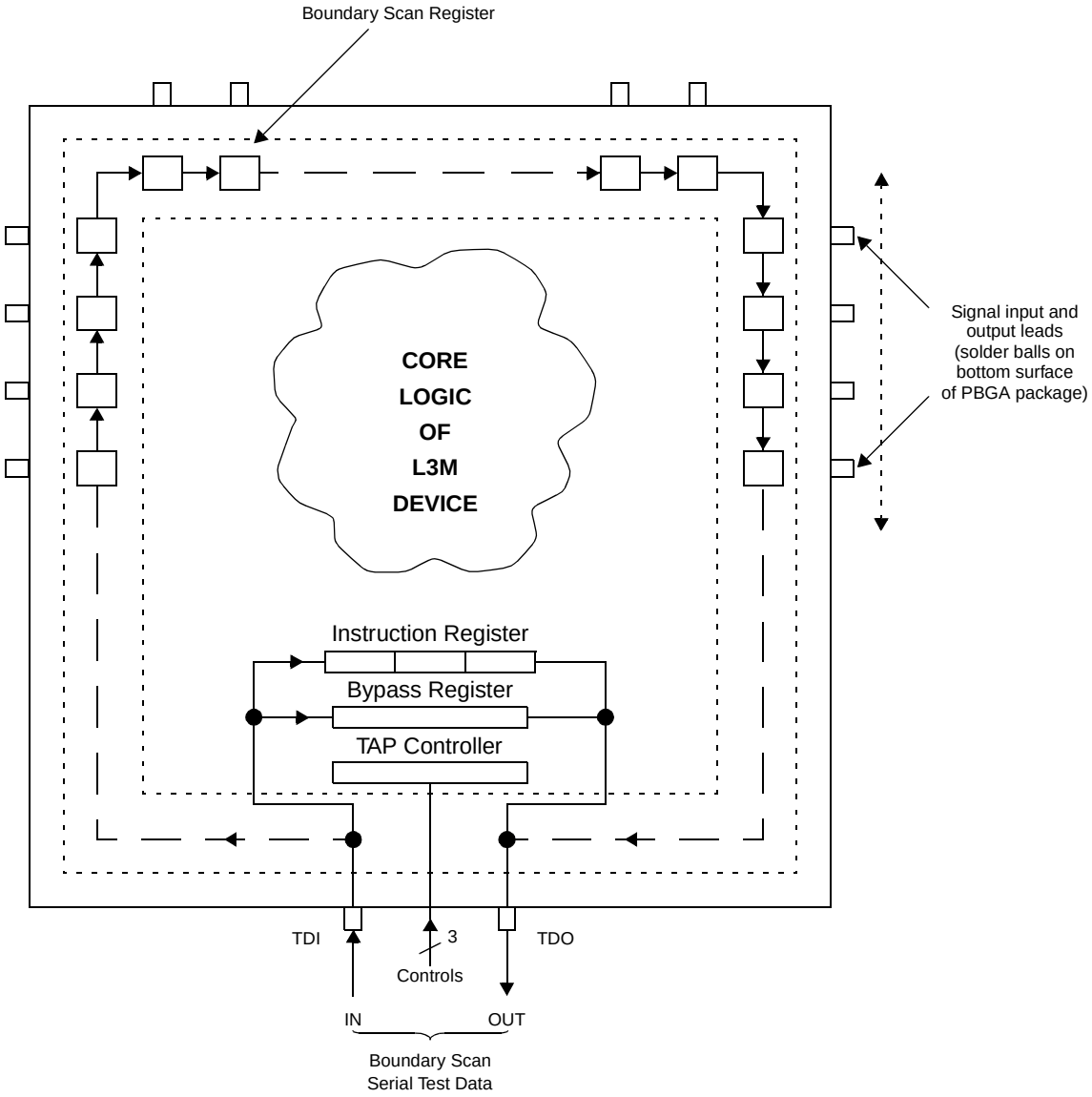
The EXTEST test instruction (000) provides the ability to test the connectivity of the L3M device to external circuitry.

The SAMPLE test instruction (010) provides the ability to examine the boundary scan register contents without interfering with device operation.

The BYPASS test instruction (111) provides the ability to bypass the L3M boundary scan and instruction registers.

During the *Capture - IR* state, a fixed value (101) is loaded into the instruction register.

Figure 36. Boundary Scan Schematic



Boundary Scan Chain

There are 104 scan cells in the L3M boundary scan chain. Bidirectional signals require two scan cells. Additional scan cells are used for direction control as needed. A boundary scan description language (BSDL) source file for each package type is available via the Products page of the TranSwitch World Wide Web site (www.transwitch.com). The following table shows the listed order of the scan cells and their function.

Scan Cell No.	Input/Output	PQFP (PBGA) Lead No.	Symbol	Comments
103	Input	107 (D16)	$\overline{\text{TRI}}$	See Note 1 (at end of table).
102	---	---	(L3 out ctrl)	When low, leads 92 (H13), 93 (H14), 142 (B3), 143 (A2) and 144 (A1) are set to a high impedance state. See Note 1.
101	Input	109 (C14)	TPOS	
100	Input	110 (A15)	TNEG	
99	Input	111 (A14)	TCLK	
98	Input	113 (A13)	A0	
97	Input	114 (D13)	A1	
96	Input	115 (B12)	A2	
95	Input	116 (C12)	A3	
94	Input	117 (D12)	A4	
93	Input	118 (B11)	A5	
92	Input	119 (C11)	A6	
91	Input	120 (D11)	A7	
90	Input	122 (A10)	$\overline{\text{WR}}$	
89	Input	123 (C10)	$\overline{\text{RD}}$ or RD/$\overline{\text{WR}}$	
88	---	---	(Rdy Ctrl)	When low, lead 128 (C8) is set to a high impedance state. See Note 1.
87	Input	124 (D10)	$\overline{\text{SEL}}$	
86	Output (3-state)	128 (C8)	RDY/$\overline{\text{DTACK}}$	
85	Output (3-state)	129 (B8)	INT/$\overline{\text{IRQ}}$	
84	---	---	(µP D(7-0) Ctrl)	When low, leads 133 thru 140 (C4, B5, A5, C5, B6, A6, C6 and D6) are set to a high impedance state. See Note 1.
83	Input	130 (C7)	RAMCI	
82	---	---	(INT/$\overline{\text{IRQ}}$ Ctrl)	When low, lead 129 (B8) is set to a high impedance state. See Note 1.

Scan Cell No.	Input/Output	PQFP (PBGA) Lead No.	Symbol	Comments
81	Input	131 (B7)	MOTO	
80	Output (3-state)	133 (D6)	D0 (out)	
79	Input	133 (D6)	D0 (in)	
78	Output (3-state)	134 (C6)	D1 (out)	
77	Input	134 (C6)	D1 (in)	
76	Output (3-state)	135 (A6)	D2 (out)	
75	Input	135 (A6)	D2 (in)	
74	Output (3-state)	136 (B6)	D3 (out)	
73	Input	136 (B6)	D3 (in)	
72	Output (3-state)	137 (C5)	D4 (out)	
71	Input	137 (C5)	D4 (in)	
70	Output (3-state)	138 (A5)	D5 (out)	
69	Input	138 (A5)	D5 (in)	
68	Output (3-state)	139 (B5)	D6 (out)	
67	Input	139 (B5)	D6 (in)	
66	Output (3-state)	140 (C4)	D7 (out)	
65	Input	140 (C4)	D7 (in)	
64	Output (3-state)	143 (A2)	RPOS	
63	Output (3-state)	144 (A1)	RNEG	
62	Input	1 (C2)	AISCLK	
61	Input	2 (D2)	XOSCI	
60	Output (2-state)	3 (D3)	CTRL	
59	Output (2-state)	8 (E3)	NC	Not used
58	Output (2-state)	11 (F3)	FIFOERR	
57	Output (2-state)	21 (J2)	NC	Not used
56	Output (2-state)	22 (K4)	NC	Not used
55	Output (2-state)	25 (L4)	ROCHD	
54	Output (2-state)	26 (L3)	ROCHC	
53	Output (2-state)	28 (L2)	RAIPD	
52	Output (2-state)	30 (M3)	RPOHD	

Scan Cell No.	Input/Output	PQFP (PBGA) Lead No.	Symbol	Comments
51	Output (2-state)	31 (M1)	RPOHF	
50	Output (2-state)	32 (M2)	RPOHC	
49	Output (2-state)	35 (N2)	NC	Not used
48	Output (2-state)	36 (P1)	NC	Not used
47	Input	40 (R4)	DDATA7	
46	Input	41 (T4)	DDATA6	
45	Input	42 (N4)	DDATA5	
44	Input	43 (T5)	DDATA4	
43	Input	44 (P5)	DDATA3	
42	Input	45 (R6)	DDATA2	
41	Input	46 (T6)	DDATA1	
40	Input	47 (N6)	DDATA0	
39	Input	49 (R7)	DC1	
38	Input	50 (T7)	DPAR	
37	Input	51 (P7)	DCLK	
36	Input	52 (N7)	DC1J1	
35	Input	53 (R8)	DSPE	
34	Output (3-state)	57 (T9)	APAR	
33	Output (3-state)	58 (R9)	ASPE	
32	Input	58 (R9)	ASPE	
31	Output (3-state)	59 (N10)	AC1J1	
30	Input	59 (N10)	AC1J1	
29	Output (2-state)	60 (T10)	$\overline{\text{ADD}}$	
28	Output (3-state)	61 (R10)	ACLK	
27	Input	61 (R10)	ACLK	
26	Output (3-state)	63 (N11)	ADATA7	
25	Output (3-state)	64 (T11)	ADATA6	
24	Output (3-state)	65 (R11)	ADATA5	
23	Output (3-state)	66 (P12)	ADATA4	
22	Output (3-state)	67 (T12)	ADATA3	

Scan Cell No.	Input/Output	PQFP (PBGA) Lead No.	Symbol	Comments
21	Output (3-state)	68 (P13)	ADATA2	
20	Output (3-state)	69 (R13)	ADATA1	
19	Output (3-state)	70 (T14)	ADATA0	
18	---	---	(APAR, ADATA(7-0) Ctrl)	When low, leads 57 (T9), 63 thru 70 (N11, T11, R11, P12, T12, P13, R13 and T14) are set to a high impedance state. See Note 1.
17	Input	75 (N13)	XCLKI	
16	---	---	(SPE Ctrl)	When low, leads 58 (R9), 59 (N10), and 61 (R10) are set to a high impedance state. See Note 1.
15	Input	76 (M15)	XC1	
14	Input	77 (M16)	XCLKE	
13	Output (2-state)	79 (M13)	TPOHC	
12	Output (2-state)	80 (L15)	TPOHF	
11	Input	81 (L16)	TPOHD	
10	Input	83 (L13)	TAIPC	
9	Input	84 (K15)	TAIPF	
8	Input	85 (K16)	TAIPD	
7	Input	86 (K14)	$\overline{\text{RESET}}$	
6	Output (2-state)	90 (J14)	TOCHC	
5	Input	91 (J13)	TOCHD	
4	Output (3-state)	92 (H13)	RNRZD	
3	Output (3-state)	93 (H14)	RNRZC	
2	Input	94 (H16)	STAI	
1	Input	95 (H15)	PAIS	
0	Input	96 (G13)	ISTAT	

Note 1: All outputs are disabled when the High Impedance Enable input ($\overline{\text{TRI}}$, lead 107 (D16)) is low, except during EXTEST, when the direction control Scan Cells (numbers 16 (H2), 18 (J4), 82 (L14), 84 (K15), 88 (J15), 102 (E13) and 103 (E14)) take precedence.

MEMORY MAP

Please note that all control registers (C0H to CAH) and the FIFO Leak Rate Register (A0H) must be initialized to 00H value unless otherwise specified below or required by the application.

CONTROL BITS

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C0	R/W	TUG3	STS3	DPOS1	DPOS0	APOS1	APOS0	TEST	DS3
C1	R/W	DECODE	CODE	INVCI	INVCO	RING	FLBK	L3LBK	SLBK
C2	R/W	ALM2AIS	ALM2FB9	TLAISGN	TPAISGN	TPAIS00	INTZ	ADDZ	L3Z
C3	R/W	EXZ5	EXZ4	EXZ3	EXH4	EXF2	EXG1	EXC2	EXJ1
C4	R/W	EXOO	FEBE9EN	RAMRDI	FEBEEN	XALM2AIS	TEST	TLOC2AIS	TLOS2AIS
C5	R/W	COR	TEST	DROPT	POH2RAM	RAISGN	RAISEN	WGDEC	PSL2AIS
C6	R/W	FASTPTR	TOHOUT	H4CTR	PAT23	ENANA	TXANA	TPRBS	RPRBS
C7	R/W	TESTB3	FIXPTR	TEST	DIV4	INVCTRL	TXRST	RXRST	RESETC
C8	R/W	C2 Compare							
C9	R/W	TEST						RDI5	FEBEBLK
CA	R/W	TEST		NOPOH	TEST				

STATUS BITS

Address (Hex)**	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B0	R	DLOC	DLOJ1	BUSERR	E1AIS	LOP	PAIS	PSLERR	C2EQ0
B1	R/W(L)	DLOC	DLOJ1	BUSERR	E1AIS	LOP	PAIS	PSLERR	C2EQ0
B2	R	RDI	L3LOS	L3LOC	TOVFL	L3AIS	RAMLOC	ALOC	ALOJ1
B3	R/W(L)	RDI	L3LOS	L3LOC	TOVFL	L3AIS	RAMLOC	ALOC	ALOJ1
B4	R	SINT	FEBE9	NEW	TUG3NEW	ROVFL	XSTAI	XISTAT	XPAIS
B5	R/W(L)	Reserved	FEBE9	NEW	TUG3NEW	ROVFL	XSTAI	XISTAT	XPAIS
B6	R	L3ERR	LOVFL	RFRST	TFRST	VCXOLOC	TPLOC	RPLOC	OOL
B7	R/W(L)	L3ERR	LOVFL	RFRST	TFRST	VCXOLOC	TPLOC	RPLOC	OOL

*R/W: Read/write; R: Read only; R/W(L): Read/Write - latched register.
**Even addresses contain unlatched status bits. Odd addresses contain latched status bits.

INTERRUPT MASK BITS

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BA	R/W	DLOC	DLOJ1	BUSERR	E1AIS	LOP	PAIS	PSLERR	C2EQ0
BB	R/W	RDI	L3LOS	L3LOC	TOVFL	L3AIS	RAMLOC	ALOC	ALOJ1
BC	R/W	HINT	FEBE9	NEW	TUG3NEW	ROVFL	XSTAI	XISTAT	XPAIS
BD	R/W	L3ERR	LOVFL	RFRST	TFRST	VCXOLOC	TPLOC	RPLOC	OOL

TRANSMIT POH BYTES & "O"-BITS

J1	B3 Error Mask and Test	C2	G1	F2	H4	Z3 (F3)	Z4 (K3)	Z5 (N1)	Not used	"O"-bits
00-3F	40	41	42	43	44	45	46	47	48	49 Bits 1-0

RECEIVE POH BYTES, TUG-3 H1/H2 BYTES & "O"-BITS

J1	B3	C2	G1	F2	H4	Z3 (F3)	Z4 (K3)	Z5 (N1)	H1	H2	"O"-bits
50-8F	90	91	92	93	94	95	96	97	98	99	9A Bits 1-0

PERFORMANCE COUNTERS & FIFO LEAK RATE

RCV Frame Count	Not used	FIFO Leak Rate	INC Count	DEC Count	NDF Count	TUG-3 INC Count	TUG-3 DEC Count
A0	A1	A2	A3	A4	A5	A6	A7

TUG-3 New Data Flag Count	B3 Block Error Count	FEBE Count	B3 Error Count	Line CV/PRBS Error Count	Common High Byte (FEBE, B3, CVs)
A8	A9	AA	AC	AE	FF

DEVICE IDENTIFICATION

The device identification (ID) is based on the manufacturer identity, part-number and version codes described in IEEE standard 1149.1 on Boundary Scan, using the manufacturer code assigned by the Joint Electron Device Engineering Council (JEDEC). The serial format for this ID is shown below:

MSB LSB

Version (TBD)	Part-Number 0000 1101 0111 1100	Manufacturer Identity 000 0110 1011	Fixed Bit 1
4 bits	16 bits	11 bits	1 bit

The device identification is not currently provided as a boundary scan message. However, the manufacturer identity and part-number are implemented with read-only capability for microprocessor read access. The manufacturer identity for TranSwitch devices is 107 (06B hex.). The part-number of the L3M device is 03452 (0D7C hex.). In addition, the read-only segment is expanded to include a 4-bit mask level field and a 4-bit future growth field, as shown below:

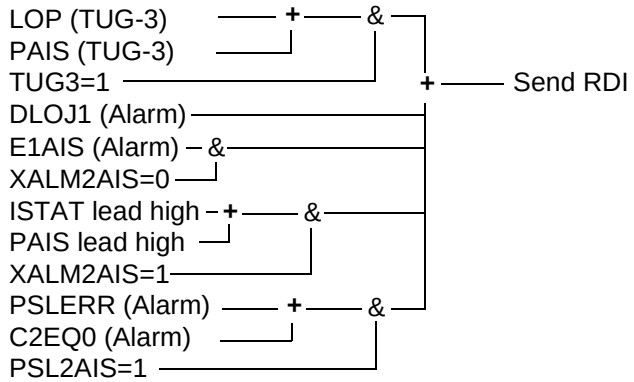
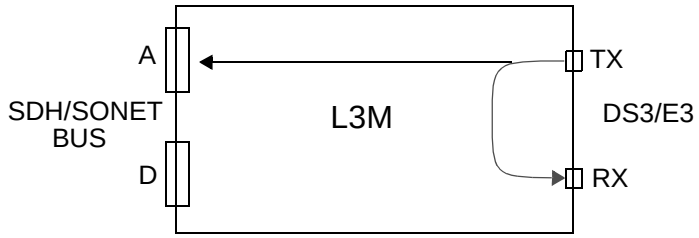
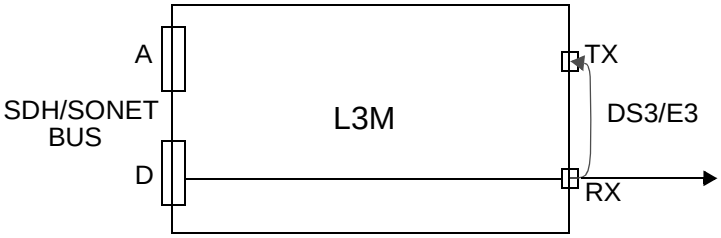
Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F4	R	Mask Level - Content TBD				Growth - Content TBD			
F3	R	Revision (Version) Level - Content TBD				PN15=0	PN14=0	PN13=0	PN12=0
F2	R	PN11=1	PN10=1	PN9=0	PN8=1	PN7=0	PN6=1	PN5=1	PN4=1
F1	R	PN3=1	PN2=1	PN1=0	PN0=0	MI10=0	MI9=0	MI8=0	MI7=0
F0	R	MI6=1	MI5=1	MI4=0	MI3=1	MI2=0	MI1=1	MI0=1	1

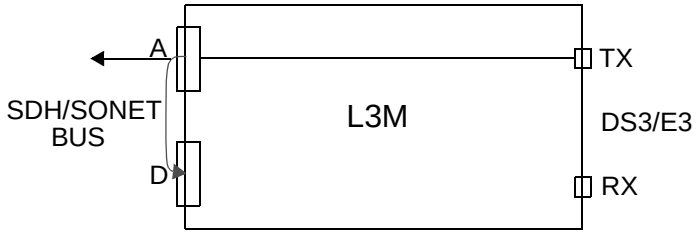
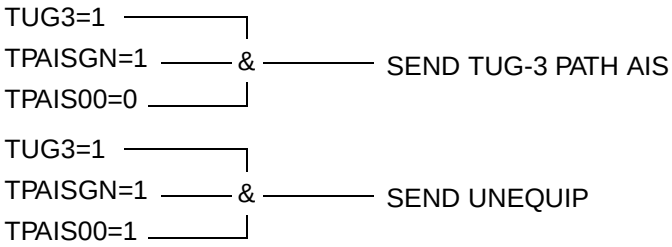
MEMORY MAP DESCRIPTIONS

CONTROL BITS

On power-up, the control bits will not be automatically initialized to a fixed default pattern. The microprocessor must write the control bits to the required system status. The control bits are not affected by either hardware or software resets.

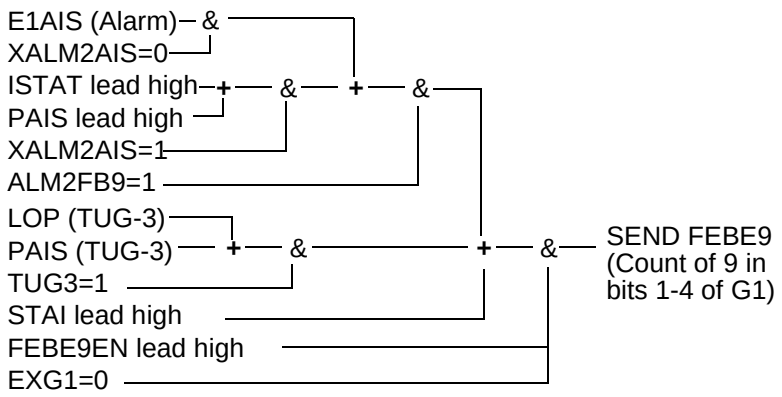
Address	Bit	Symbol	Description
C0	7, 6	TUG3, STS3	**Bus Format Control Bits:** Determine the bus format according to the table given below: TUG3 STS3 Mapping 0 0 STS-1 0 1 STS-3 1 0 Future Use 1 1 TUG-3
	5, 4	DPOS1,0	**Drop Positions 1 and 0:** Determine the locations of the TUG-3s and AU-3/STS-1 SPEs dropped from the STM-1/STS-3 according to the table given below: DPOS1 DPOS0 Mapping 0 0 TUG-3 position A (or STS-1 #1) 0 1 TUG-3 position B (or STS-1 #2) 1 0 TUG-3 position C (or STS-1 #3) 1 1 Idle state. RX front end held in reset.
	3, 2	APOS1,0	**Add Positions 1 and 0:** Determine the locations of the TUG-3s and AU-3/STS-1 SPEs to be added to the STM-1/STS-3 according to the table given below: APOS1 APOS0 Mapping 0 0 TUG-3 position A (or STS-1 #1) 0 1 TUG-3 position B (or STS-1 #2) 1 0 TUG-3 position C (or STS-1 #3) 1 1 Undefined
	1	TEST	**TEST**: A 0 must be written into this location.
	0	DS3	**DS3 Mode:** Determines the mapping mode according to the table given below: DS3 Mapping Mode 0 E3 (34.368 Mbit/s) 1 DS3 (44.736 Mbit/s)
C1	7	DECODE	**Transmit Decoder Enabled:** A 1 enables the transmit HDB3/ B3ZS decoder (for rail operation). A 0 disables the decoder (for NRZ operation).
	6	CODE	**Receive Coder Enabled:** A 1 enables the receive HDB3/B3ZS coder (for rail operation). A 0 disables the coder (for NRZ operation).
	5	INVCI	**Invert Transmit Line Clock Input:** When set to 0, the DS3 or E3 line signals are clocked into the L3M device on positive transitions of the clock (TCLK). A 1 enables the line signal to be clocked out of the L3M device on negative transitions of the clock.

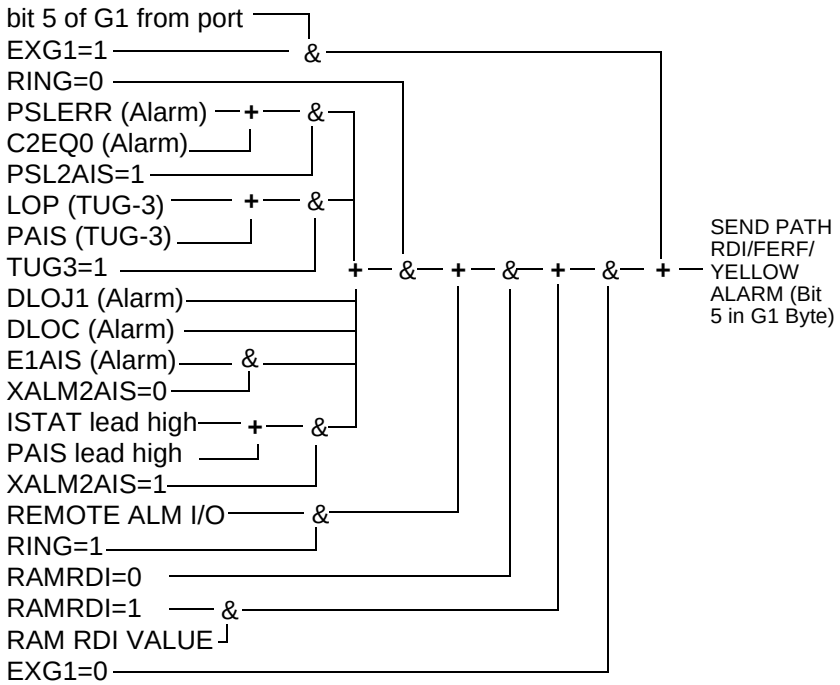
Address	Bit	Symbol	Description
C1 (cont.)	4	INVCO	**Invert Receive Line Clock Output:** When set to 0, the DS3 or E3 line signals are clocked out of the L3M device on negative transitions of the clock (RCLK). A 1 enables the line signal to be clocked out on positive transitions of the clock.
	3	RING	**Ring Operating Mode:** A 1 enables the external alarm interface FEBE count and RDI alarm indication from another L3M device to be transmitted in the G1 byte. The outgoing G1 byte comes from the POH port if the external POH G1 byte is selected. The alarm conditions at the other L3M device that may cause RDI are shown below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 
	2	FLBK	**Facility Loopback:** A 1 enables the transmit line data and clock signals to be looped back as the receive line data and clock signals.  Facility Loopback
	1	L3LBK	**Line E3/DS3 Loopback:** A 1 enables the receive line signal to be looped back as the transmit line signal. The receive data and clock are provided at the receive line interface.  Line Loopback

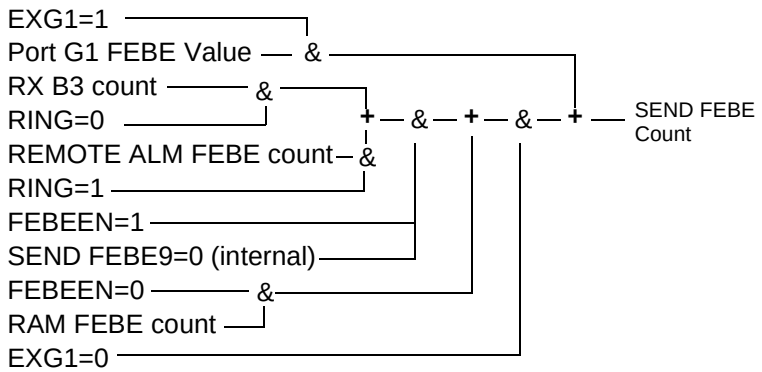
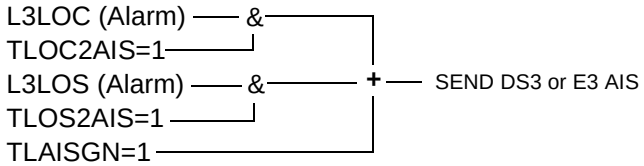
Address	Bit	Symbol	Description
C1 (cont.)	0	SLBK	**SDH/SONET Loopback:** A 1 enables the add SDH/SONET signal to be looped back as the drop signal. The drop signals from the bus are disabled. Add data and clock are provided at the bus interface.  SDH/SONET Loopback
C2	7	ALM2AIS	**External Alarm Enable AIS:** A 1 enables an AIS detected in an E1 byte (when control bit XALM2AIS = 0) or a high on either the ISTAT or PAIS leads (when control bit XALM2AIS = 1) to generate a line AIS in the receive direction when control bit RAISEN is a 1. See logic diagram for Address C5, bit 2.
	6	ALM2FB9	**External Alarm Enable FEBE9:** A 1 enables an AIS detected in an E1 byte (when control bit XALM2AIS = 0) or a high on either the ISTAT or PAIS leads (when control bit XALM2AIS = 1) to generate a count of 9 in bits 1 through 4 of the transmitted G1 byte when control bit FEBE9EN is a 1. See logic diagram for Address C4, bit 6.
	5	TLAISGN	**Transmit Line AIS:** A 1 written into this position generates and transmits a DS3 or E3 AIS towards the SDH/SONET bus, independent of the state of control bit FLBK (bit 2 in register C1H). See Note 1 below.
	4	TPAISGN	**Transmit Zeros or Path AIS Enable:** A 1 enables the L3M device to transmit an SPE with zeros (and valid pointer) or a TUG-3 path AIS towards the SDH/SONET bus, depending on the state of TPAIS00. The logic diagram for sending path AIS is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. UNEQUIP is sent instead if TPAIS00 = 1. 
	3	TPAIS00	**Transmit SPE with Zeros (Unequipped payload):** When enabled by writing a 1 to control bit TPAISGN, a 1 written into this location causes the SPE (POH bytes and payload) to be transmitted with zeros, but with a valid pointer. A 0 causes a TUG-3 AIS to be transmitted towards the SDH/SONET bus.

Note 1: DS3 AIS is defined as a valid M-frame with proper subframe structure. The data payload is a 1010... sequence starting with a 1 after each overhead bit. Overhead bits are as follows: F0=0, F1=1, M0=0, M1=1; C-bits are set to 0; X-bits are set to 1; and P-bits are set for valid parity. E3 AIS is an all ones pattern.

Address	Bit	Symbol	Description
C2 (cont.)	2	INTZ	**Interrupt High Impedance Enable**: A 0 enables the interrupt INT/$\overline{IRQ}$ (lead 129 or B8) to be either high (Intel mode) with the off state low, or to be low (Motorola mode), with the off state high. A 1 enables the off state to be high impedance.
	1	ADDZ	**Add Bus High Impedance Enable:** A 1 sets Add bus data ($\overline{ADATA}$(7-0)) and Add Parity (APAR) leads to a high impedance state, and $\overline{ADD}$ high. If the external timing mode is selected, the clock (ACLK), SPE (ASPE), and C1J1 (AC1J1) signals are also forced to a high impedance state.
	0	L3Z	**Receive Output High Impedance Enable:** A 1 forces the receive interface clock (RCLK) and data signals (RPOS and RNEG), and NRZ outputs (RNRZC and RNRZD) to a high impedance state.
C3	7	EXZ5	**Transmit External Interface Z5 byte:** A 1 enables the Z5 byte from the POH I/O to be transmitted. A 0 enables the corresponding RAM location to be transmitted.
	6	EXZ4	**Transmit External Interface Z4 byte:** A 1 enables the Z4 byte from the POH I/O to be transmitted. A 0 enables the corresponding RAM location to be transmitted.
	5	EXZ3	**Transmit External Interface Z3 byte:** A 1 enables the Z3 byte from the POH I/O to be transmitted. A 0 enables the corresponding RAM location to be transmitted.
	4	EXH4	**Transmit External Interface H4 byte:** A 1 enables the H4 byte from the POH I/O to be transmitted. A 0 enables the corresponding RAM location to be transmitted.
	3	EXF2	**Transmit External Interface F2 byte:** A 1 enables the F2 byte from the POH I/O to be transmitted. A 0 enables the corresponding RAM location to be transmitted.
	2	EXG1	**Transmit External Interface G1 Byte:** A 1 enables bits 1 through 8 in the G1 byte from the POH I/O to be transmitted. A 0 enables the corresponding RAM location or internal logic/alarms to control the transmitted state of FEBE, RDI, and the unassigned bits.
	1	EXC2	**Transmit External Interface C2 Byte:** A 1 enables the C2 byte from the POH I/O to be transmitted. A 0 enables the corresponding RAM location to be transmitted.
	0	EXJ1	**Transmit External Interface J1 Bytes:** A 1 enables the J1 bytes from the POH I/O to be transmitted. A 0 enables the corresponding RAM segment (64 locations) to be transmitted.

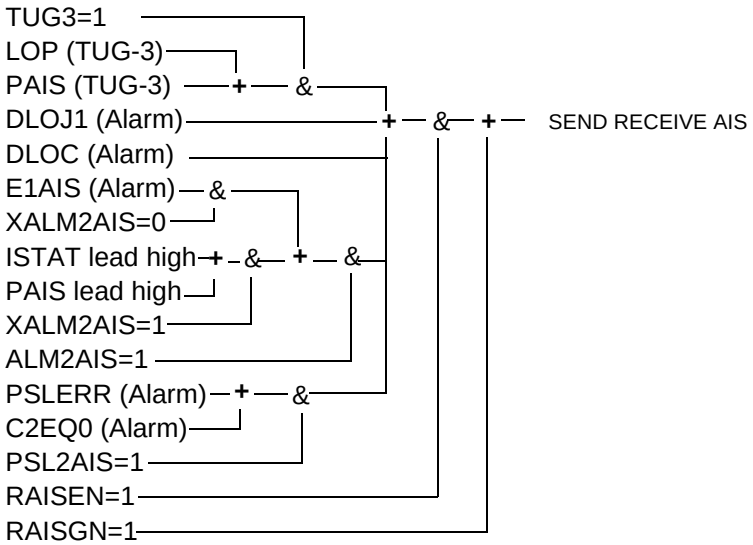
Address	Bit	Symbol	Description
C4	7	EXOO	**External "O"-Bit Select:** A 1 selects the two Overhead Communication Bits ("O"-bits) from the external interface (lead TOCHD) as the two "O"-bits transmitted in each of the nine subframes of the DS3 format or each of the three subframes of the E3 format. A 0 enables the two "O"-bits from the corresponding RAM location to be transmitted (TO2, TO1 at Address 49H).
	6	FEBE9EN	**FEBE9 Enable:** Enable bit for generating a FEBE count of 9 (this is a proprietary non-standard feature and lead FEBE9EN should be disabled for standard compliance by holding it low). When EXG1 is a 0 and FEBE9EN is high, a FEBE count of 9 is generated when: - Either the ISTAT or PAIS input lead is high, and the external alarm enable control bit XALM2AIS is a 1 and ALM2FB9 is 1; - An AIS is detected in the E1 byte, and XALM2AIS is 0 and ALM2FB9 is 1; - Either the TUG-3 PAIS or LOP alarms occur; - The STAI lead is high. The logic diagram for sending FEBE9 is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 

Address	Bit	Symbol	Description
C4 (cont.)	5	RAMRDI	**Remote Defect Indication (Yellow alarm) Enabled:** Enable bit for controlling the generation of Path RDI (bit 5 in G1 byte). When control bits RING and EXG1 are 0, and RAMRDI is a 0, RDI is generated when the following alarms or conditions occur: - Drop bus loss of J1 (DLOJ1) - Drop bus loss of clock (DLOC) - Loss of pointer (LOP) (TUG-3 operation) - Path AIS detected (PAIS) (TUG-3 operation) - Received E1 byte has a majority of 1s and control bit XALM2AIS is 0 - Either the ISTAT or PAIS input lead is high and control bit XALM2AIS is a 1 - PSLERR or C2EQ0 alarm, and control bit PSL2AIS is a 1 When control bit RING is a 1, EXG1 is a 0, and RAMRDI is a 0, the RDI state is controlled via the external alarm indication port. The microprocessor controls the RDI state when RAMRDI is a 1 and EXG1 is a 0. Note: writing a 1 to the RAMRDI bit will disable the local alarms and the alarm indication port RDI in the ring mode from controlling the state of the transmitted RDI bit. The logic diagram for sending Path RDI is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 

Address	Bit	Symbol	Description
C4 (cont.)	4	FEBEEN	**FEBE Enable:** A 1 enables the local B3 count or remote B3 count to be inserted as the FEBE count. A 0 written into this position permits the microprocessor to control the FEBE count. The logic diagram for sending FEBE for all conditions is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 
	3	XALM2AIS	**External Alarm AIS Lead Enable:** A 1 enables the external alarm leads (ISTAT and PAIS) to affect alarm generation instead of AIS in the E1 byte. A 0 causes alarm generation to be based on E1AIS from the drop bus.
	2	TEST	**TranSwitch Test Mode**: A 0 must be written into this location.
	1	TLOC2AIS	**Transmit Loss Of Clock (TLCK) AIS Enable:** A 1 enables the L3M device to send SONET/SDH DS3 AIS or E3 AIS automatically when a transmit line clock failure is detected. The logic diagram for transmitting a line AIS is given below. The + symbol represents an or function, while & represents an and function. Control bit states are given by the = sign. 
	0	TLOS2AIS	**Transmit Loss Of Signal (TPOS/TNEG) AIS Enable:** A 1 enables the L3M device to send DS3 or E3 AIS automatically when a transmit line signal failure is detected.

Address	Bit	Symbol	Description
C5	7	COR	**Clear On Read:** A 0 enables all performance counters to become non-saturating with roll over capability. The contents of the counter are not affected by a read cycle. A 1 causes the performance counters to become saturating counters, which clear on read.
	6	TEST	**TEST:** A 1 must be written into this location.
	5	DROPT	**Drop Bus Timing:** Drop timing can only be selected when the L3M lead XCLKE is low. A 1 selects drop bus timing for the add bus. A 0 selects timing signals from the add bus.
	4	POH2RAM	**Path Overhead Bytes to RAM:** Works in conjunction with the EXbn control bits (e.g., EXF2). The following table summarizes the action taken by this bit and an EXbn bit: POH2RAM / EXbn (e.g., EXF2) / Action 1 / 1 / POH bn interface byte transmitted and written to RAM location. 0 / 1 / POH bn interface byte transmitted, RAM location holds microprocessor-written value. X / 0 / POH bn value written to RAM location by the microprocessor is transmitted.
	3	RAISGN	**Generate Receive Line AIS:** A 1 written into this position generates a DS3/E3 AIS towards the line (RPOS, RNEG) independent of the state of the receive AIS enable bit (RAISEN). See Note below.

Note: DS3 AIS is defined as a valid M-frame with proper subframe structure. The data payload is a 1010... sequence starting with a 1 after each overhead bit. Overhead bits are as follows: F0=0, F1=1, M0=0, M1=1; C-bits are set to 0; X-bits are set to 1; and P-bits are set for valid parity. E3 AIS is an all ones pattern.

Address	Bit	Symbol	Description
C5 (cont.)	2	RAISEN	**Receive AIS Enable:** A 1 enables receive AIS to be generated when the following alarms/conditions occur: - Loss of drop bus clock (DLOC) - Loss of drop bus J1 (DLOJ1) - E1 AIS (E1AIS) and XALM2AIS are 0, and ALM2AIS is a 1 - ISTAT or PAIS (lead) and XALM2AIS are 1, and ALM2AIS is a 1 - Loss of pointer (LOP) (TUG-3) - Path AIS (PAIS) (TUG-3) - PSLERR or C2EQ0 occurs, and Path Signal Label Error Enable AIS control bit (PSL2AIS) is a 1 The logic diagram for generating receive line AIS is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>C5
(cont.)</td><td>1</td><td>WGDEC</td><td>Test Equipment BPV Selection: A 1 enables the decoder to detect coding violations as found in ‘Type 1’ test equipment. A 0 enables the decoder to detect coding violations as found in ‘Type 0’ test equipment. The following tables summarize the two decoding procedures of coding violations:
BPV For B3ZS
<table>
<tr><th>BPV</th><th>"Type 1”
Equipment</th><th>“Type 0”
Equipment</th></tr>
<tr><td>++ or --</td><td>000 (preceding bit(s) changed)</td><td>11</td></tr>
<tr><td>0BV or 000V</td><td>0000</td><td>011 or 0001</td></tr>
<tr><td>BB0V after odd</td><td>1000</td><td>1101</td></tr>
<tr><td>B00V after even</td><td>1000</td><td>1001</td></tr>
</table>
BPV For HDB3
<table>
<tr><th>BPV</th><th>"Type 1”
Equipment</th><th>“Type 0”
Equipment</th></tr>
<tr><td>++ or --</td><td>0000 (preceding bit(s) changed)</td><td>11</td></tr>
<tr><td>0BV or 0000V</td><td>00000</td><td>011 or 00001</td></tr>
<tr><td>BB00V after odd</td><td>10000</td><td>11001</td></tr>
<tr><td>B000V after even</td><td>10000</td><td>10001</td></tr>
</table></td></tr>
<tr><td></td><td>0</td><td>PSL2AIS</td><td>Path Signal Label Error Enable AIS: A 1 enables the L3M device to send DS3 or E3 AIS automatically towards the receive line, and path RDI (FERF) when a PSLERR or C2EQ0 alarm occurs. (See RAMRDI and RAISEN for diagrams.)</td></tr>
<tr><td>C6</td><td>7</td><td>FASTPTR</td><td>Fast Pointer Enabled: A 1 allows the L3M device to track pointer movements every frame instead of every other frame for TUG-3 operation.</td></tr>
<tr><td></td><td>6</td><td>TOHOUT</td><td>Transport Overhead Bytes Out: A 1 enables the L3M device to generate the A1, A2, C1, and the H1, H2 bytes, in the external timing mode (STS-1 mode) only. The H1 and H2 bytes are transmitted with a fixed pointer value of 6000H.</td></tr>
<tr><td></td><td>5</td><td>H4CTR</td><td>H4 Counter Enable: Normally set to 0. A 1 enables the H4 byte to be transmitted with a count generated by an internal 8-bit frame counter.</td></tr>
<tr><td></td><td>4</td><td>PAT23</td><td>2^{23}-1 Test Pattern Enable: A 0 selects the test pattern generators’ and analyzer’s pattern to be 2^{15}-1. A 1 selects the pattern generators’ and analyzer’s pattern to be 2^{23}-1.</td></tr>
<tr><td></td><td>3</td><td>ENANA</td><td>Enable Analyzer: A 1 enables the 2^{15}-1or 2^{23}-1 analyzer. PRBS errors are counted in a 16-bit counter in locations AEH and AFH.</td></tr>
<tr><td></td><td>2</td><td>TXANA</td><td>Transmit Analyzer Enable: A 1 enables the analyzer to sample the transmit NRZ line (DS3/E3) signal after the Decoder. A 0 causes the analyzer to sample the receive NRZ line data prior to the coder function. A 1 must be written into ENANA for this bit to function (see Figure 34).</td></tr>
<tr><td></td><td>1</td><td>TPRBS</td><td>Transmit Test Pattern Generator Enable: A 1 enables the transmit test pattern generator and disables the NRZ decoder output.</td></tr>
<tr><td></td><td>0</td><td>RPRBS</td><td>Receive Test Pattern Generator Enable: A 1 enables the receive test pattern generator and disables the NRZ coder input.</td></tr>
</table>

Address	Bit	Symbol	Description
C7	7	TESTB3	**Test B3 Byte:** A 1 transmits a B3 value written by the microprocessor in location 40H. A 0 enables the test byte to become a test mask. When configured as a test mask, a 1 in one or more bit positions causes those bits in the transmitted B3 byte to be inverted.
	6	FIXPTR	**TUG-3 Fixed Pointer Generation:** A 1 forces a fixed pointer of 0 to be generated in the transmitted TUG-3 regardless of any pointer movements (J1 in DC1J1) that may occur on the Drop side when the Drop timing mode is selected, or if a pointer movement (J1 in AC1J1) takes place when Add bus timing is selected. When this bit is written with a 0, a pointer movement on the Add or Drop bus is compensated with an outgoing TUG-3 pointer movement in the opposite direction.
	5	TEST	**Test Bit Position:** This bit must be set to 1.
	4	DIV4	**Phase Detector Gain:** This control bit governs the gain of the phase detector, and it should be set as indicated in the Operation section entitled “PLL Filter Connection to VCXO”.
	3	INVCTRL	**Invert Control:** Inverts the CTRL output lead (lead 3 or D3). When set to 0, the external loop filter must be non-inverting, which requires the use of an inverter in the loop (U1 in Figure 32). When set to 1, an external inverting loop filter is necessary, and U1 is not required.
	2	TXRST	**Transmit Reset:** A 1 written into this position resets the transmit section (Line to SDH/SONET) of the L3M device. This includes the transmit FIFOs and internal counters. The L3M device’s transmitter will remain reset until the microprocessor writes a 0 into this location.
	1	RXRST	**Receive Reset:** A 1 written into this position resets the receive section (SDH/SONET to Line) of the L3M device. This includes the receive FIFOs and internal counters. The L3M device’s receiver will remain reset until the microprocessor writes a 0 into this location.
	0	RESETC	**Reset Performance Counters:** A 1 written into this position resets all performance counters to 0. This bit is self clearing, and does not require the microprocessor to write a 0 into this location.
C8	7-0	C2 Compare	**Path Signal Label Compare:** The bits in this location are written by the microprocessor, and are compared against the C2 byte received (register 91H) for a signal label mismatch condition.
C9	7-2	TEST	**Test Bit Positions:** Zeros must be written into these bits.
	1	RDI5	**RDI 5 Consecutive Enable:** A 1 enables the detection/recovery of RDI (bit 5 in the G1 byte) to 5 consecutive matches/mismatches. A 0 enables the detection/recovery of RDI to 10 consecutive matches/mismatches.
	0	FEBEBLK	**FEBE Counter Block Count Enable:** A 1 configures the FEBE counter (register locations AA and AB) to count one or more FEBE errors per received G1 byte as one error (block). A 0 configures the FEBE counter to count the number of errors detected (1 to 8).

Address	Bit	Symbol	Description
CA	7-6	TEST	**Test Bit Positions:** These bits must be set 0.
	5	NOPOH	**No Path Overhead:** When this bit is set to 1, the VC-4 path overhead time slots of the Add bus data signals ADATA(7-0) are set to a high impedance and the $\overline{\text{ADD}}$ signal is high during these time slots. When this bit is set to 0, ADATA(7-0) and $\overline{\text{ADD}}$ are active during these time slots. The ADATA (7-0) byte values are set to 00H during these time slots.
	4-0	TEST	**Test Bit Positions:** These bits must be set 0.

STATUS BITS

Status bits report the condition of alarms. Unlatched bit positions (even addresses) respond to transient alarm conditions. Latched bit positions (odd addresses) are set upon occurrence of an alarm condition and then stay high until they are cleared by a read cycle. It is important to remember that, when reading the latched registers in the L3M, the contents should be read a second time before determining the current status.

Address	Bit	Symbol	Description
B0 & B1	7	DLOC	**Drop Bus Loss Of Clock Alarm:** A loss of clock alarm occurs when the input Drop clock is stuck high or low for 1000 ± 500 nanoseconds. Recovery occurs on the first clock transition.
	6	DLOJ1	**Drop Bus Loss of J1:** A loss of J1 alarm occurs when: - 8 consecutive new J1 positions have been detected or - J1 is stuck low for 8 consecutive frames or - J1 is stuck high for 8 consecutive bytes or - 8 J1 pulses are received in one frame. Recovery occurs when the J1 pulse is detected in the same location for 8 consecutive frames.
	5	BUSERR	**Bus Parity Error:** A 1 indicates a parity error has been detected on the drop bus. Odd parity is calculated over the DDATA, DSPE, DC1J1 or DC1, and DPAR leads. Other than providing this alarm, no other action is taken.
	4	E1AIS	**E1 Byte AIS Detected:** A 1 indicates that AIS has been detected in the E1 byte corresponding to AU-3/STS-3 STS-1. For TUG-3 operation, the E1 in slot 0 is monitored. Majority logic (5 out of 8 1s) is used for detection. The following alarms in the TranSwitch SOT-3/SOT-1 devices generate an E1 byte having an AIS indication: loss of frame, loss of signal, loss of pointer, and line AIS detected. Internal pointer processing is performed for the TUG-3 signal according to ETSI draft document pr ETS 300 417-1, July 1994.
	3	LOP	**Loss Of Pointer Alarm:** Valid for TUG-3 pointer processing only. A loss of pointer alarm occurs when a New Data Flag (NDF) or an invalid pointer is detected for eight consecutive frames. Recovery occurs when a valid pointer is received for three consecutive frames.
	2	PAIS	**Path AIS Alarm:** Valid for TUG-3 pointer processing only. A Path Alarm Indication Signal (AIS) is detected when all ones are detected in the 16 bit pointer word (H1 and H2) for three consecutive frames. Recovery occurs when a valid NDF is received, or a valid pointer is detected, for three consecutive frames.
	1	PSLERR	**Path Signal Label Error:** A 1 indicates that the comparison between the received C2 byte and the microprocessor-written C2 byte or certain fixed values did not match 5 times consecutively (i.e., the two mismatch test conditions are C2 ≠ value in register C8H and-gated with C2 ≠ 01H, or C2 = 00H). Recovery to 0 occurs when the comparison matches five times consecutively.
	0	C2EQ0	**Unequipped Alarm:** An unequipped alarm is detected (C2EQ0 = 1) when the C2 byte is equal to 00H 5 times consecutively. Alarm recovery to C2EQ0 = 0 occurs when the C2 byte is not equal to 00H five times consecutively.

Address	Bit	Symbol	Description
B2 & B3	7	RDI	**Receive RDI (Yellow) Alarm:** When RDI5 is set to 0, a 1 in RDI indicates that bit 5 in the G1 byte has been detected as a one for 10 consecutive frames. When RDI5 is set to 0, RDI recovers to 0 when a 0 has been detected for 10 consecutive frames. When RDI5 is a 1, detection and recovery of RDI occurs after 5 consecutive events instead of 10.
	6	L3LOS	**Mapper Transmit Loss Of Signal:** For an E3 signal, a loss of signal alarm occurs when the positive/negative rail is stuck low for 256 bit times. Recovery occurs when there are at least 32 transitions (both positive and negative rail) in a count of 256 clock cycles. For a DS3 signal, a loss of signal alarm occurs when either the positive or negative rail is stuck low for 200 bit times. Recovery occurs on the first transition (both positive and negative rail). When the interface is configured for NRZ operation, an active high on the TNEG will be an external loss of signal indication and will cause a L3LOS indication.
	5	L3LOC	**Mapper Transmit Loss of Clock:** A 1 indicates the incoming line clock (TCLK) signal has been stuck high or low for 1000 ± 500 nanoseconds. Recovery occurs on the first clock transition.
	4	TOVFL	**Transmit FIFO Overflow/Underflow:** A 1 indicates that the transmit FIFO has either underflowed or overflowed. When this happens, the FIFO automatically resets to a preset position.
	3	L3AIS	**Mapper E3 Transmit AIS Detected:** For an E3 signal, AIS is detected when four or fewer zeros are detected in 1536 bits, twice in a row. Recovery occurs when there are five or more zeros detected in 1536 bits two consecutive times.
	2	RAMLOC	**Loss Of Microprocessor RAM Clock:** A 1 indicates that the RAM clock (RAMCI) has been stuck high or low for 1000 ± 500 nanoseconds. Recovery occurs on the first clock transition.
	1	ALOC	**Add Bus Loss Of Clock:** A loss of clock alarm occurs when the input add clock (ACLK) is stuck high or low for 1000 ± 500 nanoseconds. Recovery occurs on the first clock transition. When the add bus clock is an output, the external byte clock (XCLKI) is monitored for loss of clock instead, and its loss is reported by this alarm.
	0	ALOJ1	**Add Bus Loss of J1:** A loss of J1 alarm occurs when: - 8 consecutive new J1 positions have been detected or - J1 is stuck low for 8 consecutive frames or - J1 is stuck high for 8 consecutive bytes or - 8 J1 pulses are received in one frame. Recovery occurs when the J1 pulse is detected in the same location for 8 consecutive frames.

Address	Bit	Symbol	Description
B4 & B5	7	SINT (B4 only)	**Software Interrupt:** A software interrupt indication occurs when one or more bit locations in the interrupt mask locations is set to 1, and the corresponding latched alarm is active. The SINT state is exited when the latched alarm causing the interrupt clears or its corresponding bit in the interrupt mask is cleared.
	6	FEBE9	**FEBE Count of 9 Indication:** An STS FEBE9 indication occurs when the code 1001 (count of 9) in bits 1-4 in the received G1 byte is detected for five consecutive frames. The alarm is terminated when any code other than the 1001 is detected in bits 1-4 for five consecutive frames.
	5	NEW	**New Alarm:** An indication that a new J1 location, other than those resulting from INC or DEC, has been detected.
	4	TUG3NEW	**TUG-3 New Alarm:** A TUG-3 new indication occurs when three consecutive new pointers, or an NDF and a match of the SS bits and the pointer offset value is in range, has been detected.
	3	ROVFL	**Receive FIFO Overflow/Underflow:** A 1 indicates an underflow or overflow condition in the receive direction (SDH/SONET to line). When this happens, the FIFO will automatically reset to a preset position and the FIFOERR output (lead 11 or F3) will pulse high.
	2	XSTAI	**SDH/SONET Network Alarm Indication:** A 1 indicates that the input on the lead labeled STAI is high.
	1	XISTAT	**External STS-1 Alarm:** A 1 indicates that the input on the lead labeled ISTAT is a high. A 1 is equal to an external alarm condition (e.g., LOP).
	0	XPAIS	**External Path AIS:** A 1 indicates that the input on the lead labeled PAIS is a high. A 1 is equal to an external alarm condition (i.e., Path AIS).

Address	Bit	Symbol	Description
B6 & B7	7	L3ERR	**Analyzer Error Indication:** A 1 indicates that the 2^{15}-1 or 2^{23}-1 analyzer has detected an error when enabled. A 1 written to ENANA (bit 3, location C6) enables the analyzer. This indication will be disabled during operation when control bit ENANA is a 0.
	6	LOVFL	**Leak FIFO Overflow/Underflow Alarm:** A 1 indicates that the leak FIFO has underflowed or overflowed. When this occurs, the FIFO will automatically reset to a preset position and the FIFOERR output (lead 11 or F3) will pulse high.
	5	RFRST	**Receive FIFO Reset Indication:** A 1 indicates that either of the receive FIFOs has been reset. This may occur because of a FIFO overflow/underflow alarm, or when the receive section has been reset by writing a 1 to control bit RXRST, or upon hardware reset.
	4	TFRST	**Transmit FIFO Reset Indication:** A 1 indicates that the transmit FIFO has been reset. This may occur because of a FIFO overflow/underflow alarm, or when the transmit section has been reset by writing a 1 to control bit TXRST, or upon hardware reset.
	3	VCXOLOC	**Loss of VCXO Clock:** A 1 indicates that the external VCXO clock has been stuck high or low for 1000 $\pm$ 500 nanoseconds. Recovery occurs on the first clock transition.
	2	TPLOC	**Loss of Transmit PLL Clock:** A 1 indicates that the internal PLL clock has been stuck high or low for 1000 $\pm$ 500 nanoseconds. Recovery occurs on the first clock transition.
	1	RPLOC	**Loss of Receive PLL Clock:** A 1 indicates that the internal PLL clock has been stuck high or low for 1000 $\pm$ 500 nanoseconds. Recovery occurs on the first clock transition.
	0	OOL	**Analyzer Out of Lock:** A 1 indicates that the analyzer, when enabled, is out of lock.

Interrupt Mask Bits

A 1 written to any of the bits in the interrupt mask (except HINT), and the occurrence of the corresponding alarm, causes a software interrupt (SINT) to occur. If the hardware interrupt bit (HINT) is also written with a 1, then a hardware interrupt also occurs.

Address	Bit	Symbol	Description
BA	7	DLOC	Drop Bus Loss Of Clock
	6	DLOJ1	Drop Bus Loss of J1
	5	BUSERR	Bus Parity Error
	4	E1AIS	E1 Byte AIS detected
	3	LOP	Loss Of Pointer (TUG-3 operation)
	2	PAIS	Path AIS (TUG-3 operation)
	1	PSLERR	Path Signal Label Error
	0	C2EQ0	C2 Equal to 0 alarm (unequipped)
BB	7	RDI	Receive RDI (yellow) detected.
	6	L3LOS	Transmit Line Loss Of Signal
	5	L3LOC	Transmit Line Loss Of Clock
	4	TOVFL	Transmit FIFO Error (underflowed or overflowed)
	3	L3AIS	E3 Transmit Line AIS Detected
	2	RAMLOC	Loss Of Microprocessor RAM Clock (RAMCI signal, lead 130 or C7)
	1	ALOC	Add Bus Loss Of Clock
	0	ALOJ1	Add Bus Loss of J1
BC	7	HINT	Hardware Interrupt Enable
	6	FEBE9	FEBE Count of 9 indication
	5	NEW	New Alarm - NDF and 3x new pointer events (TUG-3 operation)
	4	TUG3NEW	TUG-3 New Alarm - Three new pointer events
	3	ROVFL	Receive FIFO Overflow/Underflow
	2	XSTAI	SDH/SONET Network Alarm Indication
	1	XISTAT	External STS-1 Alarm (ISTAT) signal detected as a 1 (if enabled)
	0	XPAIS	External Path AIS (PAIS) signal detected as a 1 (if enabled)
BD	7	L3ERR	Internal Analyzer bit error detected.
	6	LOVFL	Leak FIFO Overflow/Underflow
	5	RFRST	Receive FIFO Reset Indication
	4	TFRST	Transmit FIFO Reset Indication
	3	VCXOLOC	VCXO Loss Of Clock
	2	TPLOC	Transmit PLL loss of clock
	1	RPLOC	Receive PLL loss of clock
	0	OOL	Analyzer out of lock.

Transmit Path Overhead Bytes And "O"-bits

The Transmit Path Overhead bytes consist of the J1, B3, C2, G1, F2, H4, Z3 (F3), Z4 (K3), and Z5 (N1) bytes, where Z3, Z4 and Z5 are ANSI designations. The POH bytes may be individually transmitted from the POH interface, or from RAM locations written by the microprocessor. When POH2RAM is a 1, the POH interface byte selected for transmission is written into the common RAM location as transmitted. For example, if EXC2 is set to 1, the transmit POH interface C2 byte is written into the assigned RAM location, in addition to being transmitted. If EXC2 is set to 0, the transmitted byte is the value written into the corresponding RAM location by the microprocessor. When a 0 is written into the POH2RAM control bit, the L3M device disables the capability of writing any of the selected POH interface bytes into their RAM locations. However, individual bytes may still be transmitted from either the POH interface or the microprocessor-written RAM location. This feature permits switching back and forth between a selected POH interface byte or a RAM location for transmission, without having to re-initialize the RAM location. The following table is a summary of this operation:

POH2RAM	EXbn*	Action
1	1	POH interface byte bn written into RAM, and also transmitted.
0	1	POH interface byte bn transmitted, but not written into RAM. Microprocessor writes RAM value as required.
X	0	POH RAM value of bn byte transmitted.

* e.g., bn = C2.

The relationship between a transmitted Path Overhead byte and the corresponding RAM location is as follows:

Bits of RAM Location

7	6	5	4	3	2	1	0

Bits of Transmitted POH Byte

1	2	3	4	5	6	7	8

The “O”-bits consists of two overhead communication bits per subframe, for nine subframes, in the DS3 format, or for 3 subframes in the E3 format. The selection of the two bits per subframe, either from the “O”-bit interface or from RAM, operates in the same way as the Path Overhead bytes, but “O”-bits from the transmit “O”-bit port are not written into RAM. When sourced from the RAM, the same “O”-bit pair will be sent throughout the entire SONET frame (i.e., the “O”-bit value from RAM is accessed only once per frame).

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>00
to
3F</td><td>7-0</td><td>J1</td><td>Path Trace: The bytes written into this location provide a repetitive 64 byte fixed length message for transmission. The bytes written into these positions are either from the microprocessor or from the external POH I/O.</td></tr>
<tr><td>40</td><td>7-0</td><td>B3
Error
Mask</td><td>B3 Error Mask: When control bit TESTB3 is a 0, the bit columns written with a one represent the columns in the B3 byte in which errors are generated. The B3 errors are sent until this position is rewritten with a 00H. When control bit TESTB3 is a 1, the value written into this location is the transmitted B3 byte.</td></tr>
<tr><td>41</td><td>7-0</td><td>C2</td><td>Path Signal Label (microprocessor): The bits written into this position indicate the construction of the AU-3, TUG-3, or SPE.</td></tr>
<tr><td>42</td><td>7-0</td><td>G1</td><td>Transmit Byte G1: This byte is used for sending the microprocessor-controlled states for FEBE, RDI, and the unassigned bits, according to states given in the tables below:

<table>
<tr><td>Transmit G1 Bit</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td></tr>
<tr><td>RAM Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td></td><td colspan="4">TFEBE</td><td>TRDI</td><td colspan="3">Unassigned</td></tr>
</table>

TFEBE
<table>
<tr><th>EXG1</th><th>FEBEEN</th><th>Action</th></tr>
<tr><td>0</td><td>0</td><td>Microprocessor-written value sent</td></tr>
<tr><td>0</td><td>1</td><td>Internal or mate (ring mode) value sent</td></tr>
<tr><td>1</td><td>X</td><td>External POH value sent</td></tr>
</table>

TRDI
<table>
<tr><th>EXG1</th><th>RAMRDI</th><th>Action</th></tr>
<tr><td>0</td><td>0</td><td>Internal or mate (ring mode) value sent</td></tr>
<tr><td>0</td><td>1</td><td>Microprocessor-written value sent</td></tr>
<tr><td>1</td><td>X</td><td>External POH value sent</td></tr>
</table>

Unassigned Bits
<table>
<tr><th>EXG1</th><th>Action</th></tr>
<tr><td>0</td><td>Microprocessor-written value sent</td></tr>
<tr><td>1</td><td>External POH value sent</td></tr>
</table>
</td></tr>
</table>

Address	Bit	Symbol	Description
43	7-0	F2	**User Channel:** This location provides microprocessor- or I/O- written information between elements.
44	7-0	H4	**H4 Channel:** This byte is not used in this mapping, and should be set to 00H by the microprocessor or I/O. Writing a one to the H4CTR bit inserts an 8-bit counter into this byte.
45 46 47	7-0 7-0 7-0	Z3 (F3) Z4 (K3) Z5 (N1)	**Z3 (F3), Z4 (K3), Z5 (N1) Bytes:** The processing of these bytes is not supported in the L3M. However, the microprocessor may write the transmit values of these bytes in these registers.
48	7-0		Not used.
49	7-2		Not used.
	1 0	TO2 TO1	**Transmit "O"-Bits:** These two bits correspond to the two "O"-bits found in each of the nine subframes in the DS3 format or the three subframes in the E3 format. The "O"-bits are read once per frame and inserted into each of the subframes.

Receive Path Overhead Bytes, Tug-3 H1/h2 Bytes And "O"-bits

The received bytes are written into the locations given below, and are also provided at the receive Path Overhead byte interface.

The relationship between a received Path Overhead byte and the corresponding RAM location is as follows:

Bits of RAM Location:

7	6	5	4	3	2	1	0

Bits of Received POH Byte:

1	2	3	4	5	6	7	8

Address	Bit	Symbol	Description
50 to 8F	7-0	J1	**Path Trace:** The received J1 bytes are written in the 64 byte segment in a rotating fashion. There is no specific starting point.
90	7-0	B3	**Path B3:** The value in this location is the received B3 parity byte.
91	7-0	C2	**Path Signal Label:** These bits indicate the construction of the AU-3, TUG-3, or SPE (e.g., unequipped).
92	7-0	G1	**Receive Byte G1:** This location provides the receive status of the FEBE bits, Path RDI, and unassigned bits in the G1 byte. Receive G1 Bit 1 2 3 4 5 6 7 8 RAM Bit 7 6 5 4 3 2 1 0 RFEBE RRDI Unassigned
93	7-0	F2	**User Channel:** This location provides user information between elements.
94	7-0	H4	**H4 Byte:** This byte is not specified for use in this application. It is provided for future use as required.
95 96 97	7-0 7-0 7-0	Z3 (F3) Z4 (K3) Z5 (N1)	**Path Growth:** The Z3, Z4 and Z5 bytes are designated for future growth. The Z5 byte has been assigned for Tandem Connection application.
98 99	7-0	H1 H2	**Received H1 and H2 Pointer:** The contents of the H1 and H2 pointer for a TUG-3 are provided in the following bit order for a microprocessor read cycle. H1 H2 Bit 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 N N N N S S I D I D I D I D I D I D
9A	1 0	RO2 RO1	**Receive "O"-Bits:** The received states of the two Overhead Communication channel bits found in the nine subframes in the DS3 format or the three subframes in the E3 format. The two bits are updated once a frame from one of the subframes in the frame.

Performance Counters And Fifo Leak Rate

All 16-bit performance counters allow uninterrupted access, without the danger of one byte changing while the other byte is read. To perform a 16-bit read, the low order byte is read first. This causes the high order byte of the counter to be transferred to a common high order byte at location FFH. The common high order byte should be read next to complete the count transfer; if another performance counter low order byte is read first, the contents of the common high order byte will change to reflect the performance counter just read. Counts that occur during the read cycle are held for the counter to be updated afterwards.

All the performance counters can also be configured to be either saturating or non-saturating. When a 1 is written to control bit COR (clear on read), the performance counters are configured to be saturating, with the counters stopping at their maximum count. An 8-bit or 16-bit counter is reset on a microprocessor read cycle. When a 0 is written to control bit COR, the performance counters are configured to be non-saturating, and roll over to zero after the maximum count in the counter is reached. The counters are then not cleared on a read cycle.

All the performance counters can be reset simultaneously by writing a 1 to control bit RESETC. This bit is self clearing, and does not require writing a 0 into this location.

All drop bus related performance counters are inhibited (i.e., will not increment) when one or more of the following alarms occurs:

- Loss of Drop bus clock (DLOC)
- Loss of Drop bus J1 (DLOJ1)
- AIS detected in the E1 byte (when XALM2AIS = 0)
- When either ISTAT or PAIS lead is high (when XALM2AIS = 1)
- Loss of pointer (TUG-3)
- Path AIS (TUG-3)

The performance counters can also be written by the microprocessor. However, when writing to a 16-bit counter (at locations n, n+1) it is recommended that the low order byte at location n should be written first. The high order byte can be written by addressing location n + 1. Since the writes occur in separate cycles, care must be taken to prevent the low byte from carrying-out to the high byte before the high byte is initialized. Writing a low byte equal to 00H will provide the maximum time for the microprocessor to update the high byte.

Address	Bit	Symbol	Description
A0	7-0	Rcv Frame Cnt	**Receive SDH/SONET Frame Count:** Counts the number of received SDH/SONET frames.
A1	7-0		Not used.
A2	7-0	FIFO Leak Rate	**FIFO Leak Rate Register:** The number written into this location represents the number of frames between consecutive leaked bits, in multiples of four frames (i.e., a value of x means that there are 4x frames between bit leaks). The recommended value of zero causes a bit to be leaked every other frame.
A3	7-0	INC Count	**Positive Justification Counter:** Counts the number of positive (increment) pointer movements in the AUG/VC-4 or STS-3/STS-1 based on J1 movements.

Address	Bit	Symbol	Description
A4	7-0	DEC Count	**Negative Justification Counter:** Counts the number of negative (decrement) pointer movements in the AUG/VC-4 or STS-3/STS-1 based on J1 movements.
A5	7-0	New Count	**New Data Flag (NDF) Counter:** Counts the number of J1 movements for the AUG/VC-4 or STS-3/STS-1.
A6	7-0	TUG-3 INC Count	**TUG-3 Positive Justification Counter:** Counts the number of positive (increment) pointer movements in the TUG-3, based on interpretation of H1 and H2.
A7	7-0	TUG-3 DEC Count	**TUG-3 Negative Justification Counter:** Counts the number of negative (decrement) pointer movements in the TUG-3, based on interpretation of H1 and H2.
A8	7-0	TUG-3 NDF Count	**TUG-3 New Data Flag (NDF) Counter:** Counts the number of New Data Flags (NDFs) or new pointers in the TUG-3 pointer (H1/H2). Note: The TUG-3 NDF counter will not register a count when the pointer is changed between certain sets of values (i.e., 192 to 194 or 193 to 195). The TUG-3 NDF counter will register two counts for the inverse case, (i.e., 194 to 192 or 195 to 193).
A9	7-0	B3 Block Count	**B3 Blocks (in error) Counter:** Counts the number of B3 blocks which are received in error.
AA	7-0	FEBE Count	**Far End Block Error Counter:** Counts the FEBE error count indication received in bits 1 through 4 of G1 when control bit FEBEBLK is a 0. When FEBEBLK is a 1, one or more errors per received G1 byte are counted as 1 error (block). Location AAH is the low order byte, while location ABH is the high order byte of the 16-bit counter. After reading the low order byte from AAH the corresponding high order byte (ABH) should be read from FFH.
AC	7-0	B3 Counter	**B3 Error Counter:** Counts the number of B3 errors that occur between the incoming value and calculated value. Location ACH is the low order byte, while location ADH is the high order byte of the 16-bit counter. After reading the low order byte from ACH the corresponding high order byte (ADH) should be read from FFH.
AE	7-0	Coding Errors	**HDB3/B3ZS Coding Error Counter:** Counts the number of internal coding violation errors detected when in P/N rail mode. Location AEH is the low order byte while location AFH is the high order byte of the 16-bit counter. When control bit ENANA is set to 1, PRBS errors are counted when the internal analyzer is in lock (no OOL alarm). After reading the low order byte from AEH the corresponding high order byte (AFH) should be read from FFH.
FF	7-0	Common High Byte Count	**Common High Order Byte:** This location contains a copy of the high order byte that was associated with the low order byte of the 16-bit counter most recently read.

PACKAGE INFORMATION

The L3M device is available in two package formats. One is a 144-lead plastic quad flat package suitable for surface mounting, as shown in Figure 37. The other is a 208-lead small outline plastic ball grid array package suitable for surface mounting, as illustrated in Figure 38.

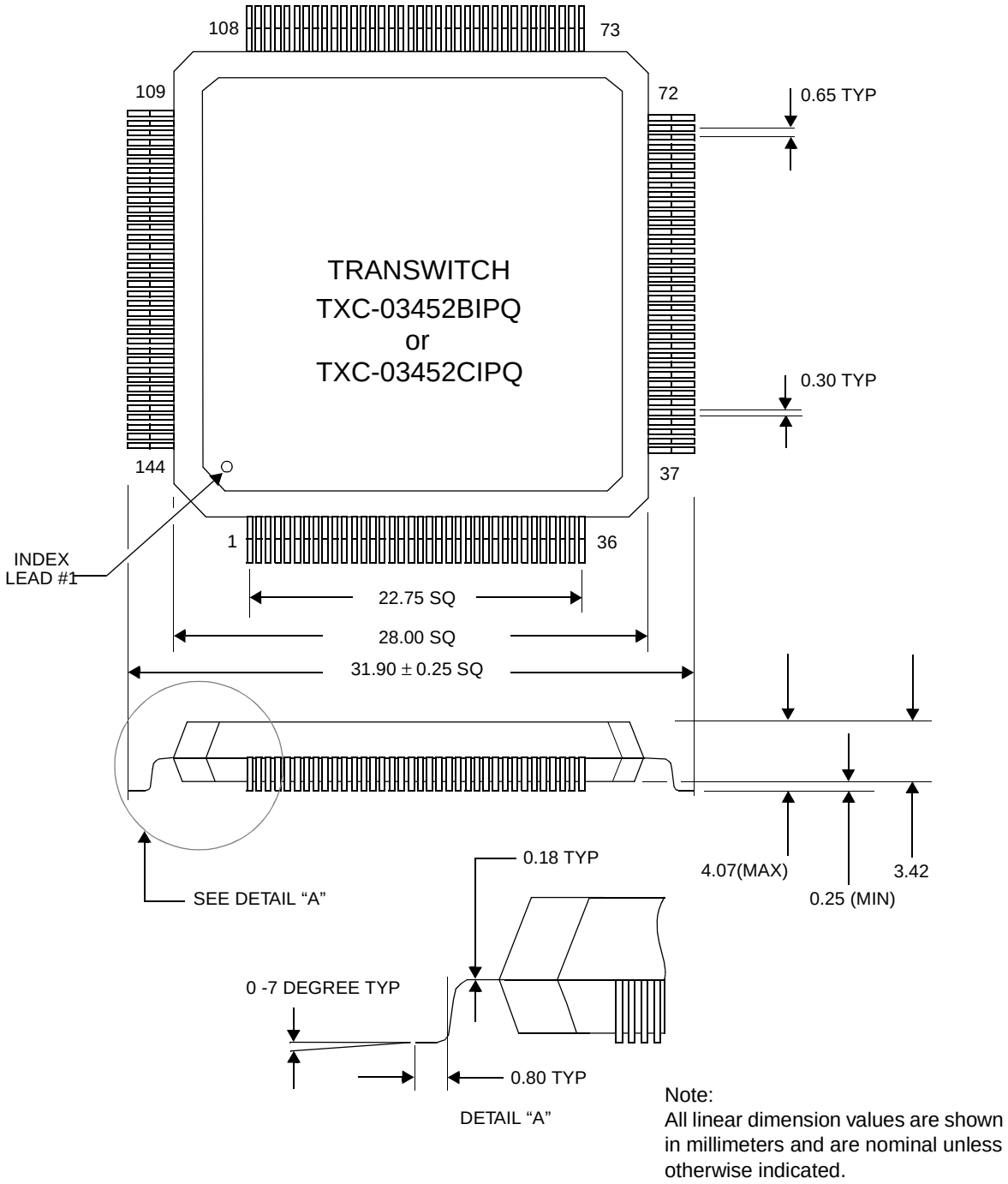
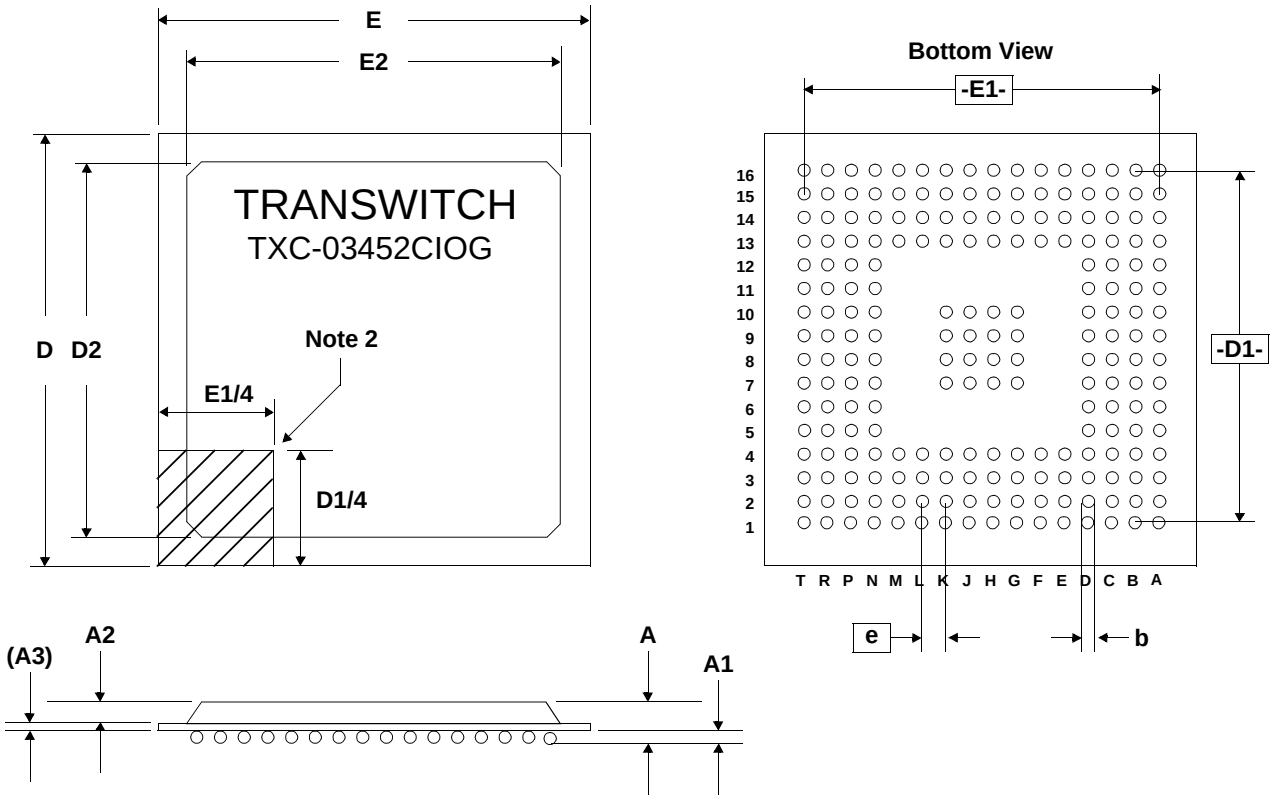


Figure 37. L3M TXC-03452B 144-Lead Plastic Quad Flat Package



Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 16 x 16, JEDEC code MO-151-AAF-1

Dimension (Note 1)	Min	Max
A	1.35	1.75
A1	0.30	0.50
A2	0.75	0.85
A3 (Ref.)	0.36	
b	0.40	0.60
D	17.00	
D1 (BSC)	15.00	
D2	15.00	15.70
E	17.00	
E1 (BSC)	15.00	
E2	15.00	15.70
e (BSC)	1.00	

Figure 38. L3M TXC-03452B 208-Lead Small Outline Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number:	TXC-03452BIPQ (not recommended for new designs)	144-Lead Plastic Quad Flat Package
	TXC-03452CIPQ	144-Lead Plastic Quad Flat Package
	TXC-03452CIOG	208-Lead Small Outline Plastic Ball Grid Array Package

RELATED PRODUCTS

TXC-02030, DART VLSI Device (Advanced E3/DS3 Receiver/Transmitter). DART performs the transmit and receive line interface functions required for transmission of E3 (34.368 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). Transmits and receives at STS-3/STM-1 rates. Provides the complete STS-3/STM-1 frame synchronization function. Connects directly to optical fiber interface components.

TXC-03001/TXC-03001B, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). This device performs section, line and path overhead processing for STS-1 SONET signals. Has programmable STS-1 or STS-N modes.

TXC-03003/TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals. Compliant with ANSI and ITU-TSS standards.

TXC-03303, M13E VLSI Device. Extended feature version of the TXC-03301 (M13).

TXC-03305, M13X VLSI Device (DS3/DS1 Mux/Demux). This single-chip device provides the functions needed to multiplex and demultiplex 28 independent DS1 signals to and from a DS3 signal with either an M13 or C-bit frame format. It includes some enhanced features relative to the M13E device.

TXC-06103, PHAST-3N VLSI Device (SONET/SDH STM-1, STS-3 or STS-3c Overhead Terminator) This PHAST-3N VLSI device provides a COMBUS interface for downstream devices and operates from a power supply of 3.3 volts.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
11 West 42nd Street
New York, New York 10036

Tel: (212) 642-4900
Fax: (212) 302-1286
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

2570 West El Camino Real
Suite 304
Mountain View, CA 94040

Tel: (650) 949-6700
Fax: (650) 949-6705
Web: www.atmforum.com

ATM Forum Europe Office

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Belgium

Tel: 2 761 66 77
Fax: 2 761 66 79

ATM Forum Asia-Pacific Office

Hamamatsu-cho Suzuki Building 3F
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
7730 Carondelet Avenue, Suite 407
Clayton, MO 63105-3329

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LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated L3M TXC-03452B Data Sheet that have significant differences relative to the previous and now superseded Data Sheet:

Updated L3M TXC-03452B Data Sheet:	Edition 6, April 2001
Previous L3M TXC-03452B Data Sheet:	Edition 5A, February 2000

The page numbers indicated below of this updated data sheet include changes relative to the previous data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
2 -3	Updated the Table of Contents and List of Figures.
12	Changed the PBGA Lead Diagram labels for leads K15 and K16 to Symbols TAIPF, TAIPD respectively.
22	In the Receive Desynchronizer table changed the lead Type for symbol CTRL.
23	In the Boundary Scan Testing Table, changed text of the Name/Function column for symbol $\overline{TRS}$.
24	Added Note 5 below the Absolute Maximum Ratings and Environmental Limitations table. In the Power Requirements Table changed the values in the Max column for I_{DD} and P_{DD}.
28	Added Note 2 for the RCLK duty cycle, below the table of Figure 8.
48	In the table below Figure 29, changed Boundary Scan Timing Min values for Symbols $t_{H(1)}$, $t_{SU(2)}$, and $t_{H(2)}$. Changed the value in the Max column for Symbol t_D.
54	Changed title of Figure 34, added clock input for Rx PRBS Generator, and added the note.
65	Added “Unequipped payload” to description of Symbol TPA1S00 (C2, Bit 3).
88	In the Related Products Section removed the fifth and last paragraphs.
91	Updated List of Data Sheet Changes.

- NOTES -

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