SYN155C Device
155-Mbit/s Synchronizer Clock & Data Output
TXC-02302B

DATA SHEET

FEATURES

- Transmits and receives at STS-3/STM-1 rates
- Compatible with available optical components
- Detects frame of incoming 155.52 Mbit/s signal, converts it to a 19.44 MByte/s or a 38.88 Mnib/s parallel signal, clock and frame on terminal side
- Receives 19.44 MByte/s or 38.88 Mnib/s data from terminal, converts to serial data on the line side
- Pseudo-ECL receive and transmit clock and data ports
- Provides loopback of clock and data in both directions
- Optionally performs scrambling/descrambling and B1 parity calculations
- Performance monitoring of the received signal includes:
  - Loss of Signal (LOS)
  - Out of Frame (OOF)
  - Loss of Frame (LOF)
  - Receive Frame Error (RFE)
- Compliant with ANSI and ITU-T (CCITT) documents:
  - ANSI T1.105-1991
  - ITU-T (CCITT) G.708
- Transmit and reference clock framing signal inversion capability

DESCRIPTION

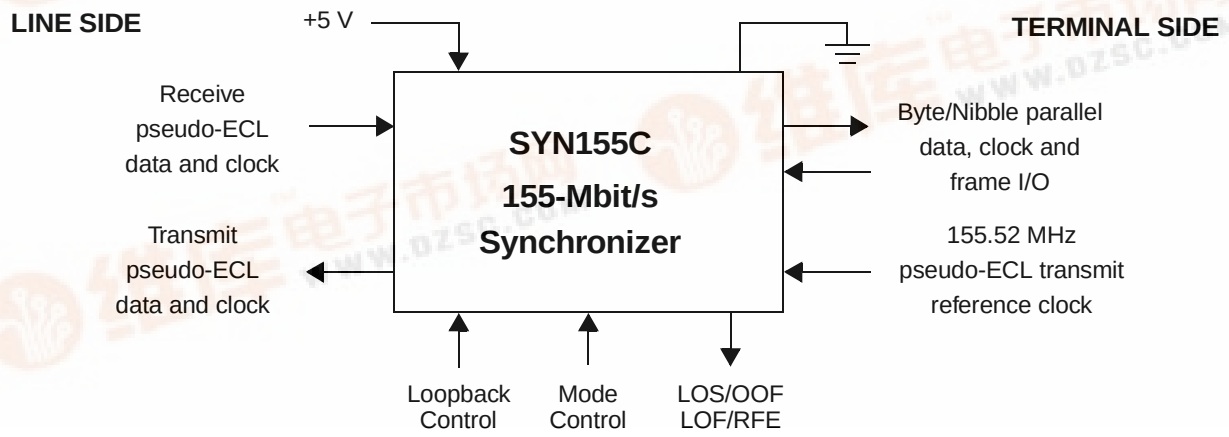
The SYN155C synchronizer device provides a complete STS-3/STM-1 frame synchronization function in a single low-power CMOS unit. The SYN155C performs the frame synchronization algorithm defined in ANSI/ITU-T (CCITT) publications on an incoming 155.52 Mbit/s signal, and outputs signal bytes or nibbles along with a byte/nibble clock and frame indication signal. In the transmit direction, bytes or nibbles from a SONET/SDH device are accepted and sent out in serial to the fiber transmitter with a separate transmit clock signal.

The SYN155C supports two frame synchronization modes: a full tracking mode which finds frame and verifies it on following frames; and a non-tracking mode which finds frame but performs no verification.

The serial line side is designed to connect directly to the fiber interface components using pseudo-ECL voltage levels (ECL operating from +5 V to ground), thus avoiding the need for ECL-to-TTL or ECL-to-CMOS level conversion.

APPLICATIONS

- STS-3/STM-1 transmit/receive using optical input/output
- Add/drop OC3 multiplexers
- Optical SONET bus extender
- Test and performance monitoring equipment



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LIST OF FIGURES

BLOCK DIAGRAM

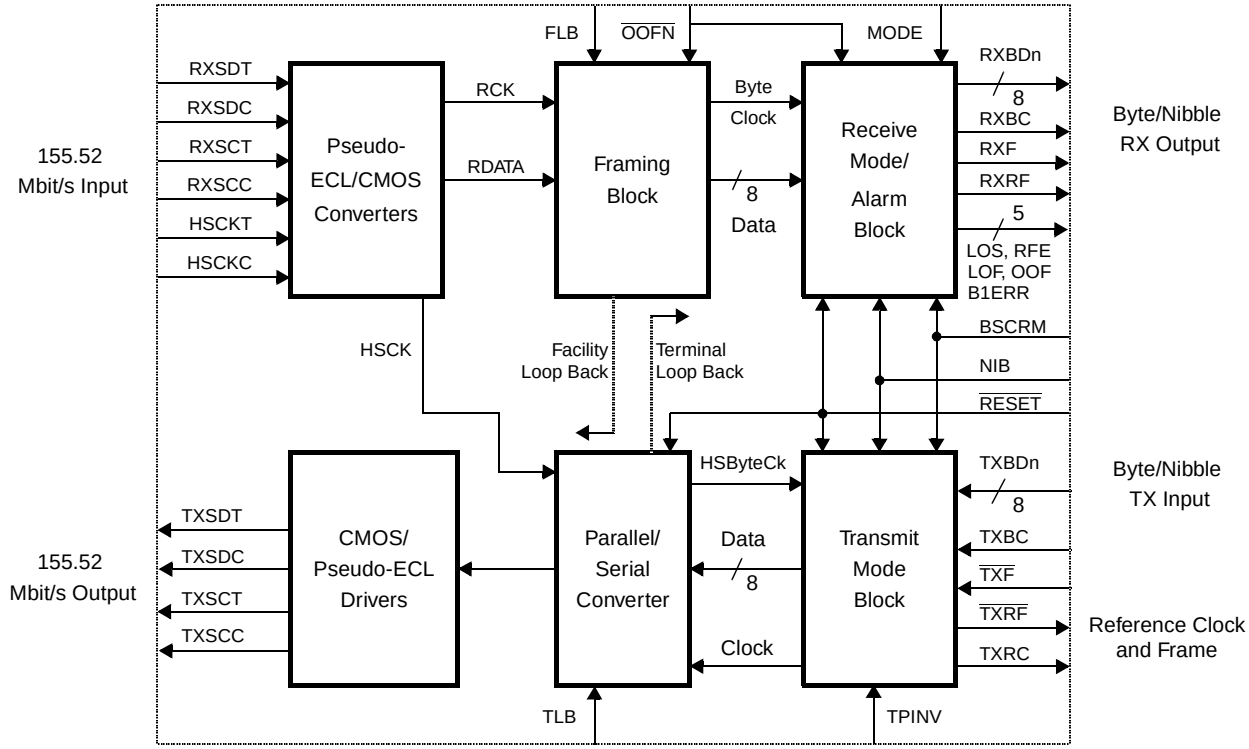


Figure 1. SYN155C TXC-02302B Block Diagram

BLOCK DIAGRAM DESCRIPTION

Figure 1 shows the block diagram of the SYN155C. The Pseudo-ECL/CMOS Converter Block converts the pseudo-ECL true and complement receive clocks (RXSCT and RXSCC), receive data (RXSDT and RXSDC), and reference clocks (HSCKT and HSCKC) to CMOS levels. Receive clock and data CMOS signals are then connected to the Framing Block which performs a serial search for the framing pattern in the STS-3/STS-3c/ STM-1 signal. Within the Framing Block, a new frame search can be initiated via $\overline{\text{OOFN}}$. After the framing pattern is detected, the serial data is converted to parallel data and sent to the Receive Mode/Alarm Block.

The Receive Mode/Alarm Block offers two framing modes -- full tracking and non-tracking -- which are selected by the control lead labeled MODE. In addition, this block provides descrambling and a nibble interface in the receive direction through selection of the control pins BSCRM and NIB, respectively.

The full tracking mode meets the framing algorithm requirements specified in ITU-T (CCITT) Recommendation G.709 and ANSI document T1.105. In the full tracking mode, the SYN155C performs the search for the first occurrence of the framing pattern (F6 Hex pattern), and then by bytes to check if it is part of the frame sequence. If it is not, then the bit-serial search shall be reinitiated at the bit phase at which it was interrupted. This pattern is continued until the framing pattern is found. Then it is validated by looking at a byte occurrence one frame later. The SYN155C holds the receive frame pulse (RXF) low prior to validation and when an out of frame (OOF) occurs. However, the SYN155C does not force the receive data (RXBDn) to zero. As a result, the receive data may be corrupt. When frame alignment is acquired, the receive frame pulse (RXF) is sent, and the data (RXBDn) is valid. In the full tracking mode, loss of frame (LOF), receive framing error (RFE), and OOF alarm indications are provided.

In the non-tracking mode (MODE lead is high), the SYN155C searches for the first occurrence of the framing pattern and assumes it is valid. External circuitry is required to validate that the framing pattern repeats every 125 microseconds. If this fails, the external circuitry gives an $\overline{\text{OOFN}}$ signal, which causes the SYN155C to reinitiate the search for frame alignment. In the non-tracking mode, loss of frame (LOF), receive framing error (RFE), and out of frame (OOF) alarm indications are not valid.

The scramble and B1 parity functions are enabled by forcing a high on the control lead labeled BSCRM for both the receive and transmit directions, and in either the full tracking mode or non-tracking mode. When enabled, all transmitted data after the third C1 byte is scrambled. In the receive direction, data is descrambled and B1 parity error indications are provided on the output signal lead labeled B1ERR. These indications are also sent out in the B1 byte of the receive terminal STS-3/STS-3c/STM-1 data signal. In the transmit direction, the B1 byte of the transmit terminal interface STS-3/STS-3c/STM-1 data signal is exclusive-OR gated with the internally calculated B1 value and the resulting value is transmitted in the B1 byte of the following frame. This permits the SYN155C to generate one or more parity errors. To avoid the transmission of B1 parity errors, the transmit terminal interface value of the B1 byte must be 00H.

The nibble interface is selected by placing a high on the control lead labeled NIB for both the receive and transmit directions. The nibble/byte output provides either a terminal side nibble interface (RXBD3-0), or a byte interface (RXBD7-0). The most significant bit (MSB), which is the first bit received, is provided on the RXBD3 lead for the nibble interface and on the RXBD7 lead for the byte interface.

The Transmit Mode Block provides the nibble/byte and scramble functions in the transmit direction. Nibble data (TXBD3-0) or byte data (TXBD7-0) is clocked into the Transmit Mode Block on negative transitions of the clock signal TXBC when the TPINV lead is low. When TPINV is high, data is clocked into the SYN155C on positive transitions of the clock signal. In addition, the transmit framing pulse ($\overline{\text{TXF}}$) is active high. The MSB is TXBD3 (nibble interface) and TXBD7 (byte interface) which correspond to the first bit transmitted. The location of nibbles or bytes in the STS-3/STS-3c/STM-1 signal required for the scrambling and B1 parity functions is determined by the framing pulse ($\overline{\text{TXF}}$). The Transmit Mode Block also provides a transmit reference generator which can be used by the terminal circuitry for framing and clocking out the data. The generator signal consists of a nibble or byte rate clock signal (TXRC) and an active low framing pulse ($\overline{\text{TXRF}}$) generated from the 155.52 MHz clock signals (HSCKT and HSCKC) when the TPINV lead is low. When the TPINV lead is high, the $\overline{\text{TXRF}}$ signal is active high, and clocked out of the SYN155C on negative transitions of the clock (TXRC).

The output of the Transmit Mode Block is connected to the Parallel/Serial Converter Block which converts the parallel data to serial pseudo-ECL true and complement transmit clocks (TXSCT and TXSCC) and transmit data (TXSDT and TXSDC) from CMOS levels using the HSCK clock signal.

For testing purposes, the SYN155C provides facility and terminal loopback capability.

PIN DIAGRAM

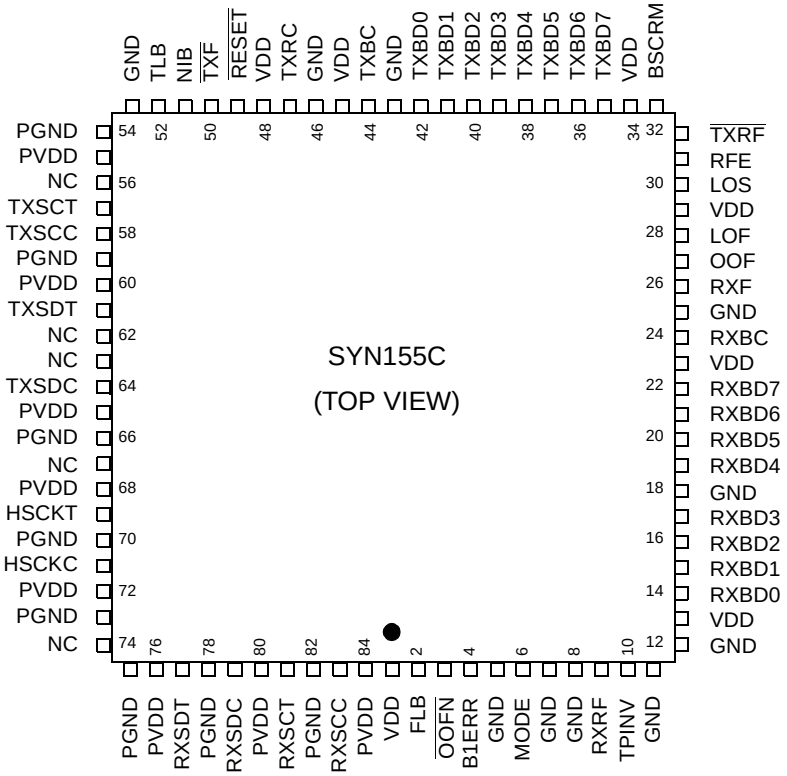


Figure 2. SYN155C TXC-02302B Pin Diagram

PIN DESCRIPTIONS

Power Supply and Ground

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	1,13,23,29,34,45,48	P	--	5 volt supply voltage, ±5%
PVDD	55,60,65,68,72, 76,80,84	P	--	Pseudo-ECL 5-volt supply voltage, ±5%
GND	5,7,8,11,12,18,25, 43,46,53	P	--	Ground
PGND	54,59,66,70,73, 75,78,82	P	--	Ground, pseudo-ECL circuits
NC	56,62,63,67,74	--	--	No internal connection (existing designs, leave floating or ground; new designs, leave floating)

*Note: I = Input; O = Output; P = Power

High-Speed Clock Transmit Reference

*Note: Pseudo-ECL input/output lines must be properly terminated to avoid interface problems. Please refer to Figure 25.

Symbol	Pin No.	I/O/P	Type *	Name/Function
HSCKT	69	I	Pseudo-ECL	**High Speed Clock True:** This 155.52 MHz (± 20 ppm) reference transmit clock and its complement HSCKC provide the clock for the transmit side clock and data, and reference clock and frame. Refer to Figure 25 for required 50 ohm termination.
HSCKC	71	I	Pseudo-ECL	**High Speed Clock Complement:** Refer to Figure 25 for required 50 ohm termination.

Pseudo-ECL Line Side Input/Output

*Note: Pseudo-ECL input/output lines must be properly terminated to avoid interface problems. Please refer to Figure 25.

Symbol	Pin No.	I/O/P	Type	Name/Function
TXSDT	61	O	Pseudo-ECL	**Transmit Serial Data True** (pseudo-ECL levels): This lead, with its complement TXSDC, can be used to drive a fiber optic transmitter. Data is clocked out relative to the falling edge of TXSCT. Refer to Figure 25 for required 50 ohm termination.
TXSDC	64	O	Pseudo-ECL	**Transmit Serial Data Complement:** Refer to Figure 25 for required 50 ohm termination.
TXSCT	57	O	Pseudo-ECL	**Transmit Serial Clock True** (pseudo-ECL Levels): This lead, with its complement TXSCC, is the output clock. Refer to Figure 25 for required 50 ohm termination.
TXSCC	58	O	Pseudo-ECL	**Transmit Serial Clock Complement:** Refer to Figure 25 for required 50 ohm termination.
RXSDT	77	I	Pseudo-ECL	**Receive Serial Data True** (pseudo-ECL levels): This lead, with its complement RXSDC, is the input data to the SYN155C. Data is sampled on the rising edge of RXSCT. Refer to Figure 25 for required 50 ohm termination.
RXSDC	79	I	Pseudo-ECL	**Receive Serial Data Complement**: Refer to Figure 25 for required 50 ohm termination.
RXSCT	81	I	Pseudo-ECL	**Receive Serial Clock True** (pseudo-ECL levels): This lead, with its complement RXSCC, is the input clock that accompanies the data on RXSDT and RXSDC. Refer to Figure 25 for required 50 ohm termination.
RXSCC	83	I	Pseudo-ECL	**Receive Serial Clock Complement:** Refer to Figure 25 for required 50 ohm termination.

*See Input and Output Parameters section below for Type definitions.

Terminal Side Input/Output

Symbol	Pin No.	I/O/P	Type	Name/Function
RXBD(7-0)	22-19,17-14	O	CMOS4mA	**Receive Byte Data:** Byte-wide data is received most significant bit (MSB) first on RXBD7, at a byte rate of 19.44 Mbyte/s. In the nibble mode, nibble-wide data is received MSB on RXBD3 at a nibble rate of 38.88 Mnibble/s. Receive data is still provided when out of frame occurs.
RXBC	24	O	CMOS4mA	**Receive Byte/Nibble Clock:** The clock rate is 19.44 MHz in the byte mode, and 38.88 MHz in the nibble mode. Data (RXBDn) is clocked out on falling transitions of this clock.
RXF	26	O	CMOS4mA	**Receive Framing Pulse:** The positive receive framing pulse is synchronized with the last byte or nibble pair in the received framing pattern (28 Hex). When OOF occurs, the receive framing pulse is held low.
TXBD(7-0)	35-42	I	CMOS	**Transmit Byte Data:** Byte-wide data is transmitted most significant bit (MSB) first on TXBD7, at a byte rate of 19.44 Mbyte/s. In the nibble mode, nibble-wide data is transmitted MSB on TXBD3 at a nibble rate of 38.88 Mnibble/s.
TXBC	44	I	CMOS	**Transmit Byte/Nibble Clock:** The clock rate is 19.44 MHz in the byte mode, and 38.88 MHz in the nibble mode. Data (TXBDn) is clocked in on negative transitions of this clock when the TPINV lead is low, and on positive transitions when the TPINV lead is high.
$\overline{\text{TXF}}$	50	I	CMOS	**Transmit Framing Pulse:** The transmit framing pulse is synchronized with the last byte or nibble pair in the transmit framing pattern (28 Hex). The transmit framing pulse is an active low when the TPINV lead is low, and active high when the TPINV lead is high.
$\overline{\text{TXRF}}$	32	O	CMOS4mA	**Transmit Reference Framing Pulse:** The negative transmit reference framing pulse is one clock cycle wide and has a frame rate of 8 KHz. The transmit reference framing pulse is active low when the TPINV lead is low, and active high when the TPINV lead is high.
TXRC	47	O	CMOS4mA	**Transmit Reference Clock:** The transmit reference clock rate is 19.44 MHz in the byte mode, and 38.88 MHz in the nibble mode. The transmit reference framing pulse ($\overline{\text{TXRF}}$) is clocked out on the positive transition of this clock when the TPINV lead is low, and negative transitions when the TPINV lead is high.
RXRF	9	O	TTL4mA	**Receive Reference Framing Pulse:** The positive receive reference frame is one clock cycle wide and has a frame rate of 8 KHz.The frame rate is derived by dividing the recovered line input clock by 19440 (155.52 MHz/ 8000), and it is therefore exactly synchronous with the input (and output) data. The phase of the RXRF pulse with respect to the output data is not specified.

Alarm Signal Input/Output

Symbol	Pin No.	I/O/P	Type	Name/Function
B1ERR	4	O	CMOS4mA	**B1 Parity Error Indication:** A positive pulse error indication is provided for each B1 bit parity error, up to a maximum of eight error indications. Each error indication is one clock cycle wide in the byte mode, and two clock cycles wide in the nibble mode.
RFE	31	O	CMOS4mA	**Receive Framing Error:** A receive framing error is declared when any bit in the framing pattern is in error, and the SYN155C is not out of frame. When present, the indication occurs at the start of the third A2 framing byte (28 Hex) of the framing pattern in the receive terminal-side data (RXBD). The timing for this signal is identical to that of RXF. This indication is valid only in the full-tracking mode.
OOF	27	O	CMOS4mA	**Out of Frame:** An out of frame alarm occurs when errors are detected in the three A2 bytes of four consecutive framing patterns (i.e., A2A2A2≠282828, Hex) while in frame alignment. The OOF alarm state is exited when two complete consecutive framing patterns (i.e., F6F6F6282828, Hex) are detected correctly. This indication is valid only in the full tracking mode. Note that the A1=F6 Hex is not required for recovering frame. Further, bit errors in the three A1 bytes cause an RFE pulse, but they do not contribute to the OOF state.
LOF	28	O	CMOS4mA	**Loss of Frame:** A loss of frame (LOF) alarm will occur if the OOF state persists for a minimum of between 2.875 milliseconds and 3.125 milliseconds. The LOF alarm state is exited when eight correct framing patterns are detected after the OOF alarm state is exited. This alarm state is valid in the full tracking mode only.
LOS	30	O	TTL4mA	**Loss of Signal:** A loss of signal alarm will occur when the incoming signal, before descrambling, is stuck high or low for 26 microseconds ± 1 microsecond, or if the clock is stuck high or low for one microsecond ± 750 nanoseconds. Recovery occurs when two consecutive frame alignment patterns are detected, in which loss of signal did not occur between the frame alignment patterns.

Control Lead Inputs*

*Note: All control input leads must be tied to the inactive logic reference level (VDD or GND) when not in use. They must not be left unconnected.

Symbol	Pin No.	I/O/P	Type	Name/Function
FLB	2	I	TTL	**Facility Loopback:** When a high is placed on this lead, received pseudo-ECL data is looped back as transmit pseudo-ECL data. Receive data is provided at the terminal side, but transmit terminal data is disabled. FLB and TLB may not be used at the same time; doing so will produce invalid results.
TLB	52	I	TTL	**Terminal Loopback:** When a high is placed on this lead, transmit terminal data is looped back as receive terminal data. Transmit data is provided at the pseudo-ECL interface, but receive data from the pseudo-ECL interface is disabled. TLB and FLB may not be used at the same time; doing so will produce invalid results.
BSCRM	33	I	TTL	**B1 Generator/Detector & Scramble/Descrambler:** A high enables the B1 parity generator/detector and the scrambler/descrambler. These features are disabled when BSCRM = 0. When enabled, all transmitted data after the third C1 byte is scrambled. In the receive direction, data is descrambled and B1 parity error indications are provided on the output signal lead labeled B1ERR. These indications are also sent out in the B1 byte of the receive terminal STS-3/STS-3c/STM-1 data signal. In the transmit direction, the B1 byte of the transmit terminal interface STS-3/STS-3c/STM-1 data signal is exclusive-OR gated with the internally calculated B1 value and the resulting value is transmitted in the B1 byte of the following frame. This permits the SYN155C to generate one or more parity errors. To avoid the transmission of B1 parity errors, the transmit terminal interface value of the B1 byte must be 00H.
MODE	6	I	TTL	**Mode:** A low enables the full tracking mode. In the full tracking mode, the SYN155C searches and tracks frame alignment. The framing pulse (RXF) is held low when out of frame occurs, however, byte/nibble data is provided. The non-tracking mode is selected by placing a high on this lead. In the non-tracking mode, frame alignment is declared valid on the first indication of the framing pattern, not the second. If the external circuitry finds that the frame pattern is false in its validation process, it sends an $\overline{\text{OOFN}}$ signal to reinitiate the frame search.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RESET}}$	49	I	CMOS	**Reset:** The SYN155C is reset when the reset pulse is held low for a minimum of 105 nanoseconds. The SYN155C must be reset after power is applied, or when the following control leads are changed during operation: BSCRM, MODE, or NIB. Refer to Note 1.
NIB	51	I	TTL	**Nibble/Byte Control Lead:** A high selects the nibble interface, while a low selects the byte interface.
TPINV	10	I	TTL	**Transmit Clock/Reference Invert:** A high on this lead inverts the transmit clock and framing pulse inputs. The positive framing pulse is clocked into the SYN155C on positive transitions of the transmit byte/nibble clock (TXBC). In addition, the transmit reference clock and framing pulse output signals are inverted. The positive reference framing pulse is clocked out on negative transitions of the reference clock (TXRC). When a low is applied to this pin, the negative framing pulse is clocked into the SYN155C on negative transitions of the transmit byte/nibble clock (TXBC). The negative reference framing pulse is clocked out on positive transitions of the reference clock (TXRC).
$\overline{\text{OOFN}}$	3	I	CMOS	**Out of Frame Negative:** An active low signal having a duration of at least two clock (RXBC) cycles causes a frame alignment search. Refer to Note 1.

Note 1: A $\overline{\text{RESET}}$ and $\overline{\text{OOFN}}$ should be applied after any mode change occurs. The $\overline{\text{OOFN}}$ must be at the same time or after a $\overline{\text{RESET}}$ becomes inactive.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	MIn	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	7.0	V	Note 1
Pseudo-ECL supply voltage	V_{PECL}		7.0	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Storage temperature range	T_S	-55	150	^oC	
Component temperature x time	TI		270 x 5	^oC x s	Note 1
Moisture Exposure Level	ME	5		Level	Per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient, Θ_{JA}			41.6	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
V_{PECL}	4.75	5.0	5.25	V	
I_{DD} + I_{PECL} (Note 1)		150	175	mA	f_i = 155.52 Mbit/s
P_{DD} + P_{PECL}		750	920	mW	V_{DD} = 5.25; Inputs switching V_{PECL} = 4.75; Inputs switching

Note 1:PECL outputs are terminated with 50Ω to 3V.

INPUT AND OUTPUT PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

Input Parameters For CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

Input Parameters For Pseudo-ECL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.7		4.0	V	$4.75 \leq V_{PECL} \leq 5.25$
V_{IL}	3.0		3.3	V	$4.75 \leq V_{PECL} \leq 5.25$
Input leakage current			1.0	µA	$V_{PECL} = 5.25$
Gate capacitance			10	pF	

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -2.0$
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.5	5.5	10.0	ns	$C_{LOAD} = 15$ pF
t_{FALL}	1.0	2.0	4.0	ns	$C_{LOAD} = 15$ pF

Output Parameters For CMOS4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.5	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	1.6*	2.6*	4.3*	ns	C_{LOAD} = 15pF
t_{FALL}	1.8*	2.8*	4.2*	ns	C_{LOAD} = 15pF

*These are calculated values.

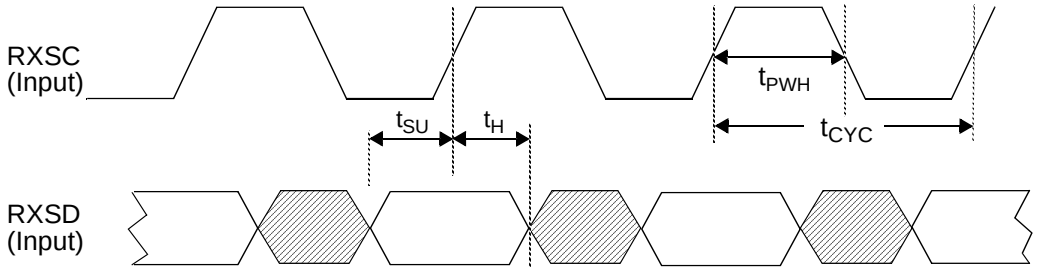
Output Parameters for Pseudo-ECL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	4.0		4.3	V	V_{PECL} = 5; I_{OH} = -22.4
V_{OL}	3.0		3.4	V	V_{PECL} = 5; I_{OL} = 7.6
I_{OL}			7.6	mA	
I_{OH}			-22.4	mA	
t_{RISE}	0.0		1.2	ns	C_{LOAD} = 25pF
t_{FALL}	0.0		1.2	ns	C_{LOAD} = 25pF

TIMING CHARACTERISTICS

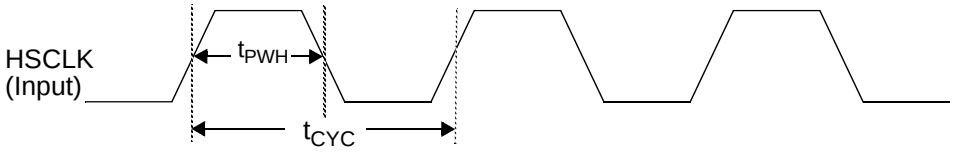
Detailed timing diagrams for the SYN155C are illustrated in Figures 3 through 23, with values of the timing intervals tabulated below the signal waveforms. All output times are measured with a maximum 25 pF load capacitance. Timing parameters are measured at $(V_{OH} + V_{OL})/2$ or $(V_{IH} + V_{IL})/2$, as applicable. For simplicity, all pseudo-ECL waveforms are shown using the TRUE signals only.

Figure 3. Line Side Pseudo-ECL Input



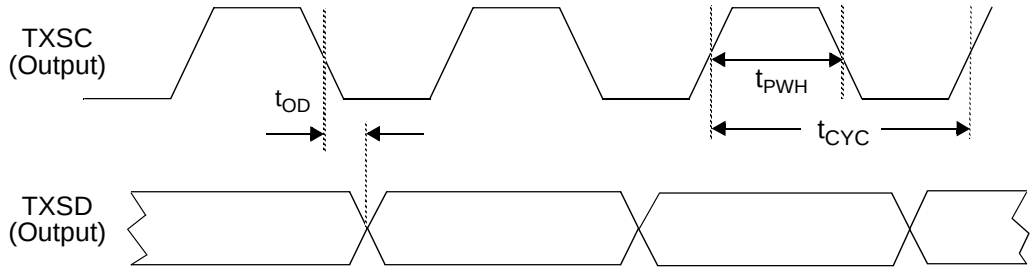
Parameter	Symbol	Min	Typ	Max	Unit
RXSC clock period	t_{CYC}		6.43		ns
RXSC duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
RXSD set-up time to RXSC↑	t_{SU}	2.0			ns
RXSD hold time after RXSC↑	t_H	1.0			ns

Figure 4. Reference Pseudo-ECL Input



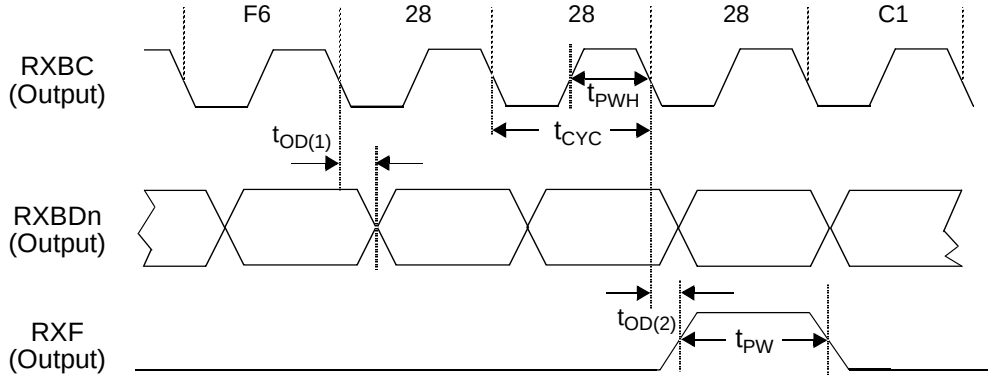
Parameter	Symbol	Min	Typ	Max	Unit
HSCLK clock period	t_{CYC}		6.43		ns
HSCLK duty cycle (t_{PWH}/t_{CYC})	--	45		55	%

Figure 5. Line Side Pseudo-ECL Output



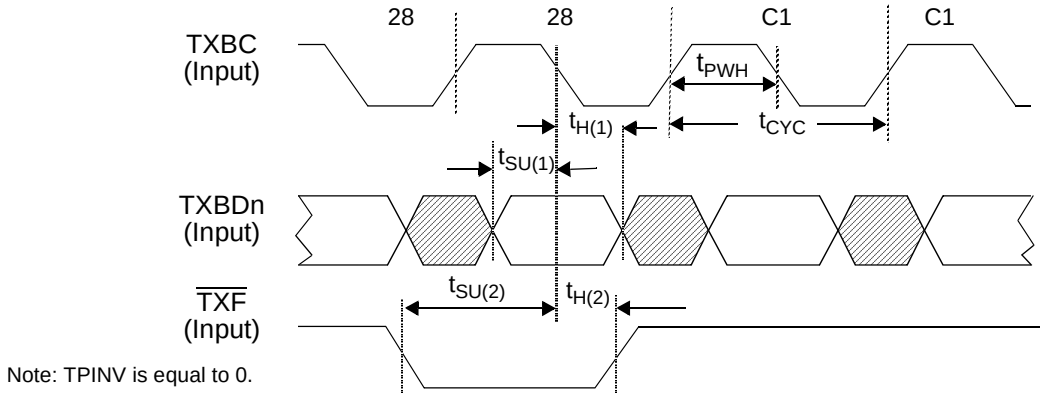
Parameter	Symbol	Min	Typ	Max	Unit
TXSC clock period	t_{CYC}		6.43		ns
TXSC duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TXSD output delay after TXSC↓	t_{OD}	-1.7		1.9	ns

Figure 6. Terminal Side Byte Output



Parameter	Symbol	Min	Typ	Max	Unit
RXBC clock period	t_{CYC}		51.44		ns
RXBC duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
RXBD output delay after RXBC↓	$t_{OD(1)}$	-1.0		6.0	ns
RXF output delay after RXBC↓	$t_{OD(2)}$	0.0		6.0	ns
RXF pulse width	t_{PW}		51.44		ns

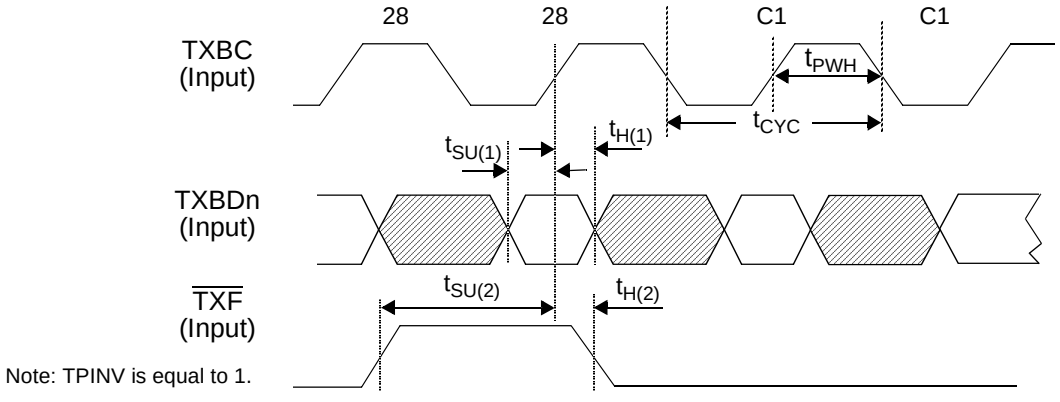
Figure 7. Terminal Side Byte Input



Note: TPINV is equal to 0.

Parameter	Symbol	Min	Typ	Max	Unit
TXBC clock period	t_{CYC}		51.44		ns
TXBC duty cycle (t_{PWH}/t_{CYC})	--	35		65	%
TXBDn set-up time to TXBC↓	$t_{SU(1)}$	5.0			ns
TXBDn hold time after TXBC↓	$t_{H(1)}$	5.0			ns
$\overline{TXF}$ set-up time to TXBC↓	$t_{SU(2)}$	5.0			ns
$\overline{TXF}$ hold time after TXBC↓	$t_{H(2)}$	5.0			ns

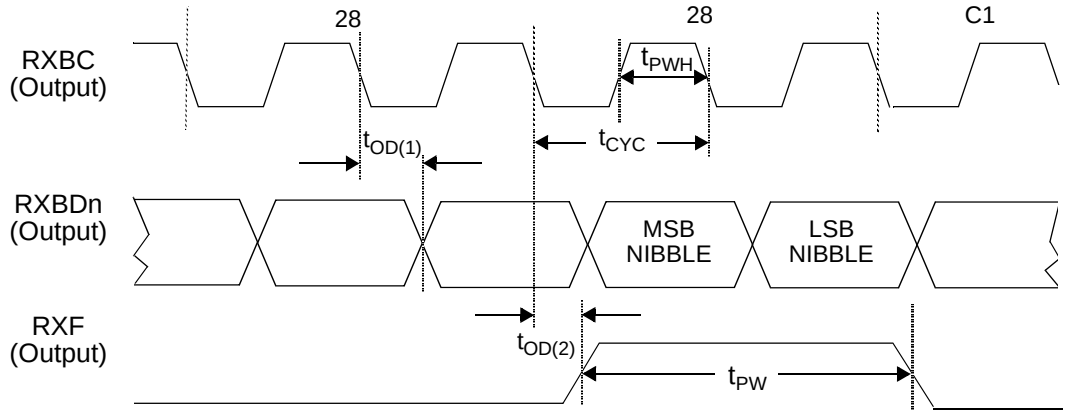
Figure 8. Terminal Side Byte Input



Note: TPINV is equal to 1.

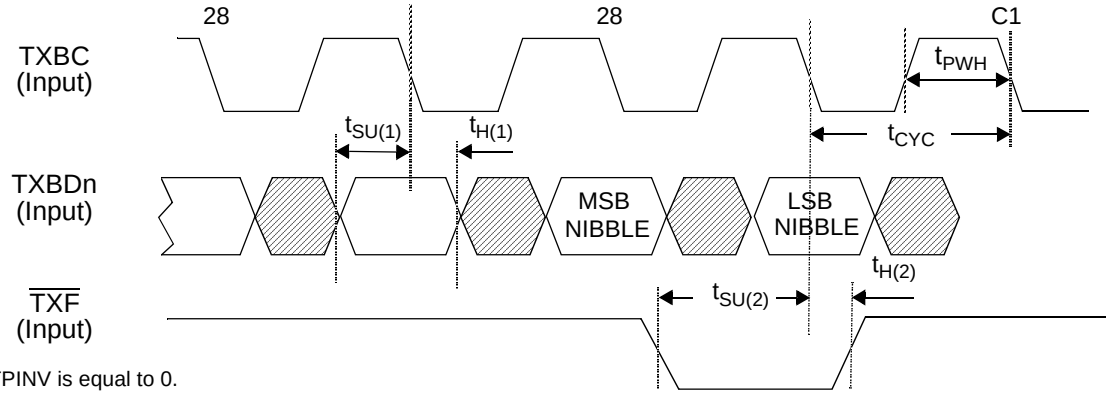
Parameter	Symbol	Min	Typ	Max	Unit
TXBC clock period	t_{CYC}		51.44		ns
TXBC duty cycle (t_{PWH}/t_{CYC})		35		65	%
TXBDn set-up time to TXBC↑	$t_{SU(1)}$	5.0			ns
TXBDn hold time after TXBC↑	$t_{H(1)}$	5.0			ns
$\overline{TXF}$ set-up time to TXBC↑	$t_{SU(2)}$	5.0			ns
$\overline{TXF}$ hold time after TXBC↑	$t_{H(2)}$	5.0			ns

Figure 9. Terminal Side Nibble Output



Parameter	Symbol	Min	Typ	Max	Unit
RXBC clock period	t_{CYC}		25.72		ns
RXBC duty cycle (t_{PWH}/t_{CYC})	--	35		65	%
RXBDn output delay after RXBC↓	$t_{OD(1)}$	-1.0		6.0	ns
RXF output delay after RXBC↓	$t_{OD(2)}$	0.0		6.0	ns
RXF pulse width	t_{PW}		51.44		ns

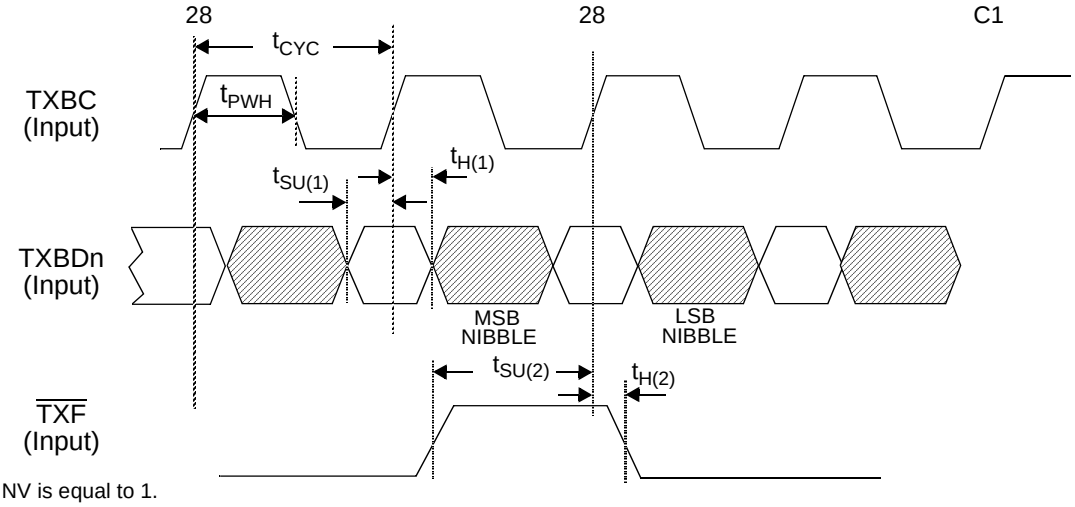
Figure 10. Terminal Side Nibble Input



Note: TPINV is equal to 0.

Parameter	Symbol	Min	Typ	Max	Unit
TXBC clock period	t_{CYC}		25.72		ns
TXBC duty cycle (t_{PWH}/t_{CYC})	--	35		65	%
TXBDn set-up time to TXBC↓	$t_{SU(1)}$	5.0			ns
TXBDn hold time after TXBC↓	$t_{H(1)}$	5.0			ns
$\overline{TXF}$ set-up time to TXBC↓	$t_{SU(2)}$	5.0			ns
$\overline{TXF}$ hold time after TXBC↓	$t_{H(2)}$	5.0			ns

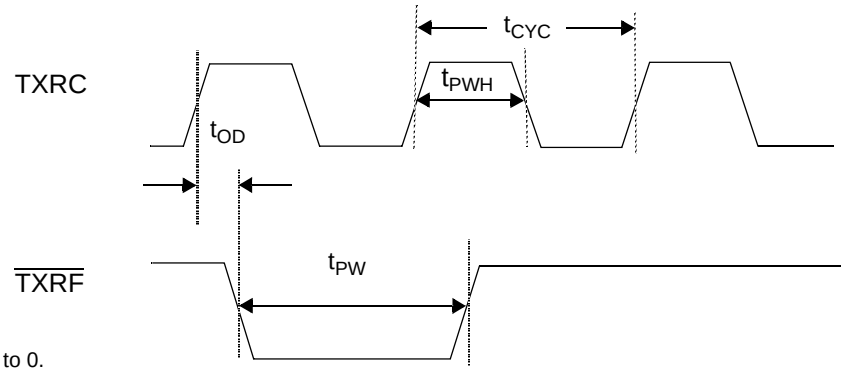
Figure 11. Terminal Side Nibble Input



Note: TPINV is equal to 1.

Parameter	Symbol	Min	Typ	Max	Unit
TXBC clock period	t_{CYC}		25.72		ns
TXBC duty cycle (t_{PWH}/t_{CYC})	--	35		65	%
TXBDn set-up time to TXBC↑	$t_{SU(1)}$	5.0			ns
TXBDn hold time after TXBC↑	$t_{H(1)}$	5.0			ns
$\overline{TXF}$ set-up time to TXBC↑	$t_{SU(2)}$	5.0			ns
$\overline{TXF}$ hold time after TXBC↑	$t_{H(2)}$	5.0			ns

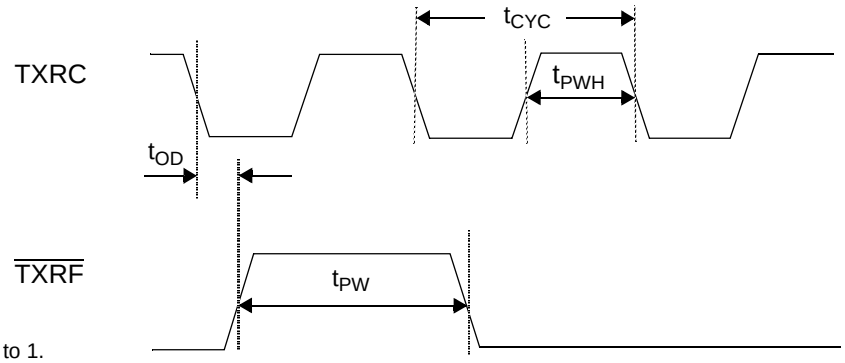
Figure 12. Terminal Side Byte Reference Signal Output



Note: TPINV is equal to 0.

Parameter	Symbol	Min	Typ	Max	Unit
TXRC clock period	t_{CYC}		51.44		ns
TXRC duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
$\overline{TXRF}$ output delay after TXRC↑	t_{OD}	0.0		6.0	ns
$\overline{TXRF}$ pulse width	t_{PW}		51.44		ns

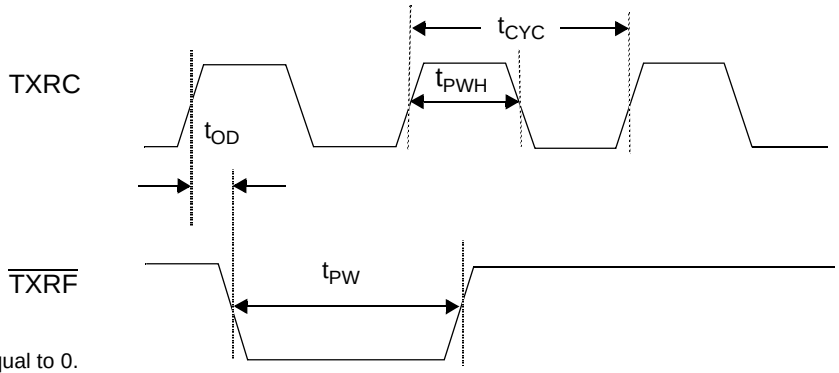
Figure 13. Terminal Side Byte Reference Signal Output



Note: TPINV is equal to 1.

Parameter	Symbol	Min	Typ	Max	Unit
TXRC clock period	t_{CYC}		51.44		ns
TXRC duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
$\overline{\text{TXRF}}$ output delay after TXRC↓	t_{OD}	0.0		6.0	ns
$\overline{\text{TXRF}}$ pulse width	t_{PW}		51.44		ns

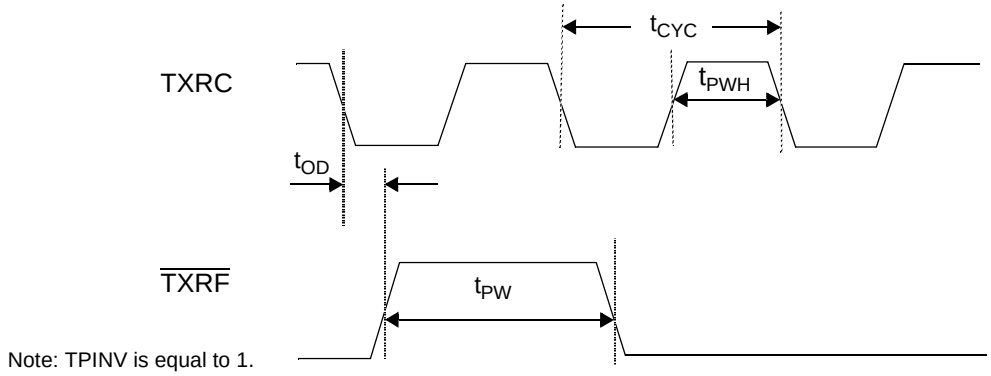
Figure 14. Terminal Side Nibble Reference Signal Output



Note: TPINV is equal to 0.

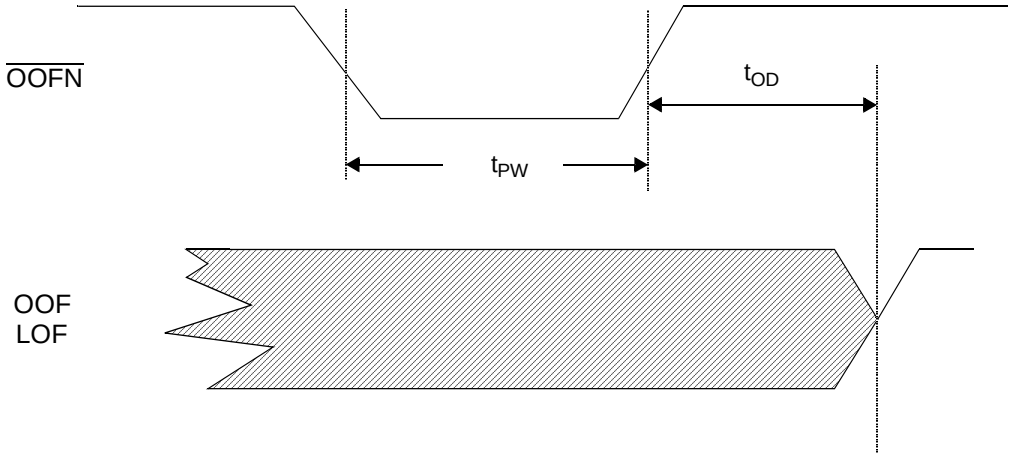
Parameter	Symbol	Min	Typ	Max	Unit
TXRC clock period	t_{CYC}		25.72		ns
TXRC duty cycle (t_{PWH}/t_{CYC})	--	35		65	%
$\overline{\text{TXRF}}$ output delay after TXRC↑	t_{OD}	0.0		6.0	ns
$\overline{\text{TXRF}}$ pulse width	t_{PW}		25.72		ns

Figure 15. Terminal Side Nibble Reference Signal Output



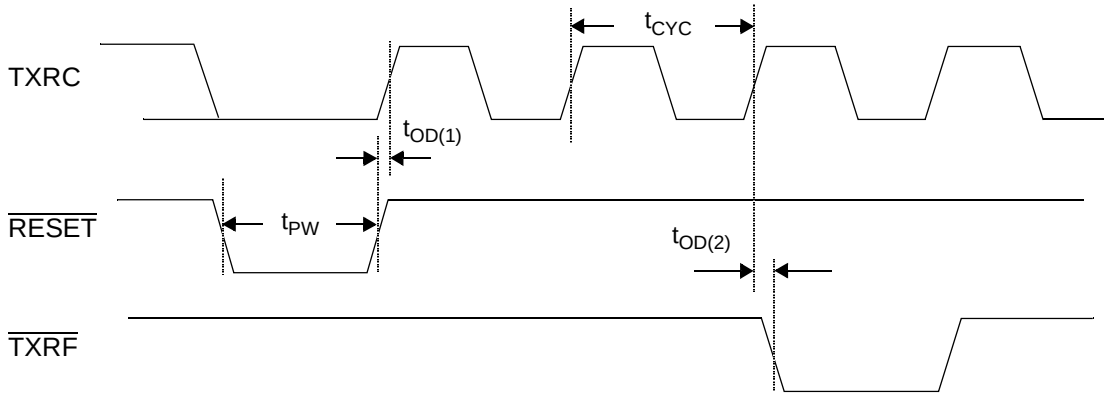
Parameter	Symbol	Min	Typ	Max	Unit
TXRC clock period	t_{CYC}		25.72		ns
TXRC duty cycle (t_{PWH}/t_{CYC})	--	35		65	%
$\overline{TXRF}$ output delay after TXRC↓	t_{OD}	0.0		6.0	ns
$\overline{TXRF}$ pulse width	t_{PW}		25.72		ns

Figure 16. $\overline{OOFN}$ Resetting Framing



Parameter	Symbol	Min	Typ	Max	Unit
OOF/LOF output delay after $\overline{OOFN}$ ↑	t_{OD}	0.0		312	ns
$\overline{OOFN}$ pulse width	t_{PW}	105			ns

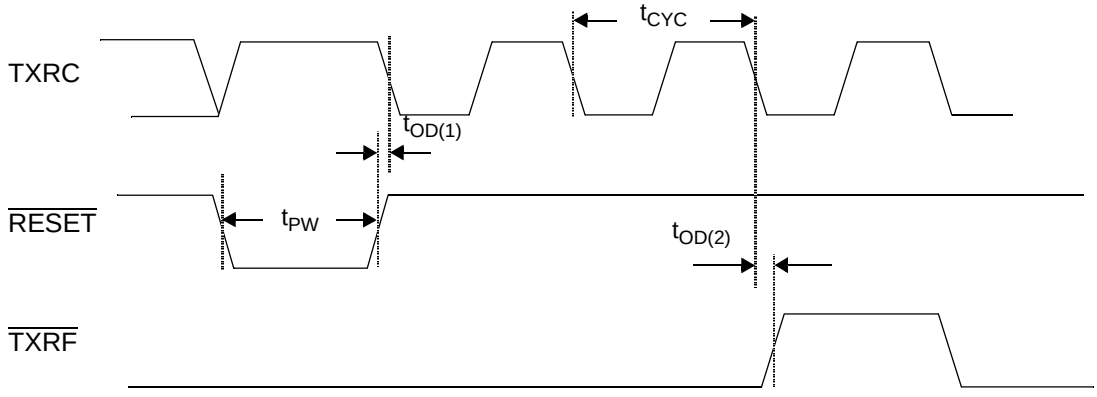
Figure 17. $\overline{\text{RESET}}$ Timing - Byte Mode



Note: TPINV is equal to 0.

Parameter	Symbol	Min	Typ	Max	Unit
TXRC clock period	t_{CYC}		51.44		ns
TXRC output delay after $\overline{\text{RESET}}$ ↑	$t_{OD(1)}$	6.0		30	ns
$\overline{\text{TXRF}}$ output delay after TXRC↑	$t_{OD(2)}$	0.0		6.0	ns
$\overline{\text{RESET}}$ pulse width	t_{PW}	105			ns

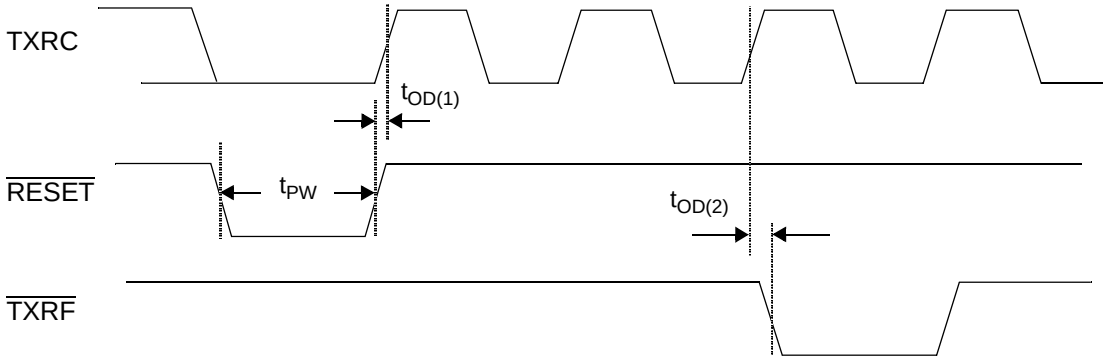
Figure 18. $\overline{\text{RESET}}$ Timing - Byte Mode



Note: TPINV is equal to 1.

Parameter	Symbol	Min	Typ	Max	Unit
TXRC clock period	t_{CYC}		51.44		ns
TXRC output delay after $\overline{\text{RESET}}$ ↑	$t_{OD(1)}$	6.0		30	ns
$\overline{\text{TXRF}}$ output delay after TXRC↓	$t_{OD(2)}$	0.0		6.0	ns
$\overline{\text{RESET}}$ pulse width	t_{PW}	105			ns

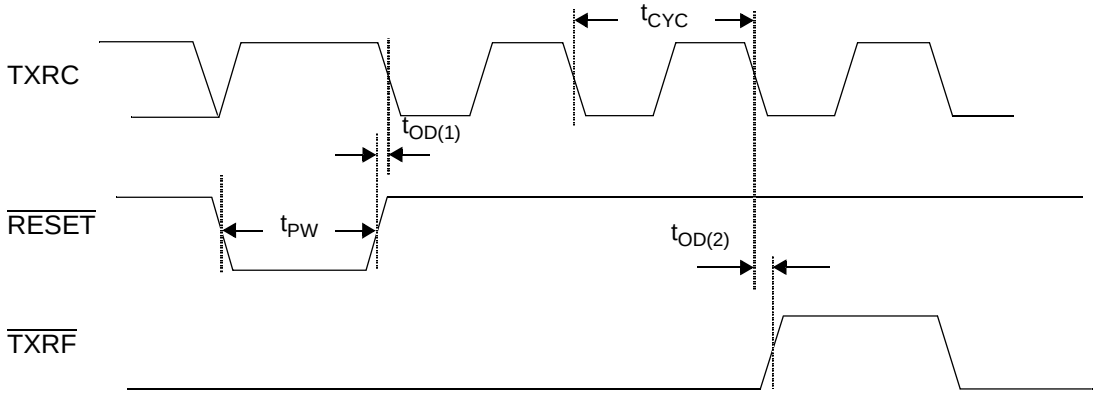
Figure 19. $\overline{\text{RESET}}$ Timing - Nibble Mode



Note: TPINV is equal to 0.

Parameter	Symbol	Min	Typ	Max	Unit
TXRC clock period	t_{CYC}		25.72		ns
TXRC output delay after $\overline{\text{RESET}}$ ↑	$t_{OD(1)}$	6.0		30	ns
$\overline{\text{TXRF}}$ output delay after TXRC↑	$t_{OD(2)}$	0.0		6.0	ns
$\overline{\text{RESET}}$ pulse width	t_{PW}	105			ns

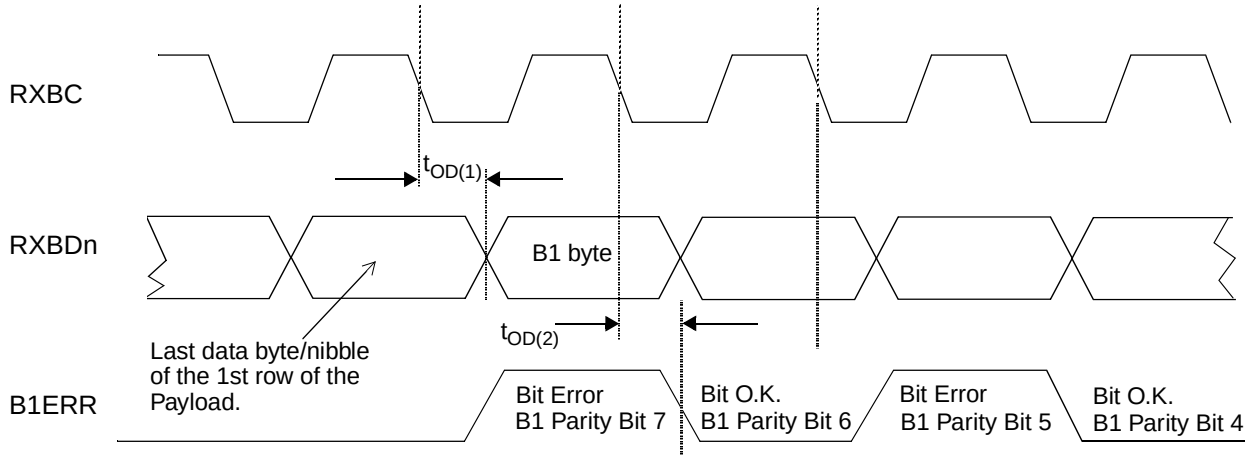
Figure 20. $\overline{\text{RESET}}$ Timing - Nibble Mode



Note: TPINV is equal to 1.

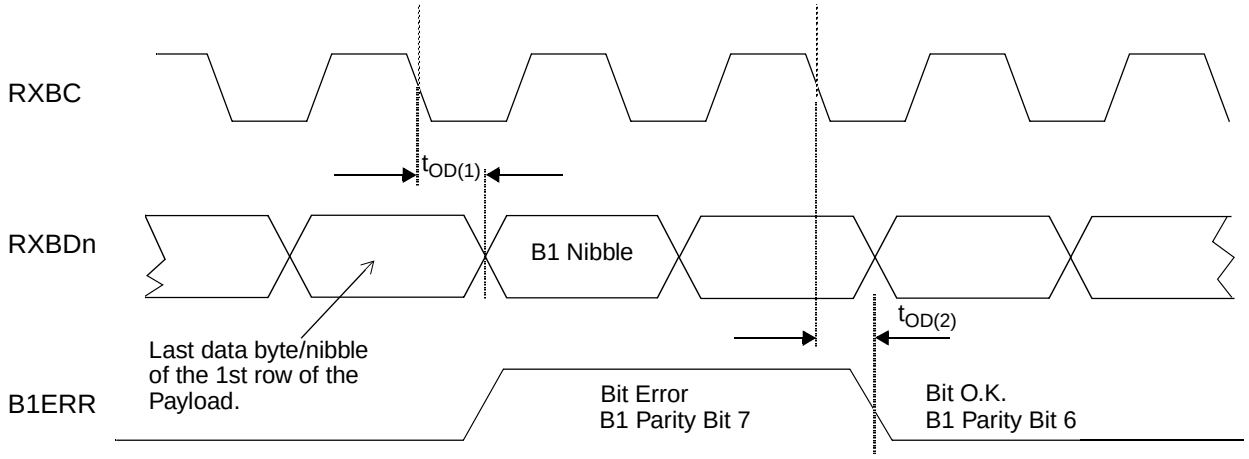
Parameter	Symbol	Min	Typ	Max	Unit
TXRC clock period	t_{CYC}		25.72		ns
TXRC output delay after $\overline{\text{RESET}}$ ↑	$t_{OD(1)}$	6.0		30	ns
$\overline{\text{TXRF}}$ output delay after TXRC↓	$t_{OD(2)}$	0.0		6.0	ns
$\overline{\text{RESET}}$ pulse width	t_{PW}	105			ns

Figure 21. B1 Error Pulse Byte Timing
(Four time slots are illustrated; up to eight bits may be in error in a given frame)



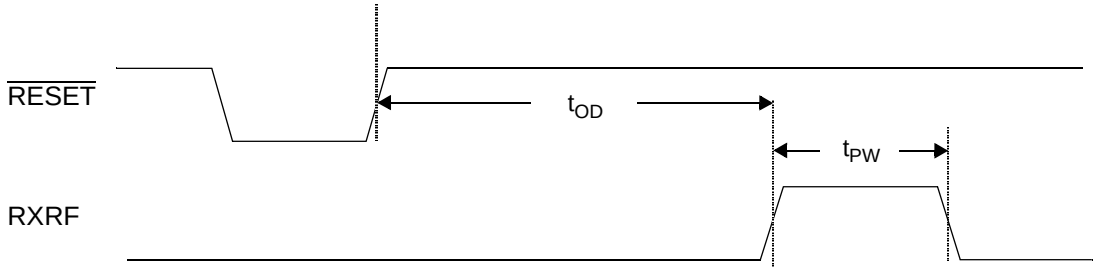
Parameter	Symbol	Min	Typ	Max	Unit
RXBDn output delay after RXBC↓	$t_{OD(1)}$	0.0		6.0	ns
B1ERR output delay after RXBC↓	$t_{OD(2)}$	0.0		6.0	ns

Figure 22. B1 Error Pulse Nibble Timing
(Four time slots are illustrated; up to eight bits may be in error in a given frame)



Parameter	Symbol	Min	Typ	Max	Unit
RXBDn output delay after RXBC↓	$t_{OD(1)}$	0.0		6.0	ns
B1ERR output delay after RXBC↓	$t_{OD(2)}$	0.0		6.0	ns

Figure 23. $\overline{\text{RESET}}$ Receive Reference Timing



Parameter	Symbol	Min	Typ	Max	Unit
RXRF output delay after $\overline{\text{RESET}}$ ↑	t_{OD}	51.44		130	ns
RXRF pulse width	t_{PW}		51.44		ns

OPERATION

POWER SUPPLY

The SYN155C has separate supply pins for V_{DD} and V_{PECL} which provide internal circuit isolation. It is recommended that separate planes and bypass networks be used for connecting the VDD and PVDD supply pins on the SYN155C to +5 volts. Each bypass network consists of a 10 microfarad capacitor in parallel with a 0.1 microfarad capacitor as shown in Figure 24. These 0.1 microfarad capacitors should be of RF-quality and closely connected to decouple each of the device's voltage leads to ground. Since the SYN155C is surface mounted, it may be necessary to mount the decoupling capacitors on the other side of the board so they are in close proximity to the device pins.

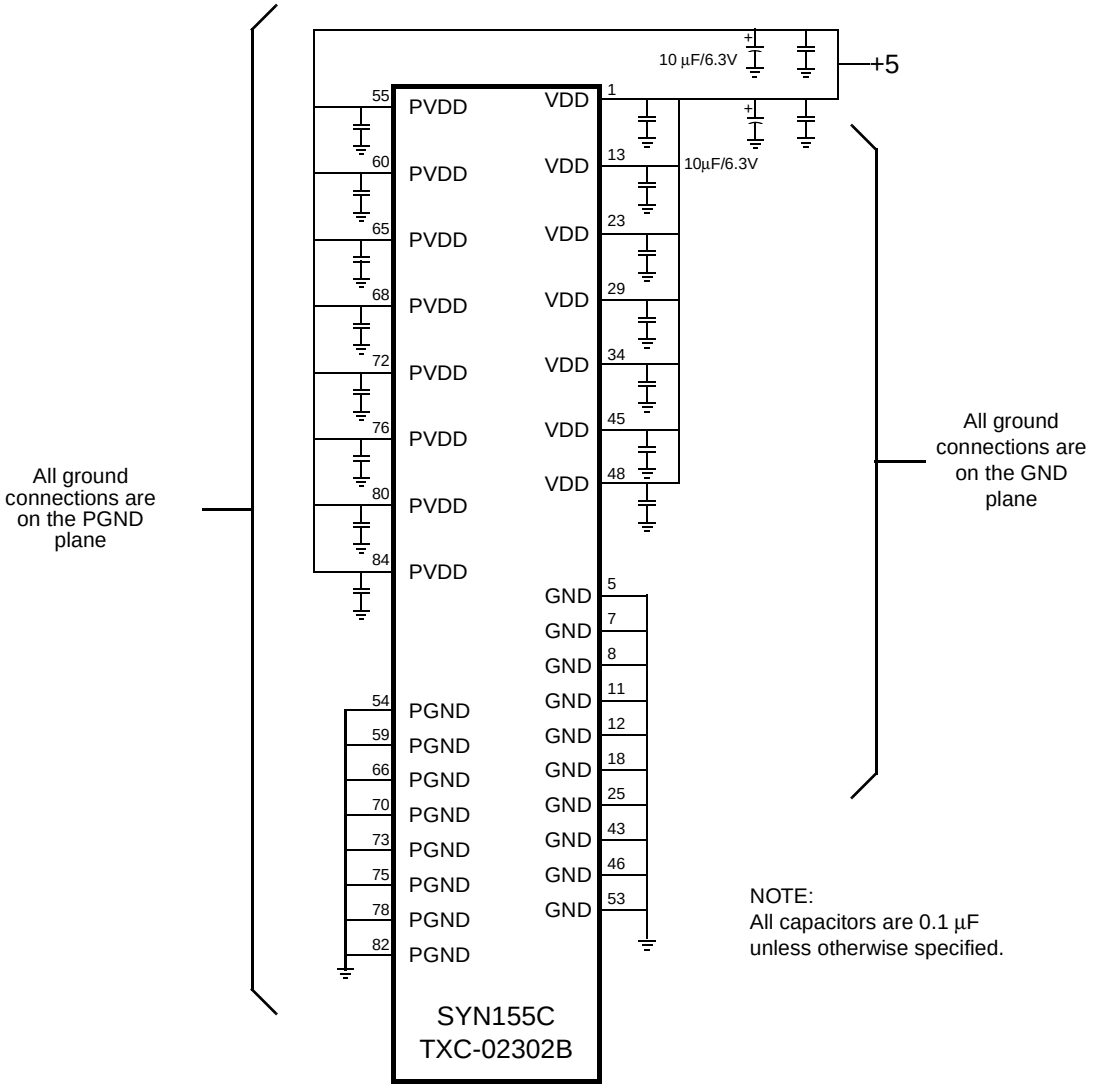
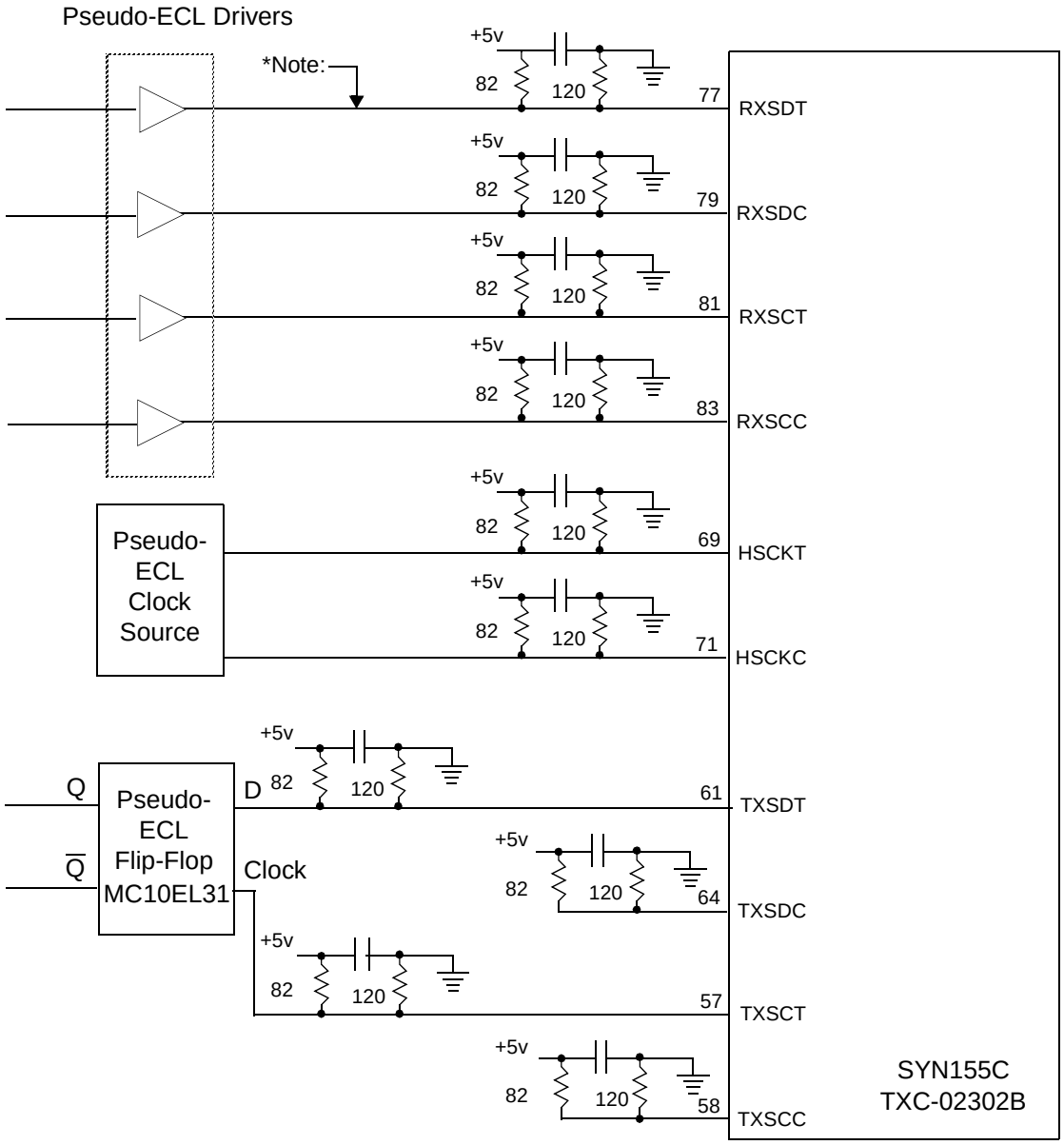


Figure 24. SYN155C Power Supply Connections

PSEUDO-ECL TERMINATIONS

Pseudo-ECL interface circuits between the SYN155C and other devices must be properly designed to avoid problems. At 155 Mbit/s, all interface lines should be treated as transmission lines and be terminated correctly. The SYN155C pseudo-ECL pins must be terminated with external 50-ohm circuits. Figure 25 shows the correct method of terminating the pseudo-ECL traces. For optimum performance, termination networks should be located as close as possible to the destination end of the trace. The pseudo-ECL flip-flop (Motorola MC10EL31 or equivalent) reduces jitter on the TXSDT output. This allows Telcordia (Bellcore) and ITU-T (CCITT) jitter requirements to be satisfied. All PCB traces are designed for 50 ohm controlled impedances. A suggested reference for PCB design information is the Motorola “MECL System Design Handbook.”



*Note: All circuit traces are designed for 50 ohm controlled impedance. All capacitors are 0.1 µF.

Figure 25. Pseudo-ECL Terminations

INITIALIZATION

The initialization sequence is as follows:

1. Apply power.
2. Apply high-speed clock.
3. Apply line input clock.
4. Set the mode controls.
5. Pulse the $\overline{\text{RESET}}$ pin.
6. Pulse the $\overline{\text{OOFN}}$ pin after the $\overline{\text{RESET}}$ becomes inactive.

LOSS OF RECEIVE LINE CLOCK AND DATA

The state of the receive terminal side data bus RXBD(7-0) during loss of receive line signal is dependent upon the state of the BSCRM input pin and the state of the receive line data.

If the BSCRM pin is low, the receive terminal data bus will follow the receive line data value, i.e., if RXSDT is high and RXSDC is low, the RXBD(7-0) bus will be all ones, but if RXSDT is low and RXSDC is high, the RXBD(7-0) bus will be all zeros.

If the BSCRM pin is high, the RXBD(7-0) bus will contain random data, which is a function of the operation of the descrambler and the state of the RXSDT/RXSDC pins.

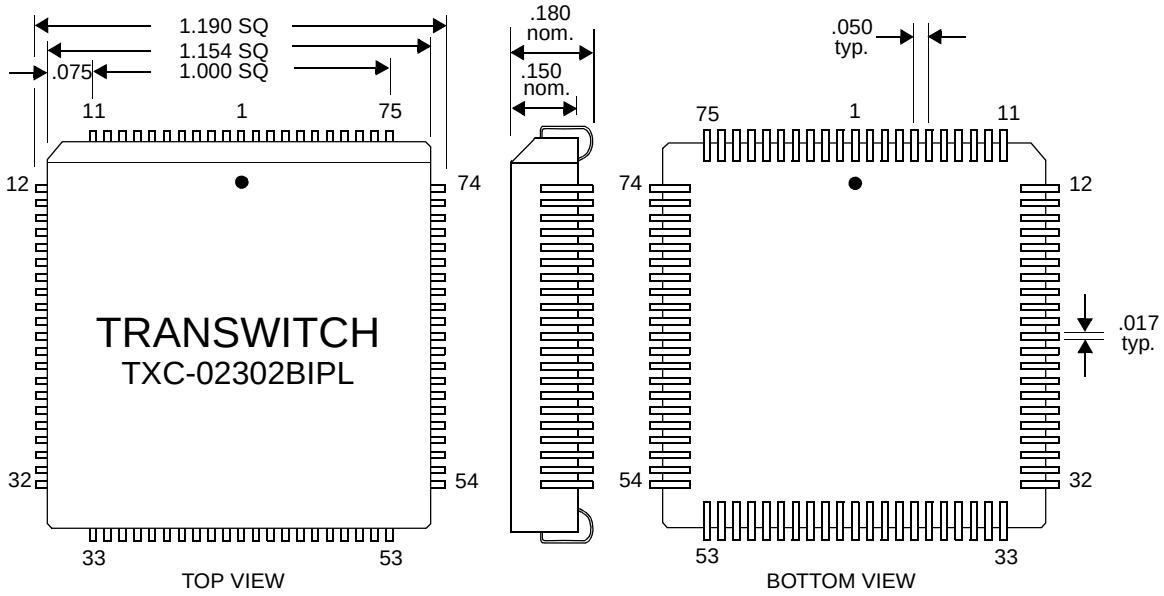
The receive terminal interface does not switch over to another clock during loss of receive line clock. Instead, the receive terminal clock and data signals stop. The RXBD(7-0) data bus signal values will be frozen at the values present when the clock stopped.

THROUGHPUT DELAY

The throughput delay from the receive line to the receive terminal is 54 Unit Intervals and the throughput delay from the transmit terminal to the transmit line is 44 Unit Intervals (where a Unit Interval is 6.43 nanoseconds).

PACKAGE INFORMATION

The SYN155C device is packaged in an 84-pin plastic leaded chip carrier suitable for socket or surface mounting, as shown in Figure 26. All dimensions shown are in inches and are nominal unless otherwise noted. All dimensions and notes for the specified JEDEC outline apply.



(JEDEC Outline MS-018)

Figure 26. SYN155C TXC-02302B 84-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

TXC-02302BIPL	84-Pin Plastic Leaded Chip Carrier

RELATED PRODUCTS

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device satisfies requirements for STM-1, STS-3, and STS-3c signals. It can be used to precede the SYN155C in the byte mode of operation.

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device provides access to all STS-1 overhead bytes in both the receive and transmit directions.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

2570 West El Camino Real
Suite 304
Mountain View, CA 94040

Tel: 650-949-6700
Fax: 650-949-6705
Web: www.atmforum.org

ATM Forum Europe Office

Av. De Tervueren 402
1150 Brussels
Belgium

Tel: 2 761 66 77
Fax: 2 761 66 79
Web: www.euroinfo@atmforum.ocm

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698
Web: www.apinfo@atmforum.com

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
7730 Carondelet Avenue, Suite 407
Clayton, MO 63105-3329

Tel: 800-854-7179 (within U.S.A.)
Tel: 314-726-0444 (outside U.S.A.)
Fax: 314-726-6418
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia Antipolis Cedex
France

Tel: 4 92 94 42 22
Fax: 4 92 94 43 33
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: 800-669-6857 (within U.S.A.)
Tel: 903-769-3717 (outside U.S.A.)
Fax: 508-650-1375
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5111
Fax: 22 733 7256
Web: www.itu.int

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: 215-697-2179
Fax: 215-697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
2575 NE Kathryn Street #17
Hillsboro, OR 97124

Tel: 800-433-5177 (within U.S.A.)
Tel: 503-693-6232 (outside U.S.A.)
Fax: 503-693-8344
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (within U.S.A.)
Tel: 908-699-5800 (outside U.S.A.)
Fax: 908-336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated SYN155C Data Sheet that have significant differences relative to the previous, and now superseded, SYN155C Data Sheet:

Updated SYN155C Data Sheet:	Edition 5, January 2000.
Previous SYN155C Data Sheet:	Edition 4, September 1994.

The page numbers indicated below of this updated data sheet include changes relative to the previous data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
2	Updated Table of Contents.
3	Added List of Figures.
5	Changed second paragraph.
6	Changed Name/Function column text for last row in table.
7	Changed Name/Function column text for Symbol HSCKT.
9	Changed Name/Function column text for Symbol LOF.
10	Changed Name/Function column text for Symbol BSCRM.
12	Renamed first table. Made extensive changes to first table and its notes and deleted rows for Symbols P_C and T_J. Added maximum value and test conditions and deleted second row in second table. Added typical values in last two rows of third table.
14	Added last two rows to second table.
15	Changed “-” to “+” in third line of text paragraph.
26	Deleted pins 62 and 63 from set of PGND pins in Figure 24.
27	Added two sentences near end of text paragraph. In Figure 25, clarified location of external termination components for pins 61, 64, 57 and 58, and added pseudo-ECL flip-flop for pins 61 and 57.
28	Added the “Loss of Receive Line Clock and Data” and “Throughput Delay” sections.
29	Changed JEDEC Outline to MS-018 and added part number in the diagram for Figure 26.
30	Changed content of “Related Products” section.
31	Changed content of “Standards Documentation Sources” section.
33	Changed content of “List of Data Sheet Changes” section.
37	Changed content of “Documentation Update Registration Form” section.

- NOTES -

- NOTES -

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DOCUMENTATION UPDATE REGISTRATION FORM

If you would like to receive updated documentation for selected devices as it becomes available, please provide the information requested below (print clearly or type) then tear out this page, fold and mail it to the Marketing Communications Department at TranSwitch. Marketing Communications will ensure that the relevant Product Information Sheets, Data Sheets, Application Notes, Technical Bulletins and other publications are sent to you. You may also choose to provide the same information by fax **(203.926.9453)**, or by e-mail **(info@txc.com)**, or by telephone **(203.929.8810)**. Most of these documents will also be made immediately available for direct download as Adobe PDF files from the TranSwitch World Wide Web Site (**www.transwitch.com**).

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